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ABSTRACT

These military-developed curriculum materials consist of three volumes of self-paced, individualized training manuals for use by those studying to be electronic computer systems technicians. Covered in the individual volumes are the following topics: computer principles (number sytems, computer circuits, computer components, computer units, input-output units, and computer power supples); general maintenance (supervision and training, general maintenance, equipment identification, and testing equipment); and system maintenance (adjustments, alignments, programming, and troubleshooting). Each volume contains a text with charts and diagrams as well as a workbook with objectives, assignments, review exercises and answers, and volume review exercises. (MN)

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MILITARY CURRICULUM MATERIALS

The military-developed curriculum materials in this course package were selected by the National Center for Research in Vocational Education Military Curriculum Project for dissemination to the six regional Curriculum Coordination Centers and other instructional materials agencies. The purpose of disseminating these courses was to make curriculum materials developed by the military more accessible to vocational educators in the civilian setting.

The course materials were acquired, evaluated by project staff and practitioners in the field, and prepared for dissemination. Materials which were specific to the military were deleted, copyrighted materials were either omitted or approval for their use was obtained. These course packages contain curriculum resource materials which can be adapted to support vocational instruction and curriculum development.

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Military Curriculum Materials for Vocational and Technical Education

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The National Center for Research in Vocational Education

Military Curriculum Materials Dissemination Is . . .

an activity to increase the accessibility of military-developed curriculum materials to vocational and technical educators.

This project, funded by the U.S. Office of Education, includes the identification and acquisition of curriculum materials in print form from the Coast Guard, Air Force, Army, Marine Corps and Navy.

Access to military curriculum materials is provided through a "Joint Memorandum of Understanding" between the U.S. Office of Education and the Department of Defense.

The acquired materials are reviewed by staff and subject matter specialists, and courses deemed applicable to vocational and technical education are selected for dissemination.

The National Center for Research in Vocational Education is the U.S. Office of Education's designated representative to acquire the materials and conduct the project activities.

Project Staff:

Wesley E. Budke, Ph.D., Director
National Center Clearinghouse

Shirley A. Chase, Ph.D.
Project Director

What Materials Are Available?

One hundred twenty courses on microfiche (thirteen in paper form) and descriptions of each have been provided to the vocational Curriculum Coordination Centers and other instructional materials agencies for dissemination.

Course materials include programmed instruction, curriculum outlines, instructor guides, student workbooks and technical manuals.

The 120 courses represent the following sixteen vocational subject areas:

- Agriculture
- Aviation
- Building & Construction Trades
- Clerical Occupations
- Communications
- Drafting
- Electronics
- Engine Mechanics
- Food Service
- Health
- Heating & Air Conditioning
- Machine Shop
- Management & Supervision
- Meteorology & Navigation
- Photography
- Public Service

The number of courses and the subject areas represented will expand as additional materials with application to vocational and technical education are identified and selected for dissemination.

How Can These Materials Be Obtained?

Contact the Curriculum Coordination Center in your region for information on obtaining materials (e.g., availability and cost). They will respond to your request directly or refer you to an instructional materials agency closer to you.

CURRICULUM COORDINATION CENTERS

EAST CENTRAL
Rebecca S. Douglass
Director
100 North First Street
Springfield, IL 62777
217/782-0759

MIDWEST
Robert Patton
Director
1515 West Sixth Ave.
Stillwater, OK 74704
405/377-2000

NORTHEAST
Joseph F. Kelly, Ph.D.
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225 West State Street
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609/292-6562

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206/753-0879

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1776 University Ave.
Honolulu, HI 96822
808/948-7834

ELECTRONIC COMPUTER SYSTEMS REPAIRMAN

Table of Contents

Volume 1

General Maintenance - Text Material Page 1
General Maintenance - Workbook Page 97

Volume 1A

Computer Principles - Text Material Page 166
Computer Principles - Workbook Page 335

Volume 2

System Maintenance - Text Material Page 399
System Maintenance - Workbook Page 505

ELECTRONIC COMPUTER SYSTEMS REPAIRMAN

Developed by:

United States Air Force

Development and Review Dates:

Unknown

Occupational Area:

Electronics

Cost:

Print Pages:

594

Availability:

Military Curriculum Project, The Center for Vocational Education, 1960 Kenny Rd., Columbus, OH 43210

Suggested Background:

Knowledge of number systems

Target Audiences:

Grades 10-adult

Organization of Materials:

Student workbooks with objectives, assignments, review exercises and answers, volume review exercises, charts and diagrams; text

Type of Instruction:

Individualized, self-paced

Type of Materials:			No. of Pages:	Average Completion Time:
Volume 1A	–	*Computer Principles*	163	Flexible
		Workbook	63	
Volume 1	–	*General Maintenance*	82	Flexible
		Workbook	65	
Volume 2	–	*System Maintenance*	102	Flexible
		Workbook	83	

Supplementary Materials Required:

Technical maintenance manual for any particular system the students are studying

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Course Description:

This course is designed to upgrade the Apprentice (semi-skilled) repairperson to the Specialist (skilled) level. There is much basic information for persons who have no computer background. The more advanced material is designed for use in conjunction with a laboratory or on-the-job learning situation.

Electronic Computer Systems Repairman contains three volumes with workbooks, texts, exercises, volume reviews, and supplementary charts.

Volume 1A	–	*Computer Principles* is review material designed to present basic knowledge of computer principles and enhance understanding of computer circuits. It covers number systems, computer circuits, computer components, computer units, input-output units and computer power supplies.
Volume 1	–	*General Maintenance* identifies tasks and presents analytical studies which provide in-depth insight into the tasks and relates these tasks to specific areas of equipment. Each task is broken into subtasks. Because specific subtasks will differ with the computer system, the text refers the students to technical maintenance manuals for specific procedures. The general topics covered by this volume include supervision and training, general maintenance, equipment identification, and test equipment. The final chapter on equipment modification was deleted because of references to specific military procedures and forms. One section on reference designations for electrical and electronic parts and equipment was also deleted because of copyright considerations.
Volume 2	–	*System Maintenance* again includes analysis of the tasks of operational performance such as adjustments, alignments, programming and troubleshooting. During each study, all aspects of or parts of each task are identified and the placement of these parts in their proper perspective is explained. References are made to technical maintenance manuals for any particular system the students are using.

This course on electronic computer systems was designed to provide basic information for persons wishing to upgrade their skills. The materials are individualized with student workbooks and self-evaluation. The more advanced materials should be used in conjunction with a laboratory or on-the-job situation which allows practice of the principles learned in the theory portion. In addition particular maintenance tasks and schedules will vary according to the systems being used. The course volumes refer to military technical orders which outline the specific tasks and steps in the basic functions of maintenance and repair. The maintenance manual of the system being used should be substituted for those references.

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CDC 30554

ELECTRONIC COMPUTER SYSTEMS REPAIRMAN

(AFSCs 30554/54A/54B/54C/54D)

Volume 1

General Maintenance

7-4

Extension Course Institute
Air University

11

DEPARTMENT OF THE AIR FORCE

PREPARED BY
KEESLER AIR FORCE BASE
MISSISSIPPI, AIR TRAINING COMMAND

EXTENSION COURSE INSTITUTE, GUNTER AIR FORCE BASE, ALABAMA

THIS PUBLICATION HAS BEEN REVIEWED AND APPROVED BY COMPETENT PERSONNEL
OF THE PREPARING COMMAND IN ACCORDANCE WITH CURRENT DIRECTIVES ON DOCTRINE,
POLICY, ESSENTIALITY, PROPRIETY, AND QUALITY.

2

Preface

THIS TWO-VOLUME course, 30554, *Electronic Computer Systems Repairman*, is prepared to carry on the training begun at the resident training center for those trainees on upgrade training. It also provides knowledge about maintenance of electronic computer and data processing tasks for persons not on upgrade training.

The approach to training used in this CDC is one of identification of a task and then presentation of an analytical study. The study provides an in-depth insight into the task and also relates the task to specific areas of equipment. Each task analyzed is broken into its subtasks. The subtasks, after being explained, are placed in relative importance when applicable.

Since tasks are identified in many specific technical orders, technical order references are made under a separate heading in most sections. The definition of subject matter listed in the text as being found in a particular technical order has been taken from Technical Order 00-5-1, *AF Technical Order System;* however, certain manufacturers of electronic equipment have provided technical orders slightly different in structure from those listed in this text. If you find that your technical orders are designated by section and are contained in, for instance, the -2 service manual, you probably will find the logic circuits in Section III or Chapter 3. Generally, however, the logic diagrams are located in the -3 circuit diagram manual.

For your convenience in studying this volume we have placed in the workbook 23 figures, a chart, and 6 tables to which there is extended or frequent reference. Also an index to key elements has been included in this volume for quick reference.

If you have questions on the accuracy or currency of the subject matter of this text, or recommendations for its improvement, send them to Tech Tng Cen (TTOC), Keesler AFB, MS 39534.

If you have questions on course enrollment or administration, or on any of ECI's instructional aids (Your Key to Career Development, Study Reference Guides, Chapter Review Exercises, Volume Review Exercise, and Course Examination), consult your education officer, training officer, or NCO, as appropriate. If he can't answer your questions, send them to ECI, Gunter AFB, Alabama 36118, preferably on ECI Form 17, Student Request for Assistance.

This volume is valued at 36 hours (12 points).

Material in this volume is technically accurate, adequate, and current as of March 1972.

3

Acknowledgment

Chapter 3, Section 6, of this volume contains material which has been extracted from *Reference Designations for Electrical and Electronic Parts and Equipments* (Y32.16 — 1968), by permission of United States of America Standards Institute, New York, N.Y.

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CHANGE SUPPLEMENT

CDC 30554

ELECTRONIC COMPUTER SYSTEMS REPAIRMAN

(AFSCs 30554/54A/54B/54C/54D)

Volume 1

IMPORTANT: Make the corrections indicated in this supplement before beinning study of this volume. This supplement contains both "pen-and-ink" changes and replacement pages. It is perforated and three-hole-punched so that you can tear out the replacement pages and insert them in your volume.

CHANGES FOR THE TEXT:

Pen-and-Ink Changes:

Page	*Paragraph*	*Line(s)*	*Correction*
6	2-6	2	Change "3ABR30554B-1" to "3ABR30554-3."
6	2-6	11	Change "B 1" to " 3."
57	7-7.*b*(5)	6	Change second "A641" to "A841."
64	Fig. 62		Change title to read "Negative and positive triggering level with negative triggering slope."
64	Fig. 63		Change title to read "Negative and positive triggering level with positive triggering slope."
66	8-16	6	Change "20,000" to "25,000."
73		14	Change ".05-volt" to "0.5-volt."
79	8-75	10	Delete "(Refer to fig. 87,A.)"
		12	Change "87,A" to "87,B."
81			Chart 2, Group IV. Change "50,000 to 250,000 megohms" to "50,000 to 500,000 megohms."
81	8-78	2	Fourth display dot. Change "25,000 megohms" to "500,000 megohms."
84	8-95	8	Change "16-MA" to "16 micro A."

5

Page	*Paragraph*	*Line(s)*	*Correction*
		10	Change "160-MA" to "160 micro A."
90	9-18	2	After "relatively" insert "simple."
99	11-2	2,3	Delete "Materiel Control, Records, Reports, and Administration."
99	11-5,*a*	1	Change "TO 00-20-2-1" to "TO 00-20-2."
99	11-5,*d*	1	Delete "*Historical Records and.*"
99	11-5,*f*	1-6	Delete.
100	12-2	16-22	Delete beginning with "Observe the flow chart . . . the work centers."
100	12-3	2,3	Delete "from the Maintenance Control Section."
		6	Change "records" to "documentation."
100	12-4	1	Change "**Records.** The Records Section" to "**Documentation.** The Documentation Section."
		8	Change "the Records Section" to "the Documentation Section."
		9,10	Change "Workload Control for scheduling" to "Plans and Scheduling."
101	12-5	1	Change "Records" to "Documentation."
		5	Change "TOs 00-20-4 and 00-20-10-4" to "TO 00-20-4."
101	12-5	13,14	Change "Air Materiel Area (AMC)" to "Air Logistics Center (ALC)."
		24	Change "Records" to "Documentation."
101	12-7	3	Change "Workload Control for scheduling" to "Plans and Scheduling."
101	12-8	1	Change "**Workload Control**" to "**Plans and Scheduling.**"
105	14-17	2	Delete "through Maintenance Control."
		3	Delete "(check fig. 114, in the workbook)."
109	15-14	11	Delete "(2) DD Form 829-1."
		14,15	Change "TOs 00-20-4 and 00-20-10-4" to "TO 00-20-4."
110	Fig. 118		In the active portion, change "PCN REPORT (CURRENT) 9 LOG-K75" to "PCN REPORT (CURRENT) (LOG-MMO (M) 7124)."
111	16-6	5	Change "(9 LOG K75)" to "(LOG-MMO (M) 7124)."
119	Section T	24	Change "00 20 2-1" to "00 20-22."

Page Changes: Remove and insert new pages as indicated:

Remove Pages	*Insert Pages*
7 10	7 10
107 108	107 108

16

Contents

Page

Preface .... *iii*

Acknowledgment *iv*

Chapter

1 Supervision and Training 1

2 General Maintenance 14

3 Equipment Identification 51

4 Test Equipment 62

5 Equipment Modification 98

Appendix *113*

Index *117*

8

MODIFICATIONS

Chapter 1 of this publication has (have) been deleted in adapting this material for inclusion in the "Trial Implementation of a Model System to Provide Military Curriculum Materials for Use in Vocational and Technical Education." Deleted material involves extensive use of military forms, procedures, systems, etc. and was not considered appropriate for use in vocational and technical education.

CHAPTER 2

General Maintenance

THIS CHAPTER presents analysis of tasks performed in general maintenance. These tasks include performance routines, replacement, repair, and servicing. The study of repair and replacement of defective components includes a study of soldering.

3. Performance Routines, Repairs, and Operational Checks

3-1. The general maintenance functions performed by most 305XXs fall in the category of preventive maintenance routines and the repairing or replacing of electronic components. Included are such tasks as service, inspect, repair, replace and validate, and the performance of operational checks associated with these tasks. To help achieve a clear understanding of your job responsibilities in relation to the tasks, it becomes important for you to analyze why a task is performed and understand the consequences if you fail to accomplish the task. What are some of the features of maintenance routines? What is accomplished by their performance? What areas of responsibilities are included? What repairing tasks will you need to perform and what problems will you encounter? What repair skills will you need to develop? This text discusses answers to these questions.

3-2. **Service Routines and Operational Checks.** Generally, a maintenance routine requires you to clean and service equipment so that optimum equipment operation is obtained. Improper performance of these tasks can and does result in equipment status deterioration, intermittent error problems, and corrosion. In the following paragraphs you will read about situations that arise because these routines are performed haphazardly and when, how, and why repairs are made to components of a system.

3-3. You, the maintenance man, are the only one who can insure that the operations personnel have workable equipment. It therefore becomes necessary for you to have a personal feeling of accomplishment about working on the equipment in your work center. To best attain this feeling, look closely at the task to be done, analyze the task, and determine that the performance of the task will (1) provide better operational equipment for operations personnel, (2) increase the system reliability by decreasing the chance for failure, and (3) make a more presentable looking piece of equipment. The visual appearance of the equipment shows what type of maintenance repairman you really are. If the equipment is clean, even spotless, then it is easily surmised that its operational capability will be good. However, if the equipment is dirty, it follows that repair work accomplished will very likely be slovenly, crude, and poorly accomplished, and eventual system deterioration is inevitable.

3-4. **Analysis.** Perhaps the term "analysis" is new to you. Its meaning as related to your performance of tasks must be clearly understood in order for you to become a skilled technician. Fortunately, in the electronics career field all steps in our analysis are logical; no arbitrary philosophies or generalities exist. So analysis consists of:

a. Determining the objective. This is done by identifying the task to be performed; i.e., perform a PMI, replace a lamp, etc.

b. Determining the steps involved in accomplishment of the task. In preventive maintenance routines, the steps are already listed. In removal and replacement of components, the steps may or may not be listed in the TO, but they must be identified and listed.

c. Determining what principles or characteristics or specific requirements must be considered while the task is being performed. These areas include (1) possible impact on the system, such as power requirements, interruption of system operation, and partial loss of system capability; (2) physical adjacent subelements involved; (3) removal of other units to facilitate repair; and (4) the use of associated test equipment and testing procedures needed to effect repair.

3-5. Many areas are included in this type of work. Many types of devices are used to provide maintenance personnel with indicators to tell them that problem areas are developing. Some of these are visual indications such as lights, fuses, and switches; dirt and corrosion; meters and temperature readings. Other indications are audio, such as noisy motors, gears and belts, and squeaky doors.

3-6. Notice that in these areas of your responsibility, the tasks are related to both mechanical and electrical parts of the electronic and mechanical equipment. But you must also understand the equipment operation pertaining to these areas and where to find information about them.

3-7. *Use of technical orders.* In which technical order will the steps for this work normally be found? Since you are on a site and/or in a work center, you probably know that your work cards (a term usually assigned to PMIs) are designed and printed on hard card paper instead of regular TO pages. This book has a definite TO number and for most systems in the United States Air Force, the book is readily identifiable by the insertion of the letters "WC" in the last part of the technical order number. Below are some examples:

31P1-2GPA73-52-6WC
31P1-2FST2-106WC-1

3-8. Also notice that each of these technical orders is in the -6 technical order series. Therefore, when looking for and identifying preventive maintenance routines, refer to the index for the technical order and specifically look for the listing containing "6WC."

3-9. Another technical order which is important for you to know and be able to identify is the technical order showing removal and replacement of components. In most Air Force systems this book is an Air Force technical order; however, some systems use commercial publications for repair and replacement procedures of components. In Air Force technical orders, the information and procedures for replacement of components are usually found in Chapter 5 of the service manual, the -2 technical order, for that series. The -2 technical order also contains the theory of operation of a piece of equipment in an earlier chapter, as well as the characteristics of the equipment.

3-10. Servicing, Inspecting, Replacing, and Validating. As we stated in a previous paragraph, cleanliness and operational readiness of even the smallest component in a system is of paramount importance. So it then becomes necessary for you to be aware of environment and physical properties of moving parts that can cause deterioration to system function.

3-11. Let us explore a few applications of preventive maintenance routines. Also, let us see if the failure to perform these tasks could result in failure of the entire system.

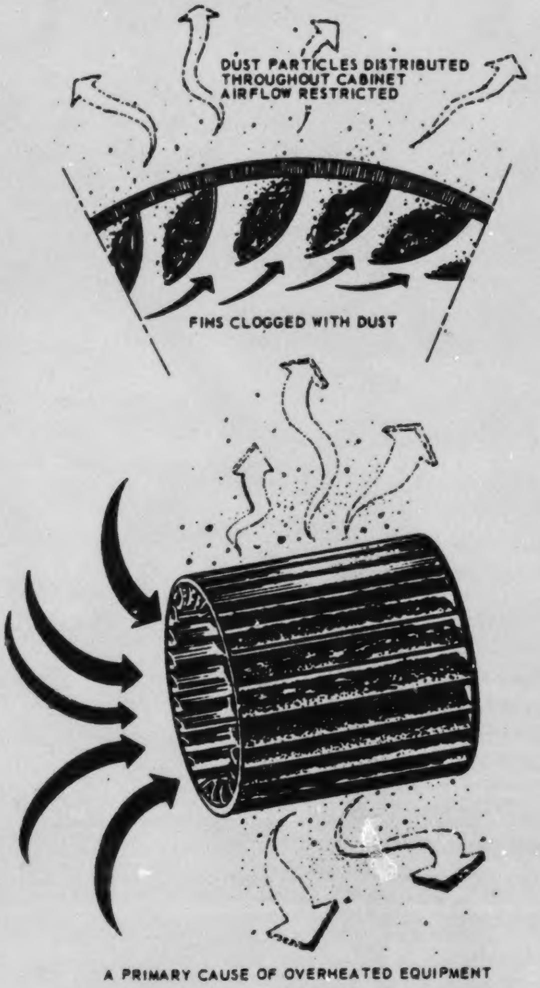

DUST PARTICLES DISTRIBUTED
THROUGHOUT CABINET
AIRFLOW RESTRICTED
FINS CLOGGED WITH DUST
A PRIMARY CAUSE OF OVERHEATED EQUIPMENT

Figure 6. Squirrel cage.

3-12. *Cleaning and lubricating air-conditioning systems.* Refer to figure 6. A typical instruction could be "*Step 1. Inspect motor, belt, and attached squirrel cage for cleanliness, proper operation, satisfactory condition, and oil.*" A simple enough step, although rather routine and unglamourous. But, what happens if the squirrel cage becomes clogged with dirt, or the belt dries and cracks, or the motor bearings become dry and burn? Your task is twofold. First, visually inspect the unit and determine the condition as clean or dirty, inspect the belt for cracks and wear, and listen for dry running motor operation; second, clean and lubricate the unit. Failure to do the task well often results in equipment downtime. Analysis of the conditions listed above is as follows: First, decrease in air flow through the entire cabinet or system results if proper cleaning of the air conditioning system is not performed. The reduction of airflow causes an increase in ambient temperature throughout the cabinet or system, increasing the possibility of intermittent failures. Second, a broken belt or frozen motor bearing causes equipment failure and results in unscheduled downtime to the work center, loss to the net, and to the Air Force mission.

3-13. Your job, then, is to prevent the need for troubleshooting and to prevent a system failure. Perform this routine with care and a definite attitude that the operation of your systems depends on it. The following are typical steps in servicing:

(1) Remove power.
(2) Remove or make access to the unit.
(3) Clean, inspect, lubricate.
(4) Reinstall, check.
(5) Restore power.

3-14. *Cleaning and inspecting cabinets, drawers, and modules.* Again the enemy is dirt and dust, grime and grease. As before, your job success depends on your ability to combat these agents.

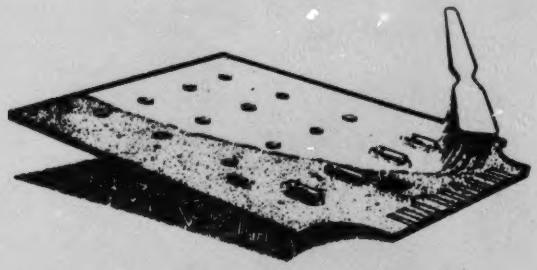


Figure 7. Dirty module.

3-15. The dirty module, shown in figure 7, may cause you to recall from your studies in basic principles what effect these agents have on circuit components. With smaller units such as printed circuit boards, microelectronics circuits, and even vacuum-tube circuits, these agents become extremely important. They may act as insulators or conductors or corrosive agents. They can often cause a distorted waveform, cause an oscillator frequency shift, or cause a phase shift in microseconds which could result in intermittent problems and equipment malfunction.

3-16. The following are typical steps in cleaning:

(1) Clean component boards, screen filters, air passages, and cables.

(2) Vacuum cabinets to allow complete air circulation.

(3) Clean dirt and grime from contacts for good electrical signal flow.

3-17. *Inspecting and servicing read and write heads used with magnetic devices.* A typical instruction could be: "Clean heads daily," or "Lubricate tape drives." What are the two most dangerous enemies of magnetic tape/drum systems? Answer: (1) Residue from the tape or drum surface being deposited on the heads and (2) magnetizing of the heads themselves. In data processing systems, some form of storage is generally used. Often these systems employ, as in the SAGE, AN/FST-2, a drum coated with oxide; or in the 465L, SACCS system, a magnetic tape unit for stored programs; or in the 412L or BUIC system, a computer with tape programs. These units require constant cleaning because of the properties of magnetic flux in the

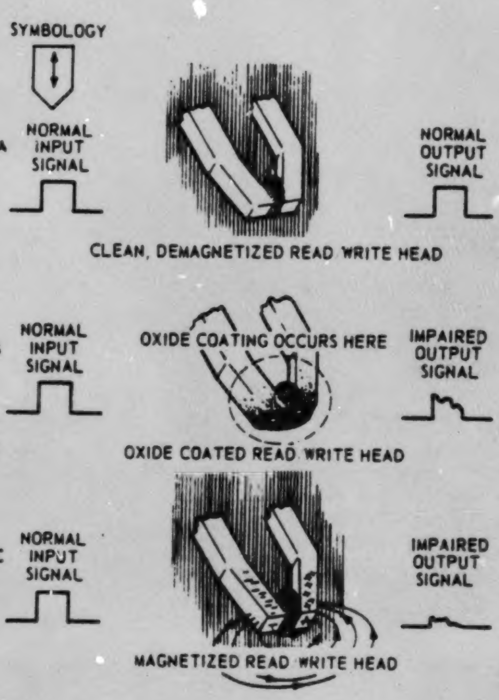


Figure 8. Magnetic heads, clean and not clean.

heads, and the loss of oxide from the tape or drum surfaces to the heads. As the flux or oxide is transferred to the heads and surrounding area, signal loss increases and system signal deterioration rapidly increases. Range data, alert messages, and problem block data are often garbled, incomplete, and of no value because of these conditions.

3-18. When we speak of magnetic flux and oxide deposits on heads, what are we talking about? Look at figure 8 and observe what happens as magnetic fields build up; notice how the response falls off. See how, because flux is present, that less of the signal is passed into or out of the read-write heads. Again look at the illustration and see how a buildup of oxide deposits interferes with the passing of signals into and from the tape when recording or playing.

3-19. Typical steps in servicing include:

(1) Clean visually all dirt and oxidation from heads.

(2) Demagnetize heads according to specific instructions with proper degaussing tool. (Remove built-up magnetic flux.)

(3) Lubricate tape drives with proper chemical agent.

(4) Visually examine heads for pitting, cracks, scars, or any other indication which could result in signal loss. (Use magnifying glass.)

(5) Return equipment to operational status.

(6) Check operational status.

3-20. We have examined some of the important areas in a data processor where failure of the maintenance man to perform his cleaning and lubricating task could result in the loss of equipment operational capability. The tasks in themselves are not difficult, but analysis of the tasks as described in this text explains their importance and relates the tasks to the impact these have on the equipment's operational capability and the mission of the unit, wing, and command. Let us now take a look into another area of general maintenance.

3-21. **Replacing Lights, Fuses, and Switches.** In the system on which you are now working, lights, fuses, and switches are used in abundance. This is true for all data processors. These are of vital importance to you because they show you the operational capability of the data processor. As more of the systems are changed to solid-state and integrated circuits, quick reliable indicators such as lights or fuses are needed to speed the detection of failure. It then becomes necessary to understand how these indicators are built and installed. Physical features and principles of operation need to be analyzed. The impact on the system during the repair of the unit will be included as a part of the analysis to show the relationship to the task. Logical approaches and basic steps will develop.

3-22. The analysis of this subject includes a study of the types of lamps, their uses, and typical replacement procedures used to restore the circuits to normal operation; the types of fuses normally found in data processors; the types of fuse holders plus typical replacement procedures; and finally, analysis of the switches used on data processors and typical checkout and replacement procedures associated with switches.

3-23. *Lamp and lamp sockets.* Study table 1 (in the workbook) closely because it includes a description of the most common lamps used in data processors. These lamps come in various voltage ranges, sizes, and shapes. Common lamp nomenclatures are given plus their voltage ratings. These are vital for you to understand in the event that you must replace lamps with substitute lamps. Some lamps even contain resistive and capacitive components internally.

3-24. By referring to table 1, showing the lamps, it is easy to see why each lamp requires a special type of socket. Consider the first *lamp*, the *screw base;* its socket is as shown in figure 9. Since only two wires are used, its removal and installation are relatively simple. Observance of wire replacement to the terminals of the new socket must be exercised when reinstalling a new lamp socket. Installing the wires on the wrong terminals is a modification of equipment and is not authorized unless directed.

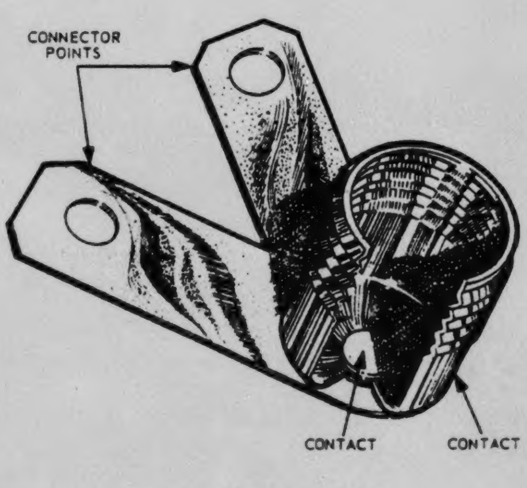


Figure 9. Screw base socket.

3-25. Power, of course, must be removed prior to removing a defective socket and installing a new socket. Precautions must always be taken when these units are worked on because, although the lamp may be using only a low-voltage DC or AC source, a shorting of the source voltage to the chassis can result in complete loss of power to the equipment and result in site downtime.

3-26. A typical removal, reinstallation procedure would be:

(1) Remove power.
(2) Label wires to be removed.
(3) Unsolder wires from socket.
(4) Solder new socket to wires.
(5) Check continuity with a VOM.
(6) Secure socket to chassis with washer and retaining nut.
(7) Apply power and perform operational check.

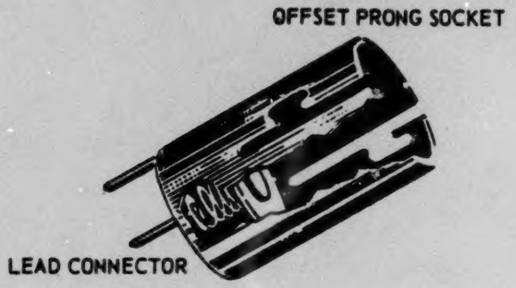


Figure 10. Off-set lamp socket.

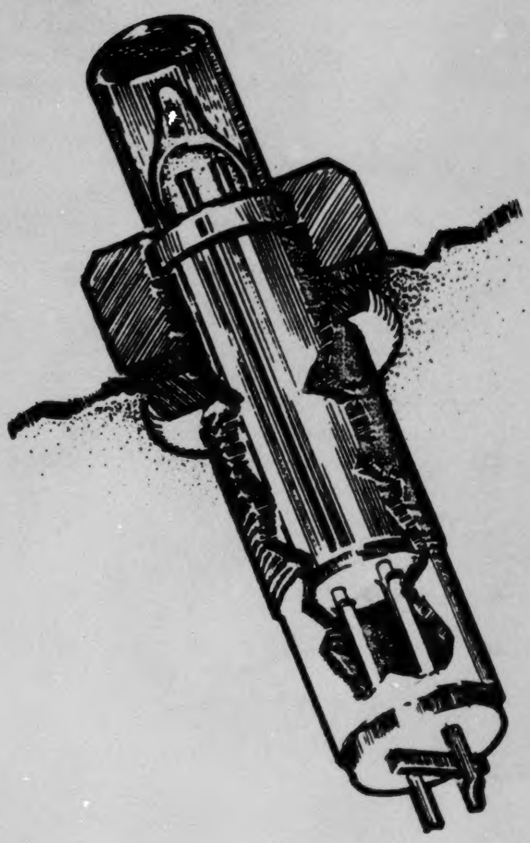


Figure 11. Deep socket, neon.

3-27. The *offset prong plug-in lamp*, as shown in table 1 (2), requires a socket as shown in figure 10. Observe how one side of the socket has a cut higher than the other side to accommodate the prongs on the side of the lamp. Also note that this socket usually contains a spring which pushes the base contact up to the lamp when the lamp is seated properly. The spring allows for insertion of the lamp to seat it properly.

3-28. Installation of a lamp requires:

(1) Aligning the prongs on the lamp with the slots in the lamp socket according to the placement.
(2) Inserting lamp into socket, depressing the spring base.
(3) Twisting the lamp and releasing it, allowing the prongs on the lamp to seat in the slots.

Removal procedures are the reverse of installation. Replacement of lamp holder (socket) is the same as for the screw type.

3-29. The *neon indicator*, shown in table 1 (3), is commonly used in data processors where counter operations are shown, when error indicators are used, and when register operation shows cycling operations. Some of these lamps contain internal resistive and capacitive networks plus lamp filaments. Most of the sockets designed to accommodate this type of lamp are generally 2- to 4-wire connected units. Refer to figure 11 and observe a type of socket which is used. Replacement of this socket requires strict adherance to identification and replacement of leads when reinstallation is performed.

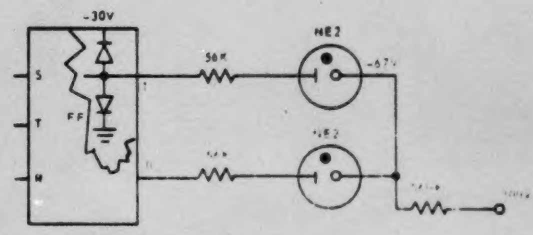


Figure 12. Indicator circuit.

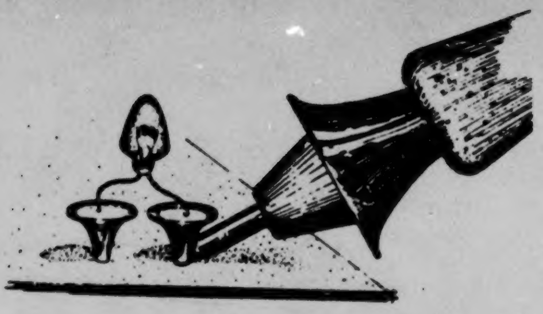


Figure 13. Neon in well socket.

3-30. An installation of this lamp is shown in the schematic in figure 12. The NE2 lamps (shown) are placed in series with the output of the flip-flops. On these flip-flops, internally the signal swing is from 0V to - 30V, depending upon the state of the flip-flop. When the output of the flip-flop is a logic 1 (0V), there is an approximate 67V difference of potential across the lamp, and it lights. In the zero state, the difference of potential is only approximately 37V, and ignition of the neon does not occur. The table shows that neons need 65V to start.

3-31. To stress safety in this area, consider that - 300 VDC is lethal voltage, extreme caution *must* be exercised when working with this area, and power *must* be removed prior to removal and replacement of any lamp socket.

3-32. The neon lamp shown in table 1 (4) is usually found in a power supply. Quite often its purpose is for regulation of the power supply. It may be a plug-in lamp with stiff leads; however, more commonly it is a lamp with no metal base, and it has flexible lead wires protruding from the glass envelope. (Refer to fig. 13.) In power supplies using this lamp, two wells filled with solder are installed to secure the leads of the lamp. Installation and removal consists of heating the envelope with a soldering iron, removing the lamp lead, and then inserting the new lamp lead in the molten solder. Again, any work performed in this area *must* be done with all power removed.

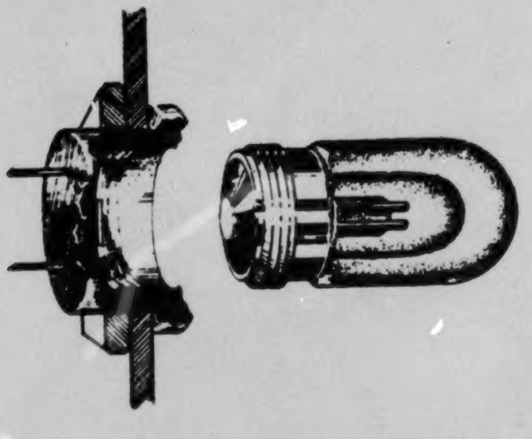


Figure 14. Subminiature socket with neon lamp.

3-33. The final lamp shown in table 1 (5) is a *subminiature lamp*. This lamp is pushed into a glass lens, and the lens is then screwed into the socket as shown in figure 14. This lamp unit usually contains a 2-wire connection; however, it may have multiple leads soldered to one of the two connector points. Strict observance of wire placement is necessary on any removal or replacement of the lamp base. Use procedures outlined in the description of the basic screw lamp.

3-34. The tasks involved in this area of work are basic and simple; yet a few specific practices do become important when analysis is applied. These are:

(1) Mark the wires to be removed and installed on the new socket.

(2) Exercise care in removing and replacing a lamp from the socket after first determining the type of lamp used.

(3) Remove power from the unit before starting any repair action.

(4) Use proper soldering techniques in all cases.

(5) Make a static check with a VOM for continuity prior to applying power.

(6) Apply power and make a dynamic check.

3-35. Learn to recognize the various types of lamps from their appearance, size, use, and description on a schematic or wiring diagram and their voltage ratings. Above all, observe and practice safety to protect yourself and your equipment. A mistake could burn or kill you. A mistake could also destroy your equipment, cause unscheduled downtime, abort a mission, or cause a loss in the net.

3-36. *Fuses and fuse holders.* We have already identified a fuse as an indicator for the maintenance man which will alert him to a defect or malfunction in the system. The primary use of any fuse is, of course, to protect an electronic unit from destruction by excessive current or voltage. This fact then leads to the analysis of fuse applications in the following terms: (1) Where are fuses normally installed? (2) What are the principles of fuse operation? (3) What sizes and shapes are they, and what type holders are provided for them? (4) Finally, what comparisons are there between the removal and replacement

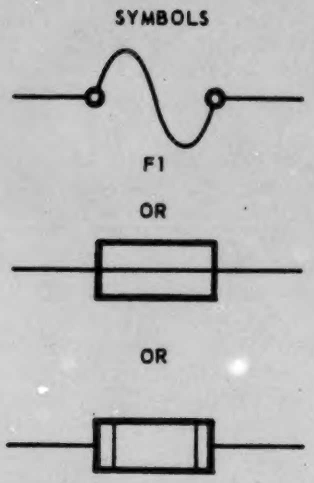


Figure 15. Fuse symbols.

of the holder to that of the lamp holders just discussed.

3-37. Typically, you will find a fuse in an input power line whether it be an AC or DC source voltage. Fuses may be installed on a drawer, a rack, and a chassis, or in a cabinet. They may be remotely placed and still be wired to the circuits of a given unit. The important thing to know is where the fuse circuits are for your equipment. Air-conditioning systems, motors, and cabinet service lights are also examples of circuits that will be fused to prevent destruction by overload in these units. On a wiring diagram you will probably see a fuse as a symbol like those shown in figure 15. The designation will usually be an "F" followed by a number. On the fuse itself will be a number. It will very likely look like this one here. Example:

Part
Number
Breakdown: F01 A 125V 2A
2A — **2-ampere rating**
125V — **125V maximum voltage**
A — **Characteristic (normal-blow)**
F01 — **Style or dimension code (ferrule, glass, size)**

3-38. The current-carrying element in a fuse melts when heated to temperatures in excess of about 170° and opens, thereby removing the source voltage from a unit. Two factors are important in this analysis: first, the type of material used for fusing and its melting properties and; second, the principles of Ohm's and Kirchoff's law as applied to circuits using fuses. In the first instance the current-carrying element used in fuses is engineered to specific thicknesses, lengths, and widths to carry specific voltage and current loads. This metal will heat and remain intact provided the applied heat does not exceed the melting point of the metal. Second, basic laws of electronics apply to selection of fuses for specific circuits. Considerations of (1) total wattage dissipation, (2) total amperage needed to maintain circuit operation, and (3) total voltage requirements must be made when determining size and type of fuse that is to be used.

3-39. How does Ohm's law apply to fuses?

Ohm's Law: $I = \frac{E}{R}$, or $R = \frac{E}{I}$, or $E = IR$, or $P = IE$

Consider a unit using a 125V, 2A fuse. Consider also that the fuse will blow at exactly 2A. What effect can an increase in line voltage have on the fuse? Using the formula $I = \frac{E}{1}$:

$I = 2A$ $E = 125V$ R (resistance of the fuse)

$\uparrow 2A = \frac{125\uparrow}{R\rightarrow}$ = blown fuse (arrows indicate a change)

With the resistance of the fuse wire as a constant, an increase in line voltage causes an increase in current, and the fuse melts. Another problem: What effect can a decrease in resistance within the circuits cause? The power formula $P = \frac{E^2}{R}$ is used. A short circuit in the operating unit will very likely lower the total resistance of the unit to almost ground potential and increase the power requirements by increasing the current flow. Since power is related to heat, the fuse filament will develop more heat and burn through.

$$\uparrow P = \frac{E^2\uparrow}{R\downarrow} = \text{blown fuse}$$

3-40. Another basic principle of electronics is Kirchoff's law. Looking at the schematic in figure 16, observe how, when the fuse is intact, current will flow into the entire circuit through the fuse and not the NE2 lamp circuit because current will always seek the easiest path. However, if the fuse blows, the current path is through the NE2 lamp. This lamp circuit will draw very little current and no damage will result to the circuit. This circuit is used where a visible indicator is used to show a blown fuse.

3-41. Refer to table 2, Fuses and Fuse Holders (in the workbook), and study the different types of fuses normally found in

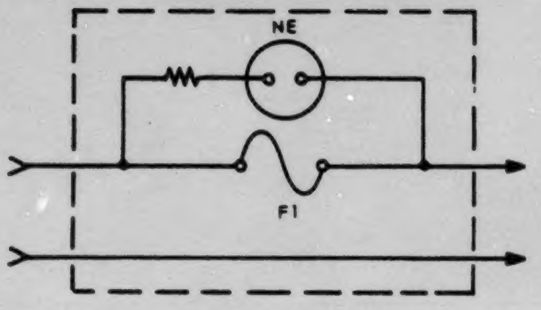


Figure 16. Fuse and neon circuit.

data processors and ancillary equipment. Compare these types with ones used in your system. Compare the holders in your equipment with the ones shown in the table. Prove that fuses in your system are installed where this text states, that symbols are drawn as shown in figure 15, and that fuses are labeled as indicated in this text by analyzing your system and technical orders for this data.

3-42. Fuse holders can become damaged and require replacement. The most common causes of damage are heat and mechanical abuse. If holders are corroded, dirty, or loosely hold the fuse, they will heat. The heat, in turn, can damage the insulating material in the holder. The heating condition will get worse with time, and the holder will have to be replaced.

3-43. By observation of the fuse holders shown in the table, it is easy to see that only two connectors will usually have to be unsoldered and resoldered when replacing a fuse holder. The tasks of replacing a fuse holder and the replacement of the lamp socket are so nearly alike that a restatement of the typical steps will apply to almost all work done on fuse holder replacement:

(1) Mark the wires to be removed.

(2) Remove power before starting any repair action.

(3) Exercise care in removing the unit.

(4) Employ proper soldering techniques in all cases.

(5) Make a static check with a VOM for continuity prior to applying power.

(6) Insert a new fuse of the proper voltage and amperage ratings, and size and type.

(7) Apply power and make a dynamic check.

3-44. The analysis of fuses and their holders has shown that the task of fuse holder replacement is simple and basic and that it parallels the techniques used in replacement of lamp sockets. Analysis has also shown that various types of fuses exist for specific purposes. Further, the fuse wire is designed to carry or handle a specific maximum voltage and current source. Exceeding these values causes the filament to melt, protecting the circuit. Also, analysis pointed out what effect a short circuit in the equipment must have on the circuit fuse. Interpretation of these facts makes it paramount that exact replacement of fuses with both proper voltage and current ratings be installed and exact types, such as fast blow or slow blow, be reinstalled.

3-45. *Switches.* The final subject to be studied in this area of maintenance is the switch. We have been using switches all of our lives. We turn on lights, appliances, and entertainment devices with them. We know that power is applied to these devices when the switch is turned on and power is removed when the switch is turned off.

3-46. In data processors the same types of switches are used for power on and off. Switches are designed for many other uses. Two broad uses of switches are (1) *digital input* and (2) *command input* devices. A switch designed to provide a *digital input* will provide the input source for either a static level logic 1 or a dynamic level 1, or a pulse train. It may even provide the source for an octal input. A switch designed to provide a *command input* will provide preset, reset, advance, repeat cycle, and other short-duration machine command signals. Analysis will also show how these switches are used and what types of switches are usually associated with these actions.

3-47. This analysis of identification of switches, their uses, and their defects also includes descriptions of their reference symbols, schematic symbols, coil operations, lamp circuits associated with these, and external circuits commonly employing switches. Since defects in switches are common to almost all types of switches, the analysis of repair or replacement of the switches is explained as a common element instead of individually. Removal and replacement techniques are related the characteristics of lamp and fuse replacement procedures.

3-48. Types of switches and their related applications. The following paragraphs explain the types of switches and their applications.

3-49. The most common switch known is the *toggle* switch. Refer to table 3 (1) (in the workbook) for a pictorial description of this switch type. This switch may be designed as a single-pole, single-throw (SPST) having two fixed conditions, ON and OFF, or it may be spring loaded as in the case of a reset switch

17

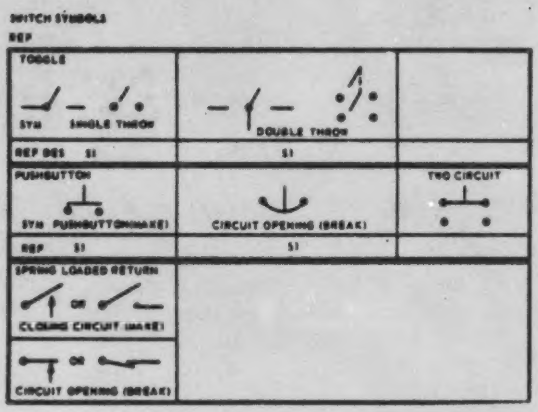

SWITCH SYMBOLS
REF
TOGGLE
SYM SINGLE THROW
DOUBLE THROW
REF DES S1
S1
PUSHBUTTON
SYM PUSHBUTTON(MAKE)
CIRCUIT OPENING (BREAK)
TWO CIRCUIT
REF S1
S1
SPRING LOADED RETURN
OR
CLOSING CIRCUIT (MAKE)
OR
CIRCUIT OPENING (BREAK)

Figure 17. Switch symbols.

where it can be turned on and will spring back to OFF when released. The spring-loaded version is usually found in *command* or *control* circuitry. This is where a *reset* pulse must be used, or a *clear* pulse is needed, or a *preset* pulse is needed. In any use listed, a relatively short-duration pulse is required and the spring-loaded toggle switch is effective.

3-50. Another switch which is used for the same purpose is the *spring-loaded pushbutton microswitch.* Its description (see table 3(2)) is different, but its function is exactly the same as the spring-loaded toggle switch. The schematic symbol and reference designation for both types of switches are shown in figure 17.

3-51. Another type of switch commonly found in data processors and display consoles is the *pushbutton switch with a lamp indicator* under the pushing surface (see table 3 (3)). This type of switch comes in two types, the nonholding or spring release return and the holding type. The holding type employs a holding coil which latches the switch in the ON position when depressed. The second pressing of the switch releases the voltage from the holding coil and returns the switch to its OFF condition. In some applications the holding coil voltage may be removed by another switch remote from the original switch.

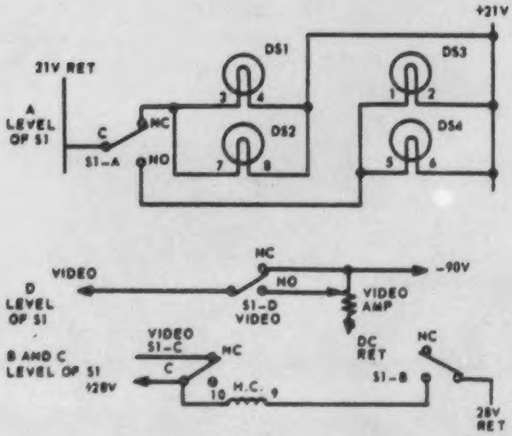

+21V
21V RET
DS1
DS3
A
LEVEL
OF S1
C
NC
S1-A
NO
3
4
1
2
DS2
DS4
7
8
5
6
NC
VIDEO
-90V
D
LEVEL
OF S1
NO
S1-D
VIDEO
VIDEO
AMP
VIDEO
S1-C
B AND C
LEVEL OF S1
+28V
C
NC
10
H.C.
9
DC
RET
NC
S1-B
28V
RET

Figure 18. Switch (with holding coil) circuit.

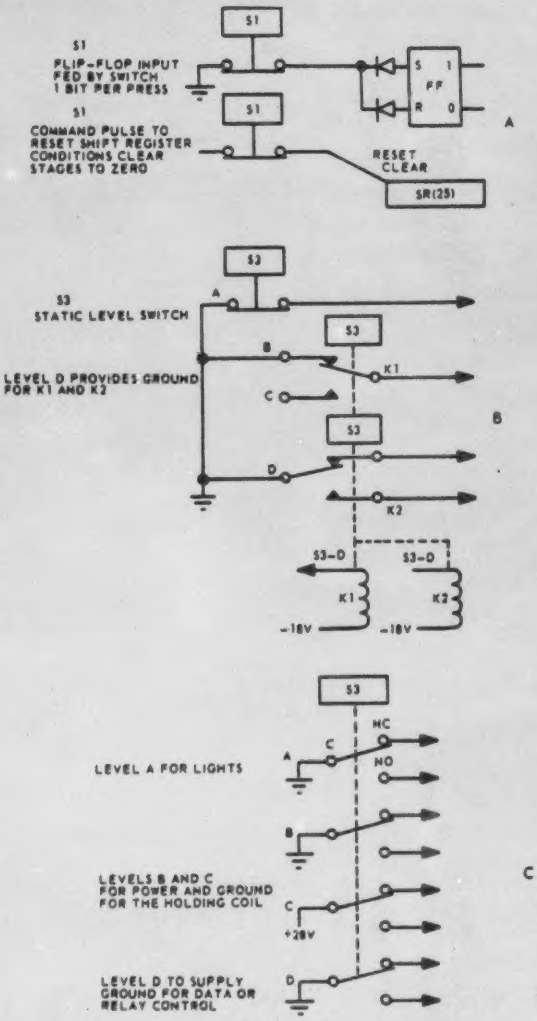

S1
S1
FLIP-FLOP INPUT
FED BY SWITCH
1 BIT PER PRESS
S
1
FF
R
0
S1
S1
COMMAND PULSE TO
RESET SHIFT REGISTER
CONDITIONS CLEAR
STAGES TO ZERO
RESET
CLEAR
SR(25)
A
S3
S3
STATIC LEVEL SWITCH
A
S3
B
K1
LEVEL D PROVIDES GROUND
FOR K1 AND K2
C
S3
B
D
K2
S3-D
S3-D
K1
K2
-18V
-18V
S3
NC
C
LEVEL A FOR LIGHTS
A
NO
B
LEVELS B AND C
FOR POWER AND GROUND
FOR THE HOLDING COIL
C
+28V
C
LEVEL D TO SUPPLY
GROUND FOR DATA OR
RELAY CONTROL
D

Figure 19. Pushbutton switch circuit.

3-52. In both these types of switches, the holding and nonholding, lamp circuits are employed to identify the condition of the switch ON or OFF. Observe the schematic in figure 18 and analyze how two of the lights (DS1 and DS2) are lighted when the switch is off and how two different lights (DS3 and DS4) are lighted when the switch is on. Trace the paths for current flow to prove this analysis. Also observe how the holding coil shown in the schematic is energized and

27

deenergized as a result of the switch action. Trace its current path. Always remember that all circuits function only when the path for current flow is complete.

3-53. The type of switch in figure 19 is usually used in digital units. It may be used (as shown in A) to enter a static level 1 to a register or counter each time it is depressed, or it may be connected as shown in B and C to relays to provide a pulse train in either binary, binary coded decimal, grey code, octal, or a special code prepared for a specialized circuit.

3-54. The *microswitch used in mechanical devices* is another switch commonly found in input-output devices (see table 3 (4)). This switch is often placed in a drive unit so that closing its contacts causes a cycle to repeat or stop. The illustration in figure 20 shows that when the switch is depressed by the pivoted arm of the cam,it breaks the cycle and causes a change in operation. These microswitches are spring loaded and, when the pivot arm is removed, the switch is returned to its normal state.

3-55. We have discussed the various switches used in data processors. Now let's identify malfunctions which might be attributed to them, what repair actions are required, and what safety factors must be employed.

3-56. Repairing or replacing defective switches.

- Defects which occur most often are:
  (1) Defective spring.
  (2) Broken contact.
  (3) Burned contact.
  (4) Shorted contacts.
  (5) Charred switch body.
- Signs of defects are:
  (1) Sticking spring-loaded switch.
  (2) No continuity when checked.
  (3) Loose toggle.
  (4) Improper placement of microswitch unit.
  (5) Improper solder connection.
  (6) Nonoperating holding coil.

3-57. Typical replacement procedures. Replacement of switches is similar to replacement of lamp and fuse holders. Since switches may have more than two connections, exact replacement of wires is an absolute must. Some switches, such as the push and lock, with lamp circuits and holding coils have as many as 12 pins. Since these are arranged in rows, they are often designated by A, B, C, D or 1, 2, 3, 4, and each row could have a normally open (NO), common (C), and normally closed (NC) connector. Identification of wires prior to their removal from the

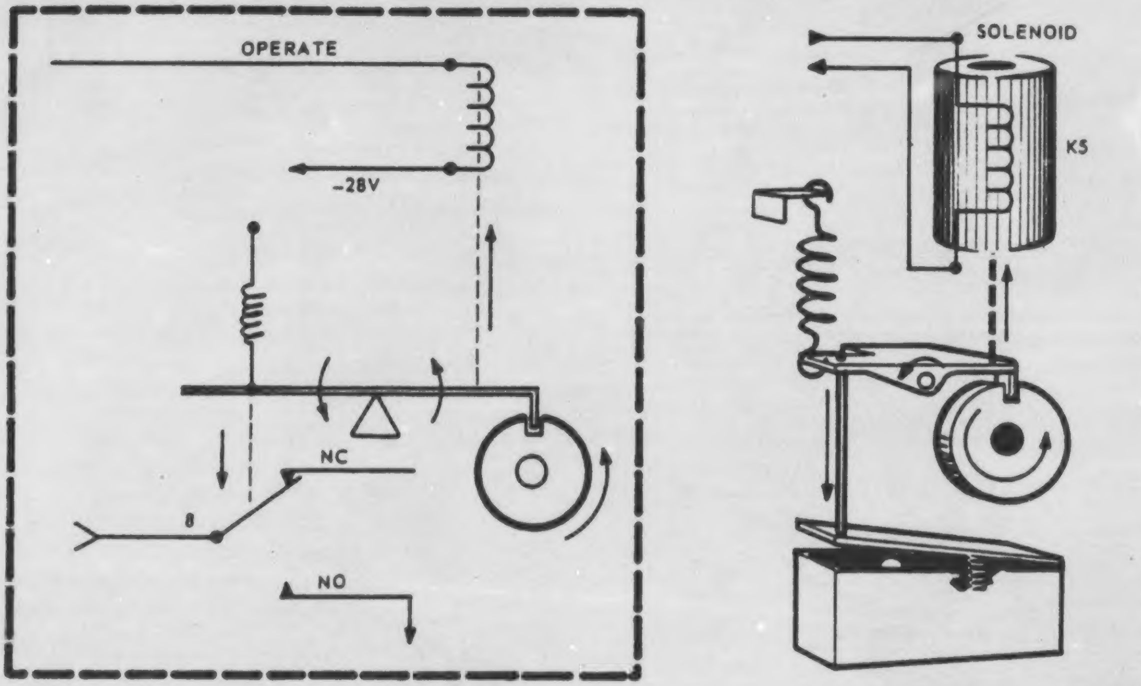


Figure 20. Microswitch operation.

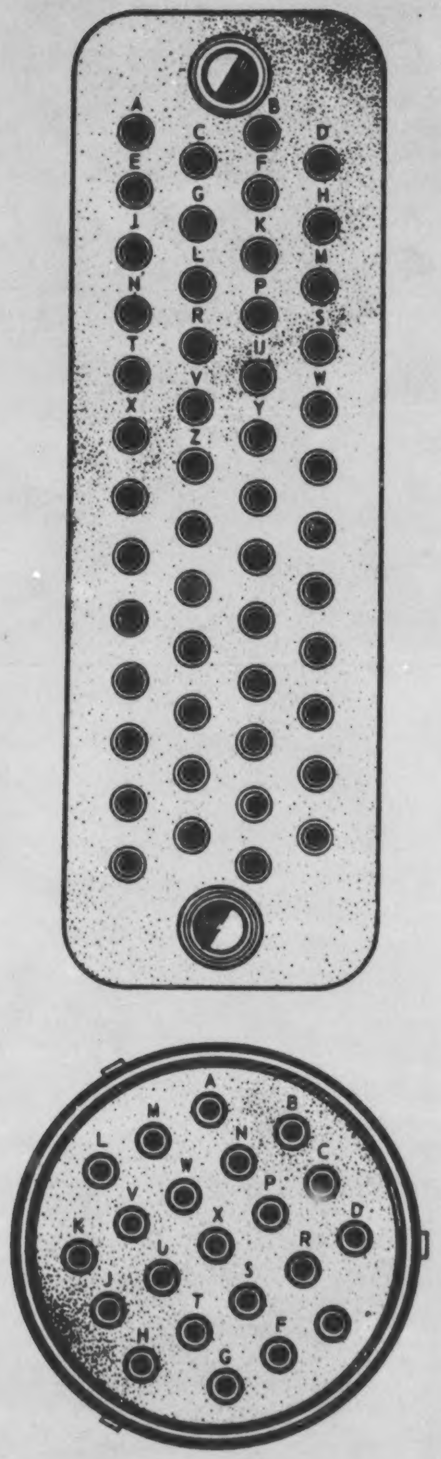


Figure 21. Connectors.

defective unit is a must.

- Remove power to switch (be safe).
- Carefully label all wires for exact replacement.
- Remove wires by using proper unsoldering techniques (if soldered).
- Position and solder new switch to leads.
- Secure switch to cabinet.
- Perform static check with a VOM.
- Perform a dynamic check with power applied to:
  (1) Insure that all lights, if any, work properly.
  (2) Insure that coil holds, or spring releases.
  (3) Insure that switch is positioned properly.
  (4) Insure that mechanical operation is as specified in the technical order.

3-58. **Inspecting and Servicing Electrical and Mechanical Connectors (Jacks, Plugs, Cable Connectors).** The analysis of this task is again in the area of general maintenance. You were working with soldered connections in the case of lights, fuses, and switches. Now you are going to analyze the solderless connector. You will focus on the types of connectors used, tools used when repairing the connectors, typical problems or defects to identify in inspections, symbol designations, and typical repair procedures.

3-59. *Types of connectors.* Figure 21 shows two examples of connectors you will find in your data processing equipment. Either connector, although used in different places in the equipment, will perform the same function; that is, connecting circuits through electrical connections to transfer data or voltages. These two types of connectors are manufactured for as few as one wire connection to as many as 225 wire connections. Each pin in a multiple pin connector is labeled (see illustration). Lettering is usually used in preference to numbers, starting with "a" through "z" and continuing with "aa" through "zz" if necessary, except for the leters "i," "o," and "q," which are never used. There are some equipment areas in which the connector pins are labeled with numerals. Learn how the connectors are labeled in your equipment and where they are. Numbering on the units usually follows general reading rules. For example, the pins are designated "a" and "b" on row 1 across, "c" and "d" on row 2 across, and so on through to the end, or "a," "b," "c," etc., clockwise in circular cable connectors.

3-60. Reference figure 22 to follow the explanation. On these multiple connector bodies, the solderless pins, both male and female, are designed to hold a single wire and are designed to be inserted into a connector body. Each pin has three basic sections: "A"—

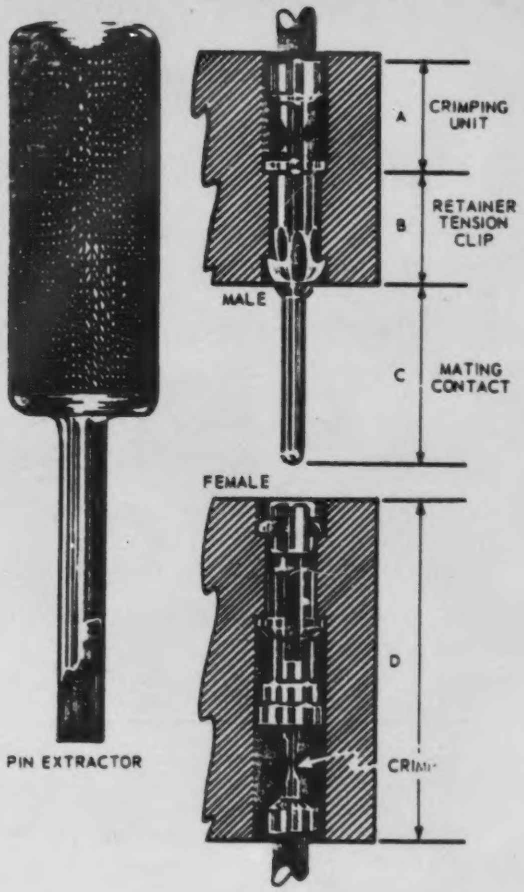


Figure 22. Solderless pin connector unit.

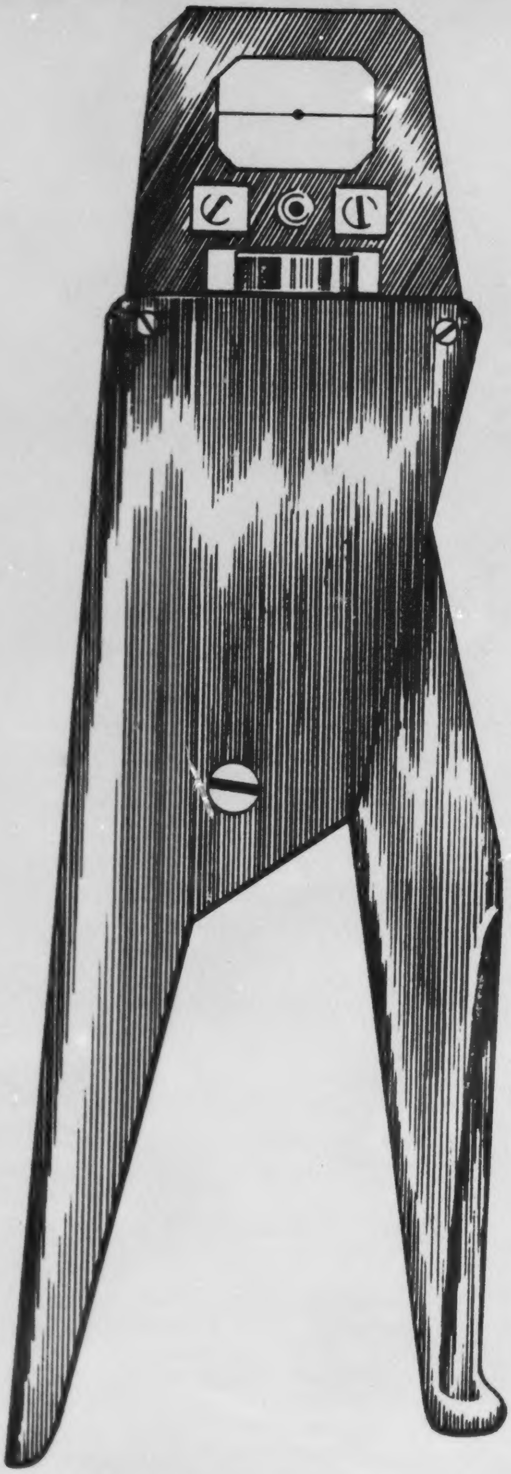


Figure 23. Crimper.

the wire retaining section which is crimped to hold the unit; "B" — the spring tension section which is designed to lock the pin in place in the hole provided in the connector body; and "C" — the male or female mating unit. Looking at "D," the cutaway cross-section of a typical connector body, observe how a ridge is employed to accept the spring tension clip, the "B" portion of the pin. When inserted in the connector body, the pin locks in place. Removal of this pin requires an extraction tool which is designed to slide over the spring tension clip, compress the spring, and allow removal of the pin.

3-61. *Types of crimping tools.* Many companies manufacture crimping tools. However, each crimper is designed to perform the same function—secure a wire to the pin by crimping a portion of the pin around the wire with enough pressure to retain the wire. Crimpers are designed to allow their function to be performed on all sizes of wire and pins. For instance, a crimper used to fasten a pin to

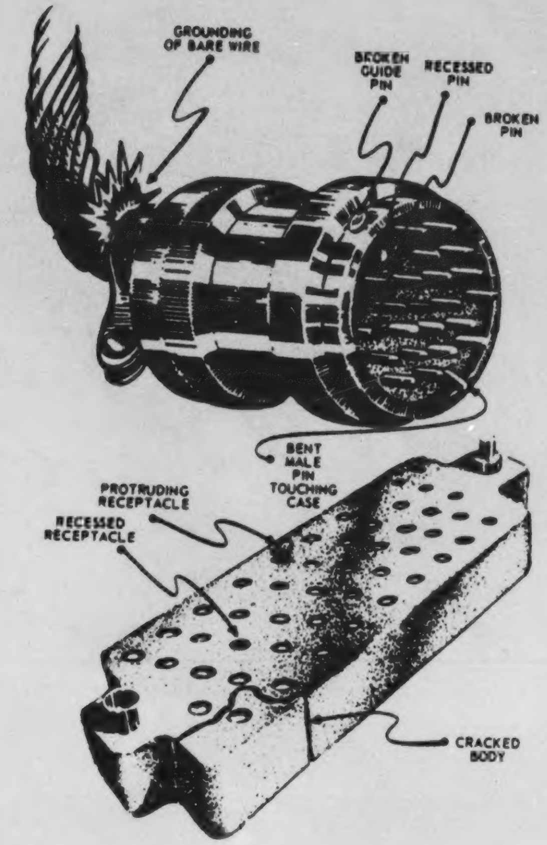


Figure 24. Defective connector.

#22 wire would have a very small opening as shown in figure 23; whereas a size #12 wire would require a crimper with a wider opening to accommodate the larger wire and pin.

3-62. When removing, replacing, or modifying the jacks, plugs, or connectors on your equipment, learn by studying the manufacturer's publication which tool is used for each size wire and pin used in your system.

3-63. *Inspections.* What do you look for when making inspections of jacks, plugs, and cables? In both the metal and the plastic body type connector, certain defects will be visible and you can use them as indicators of trouble spots. Some of the more prevalent connector problems are described below. Refer to figure 24 for the defects listed and study the possible results from these conditions.

(1) A recessed pin. In this case a male or female pin has either slipped back into the connector body because of a broken clip, the lack of spring tension on the clip, or a broken plastic recess catch. It will not mate properly with the male or female connector, and intermittent electrical connection occurs. Heat at the point of contact between the male and female connections can result, causing burning and often melting of the plastic body used to hold the pins.

(2) Loose-fitting pins. This problem occurs when a pin is pushed to one side instead of being properly mated. Again, intermittent electrical connection or shorts may result and heat builds up.

(3) Cracked or broken plastic connectors.

(4) Bare wire contact with the metal casing in metal connectors—especially at the clamp that secures the wires that enter the rear of the connector.

(5) Defective threads or missing guide pins on metal connectors.

3-64. Before analyzing the typical steps involved in removing and replacing jacks, plugs, an replacing jacks, plugs, and cable connectors, let's define the symbology used in the technical data. As outlined in the *USA Standards,* Y32-16-1968, adopted by the Department of Defense, connectors are referenced according to the following rules:

(1) "The movable (less fixed) connector of a mating pair shall be designated "P". . . .

(2) "The stationary (more fixed) connector of a mating pair shall be designated "J" or "X" . . . .

(3) "A connector "P" on a flexible cable shall mate with a fixed connector designated "J" rather than "X."

(4) "If two cables are connected, each of the connectors will be labeled "P."

(5) "A connector to mount an item . . . shall be designated with an "X" prefix if its mate is directly mated (not on flexible cable) to the mounted item . . . ."

3-65. Further explanation of these rules then brings out these factors:

(1) A plug will be designated "P" when attached to a cable or is the less fixed of two connectors. (Refer to rule 1, paragraph 3-64 above.)

(2) Jacks "J" will designate the other unit the plug matches. (Refer to rule 2, paragraph 3-64 above.)

(3) No designation is provided to indicate the male or female portions of mating pairs.

(4) A printed circuit card (PCB) or similar module will not be labeled "P" but will have an equipment location number. The receptacle for the PCB will use the "X" designator before the location number. Example: PCB "A3" goes in location "XA3." (Refer to rule 5, paragraph 3-64 above.)

3-66. *Typical removal and replacement of multiple connectors.* One very helpful feature in the manufacture of multiple lead cables is that the cable strands are twist paired and color coded. This feature is invaluable in troubleshooting and marking.

(1) Carefully mark each wire position and color code prior to starting any repair action. This may be done by using a piece of masking tape on each wire and labeling each wire with its location letter or number designation on the connector. Another method is to prepare a chart with a layout of each pin as seen on the connector and write the wire color code adjacent to the pin hole number.

(2) Remove power before proceeding with any work (be safe).

(3) Disconnect connector from panel (if applicable).

(4) Use pin extractor to release pins.

(5) Insert pins in new connector if all pins are in good condition.

(6) Replace any defective pin.

(7) Examine workmanship for properly seated pins, no cracks, and no frayed or loose wiring.

(8) Secure connector to frame (if applicable).

(9) Secure mating unit to repaired or replaced connector and carefully match guide pin.

(10) Apply power and make dynamic checks where applicable.

3-67. Inspecting and servicing of connectors is a task which requires a careful, conscientious effort by you. Your attention must focus on the elements listed in this text and peculiar factors of your equipment that may be trouble spots. You must select a definite method of identification of wires before removing them from the connector to be changed, and you must insure 100 percent accuracy and quality when reinstalling the pins. Further, you must use the correct crimping tool for the size wire and pin when replacement of pins is required. You must be able to recognize deficiencies and relate them to possible trouble symptoms. Finally you must design a method (procedure) to repair or replace the defective components.

4. Repairing or Replacing Defective Components

4-1. All commands within the Air Force prefer to have maximum availability of all equipment component spares and units on hand at all times and in serviceable condition. This trend has resulted in a philosophy of maximum on-site repair of electronic equipment and a minimum of depot overhaul. Naturally, the maintenance man will have the work to perform, but with the proper training and acquisition of skills, the task is relatively simple. This section shows how basic the task is and how the common maintenance techniques apply to a great variety of the task applications. As you study this text and are given more responsibilities in your work area, you will attain the skill necessary to maintain the equipment. This discussion:

(1) Recaps component replacement and testing techniques previously developed in this text.

(2) Identifies where technical data can be obtained for the repair, replacement, and checkout of components.

(3) Develops the knowledge needed and lists the tools to be used for soldering and desoldering.

(4) Develops typical task lists for repair and replacement of components on PCB, microelectronic assemblies, and modular units.

(5) Identifies special attention areas within typical applications.

4-2. **Replacement Techniques.** In paragraphs 3-13, 1-16, and 3-19 of this chapter, typical replacement techniques were identified. These techniques are common for replacement of electronic and mechanical components, including items like switches, light sockets, fuse holders, motors, fans, gears, moving cams, and belt-driven units, and the dismantling and reinstallation of fixed subassemblies and assemblies. Also identified were two types of testing which must be accomplished with a repair action. These are *static* and *dynamic*. The static is generally accomplished with visual inspections and continuity checks. The dynamic is usually performed with power applied using a standard performance check such as PMI or standards described in Chapter 5 of the -2 TO. To help you recall the techniques previously listed, study the list below.

(1) Remove power (be safe).

(2) Label any and all wires to be removed.

(3) Disconnect any jacks or plugs which may be used on the assembly to be repaired.

(4) Unsolder any wires as required.

(5) Remove any assembly or subassembly to facilitate access to the defective unit as required.

(6) Follow prescribed directions as outlined in TOs or contractor manuals for removal repair, and reinstallation.

(7) Remove assembly or component and replace with a serviceable assembly or component.

(8) Reinstall all wires, jacks, and accessories.

(9) Make a static check.

(10) Apply power and make dynamic checks, insuring that specifications as stated are measured.

4-3. *Technical Orders.* By this time in the study of general maintenance, it is becoming evident that technical orders are prepared under a common grouping of series, except where sectioning of a TO is used. In the task of repairing or replacing components, certain chapters of TOs are listed again because they provide the information necessary to maintain the equipment. These include the service manual, commercial publications, illustrated parts breakdown, and TO 00-25-234.

4-4. *Chapter 5 of service manual -2 TO.* "Maintenance" is the title. Subjects included in the TO which are related to the task of removal and replacement are (1) disassembly, repair and replacement including general parts replacement, (2) reassembly and testing, and (3) performance tests.

4-5. *Commercial publications.* Certain equipment purchased by the Air Force has no AF technical orders published because contractor manuals already prepared are of a high quality and are available. These publications are purchased to allow maintenance to be performed. Within these publications, certain chapters or sections provide repair and replacement procedures and testing procedures. If you have equipment which uses commercial publications for providing this information, study the publication and relate those sections of it to Chapter 5 of the AF technical orders. An example is the IBM Selectric keyboard used in SACCS, 465L system.

4-6. *Illustrated parts breakdown.* The -4 TO is the illustrated parts breakdown (IPB). This technical order provides (1) a pictorial view of the component you may have to repair or replace; (2) a part number for ordering the replacement needed; and (3) a category listing telling you if the part is recoverable, may be thrown away, or must be locally manufactured. We are not going to include the use of the IPB in this discussion but you should know that the IPB is needed for identifying the part.

4-7. *00-25-234, General Shop Practices.* This TO was published to provide Air Force personnel with general shop practices; however, it also provides information on soldering repair actions. The data in the TO pertaining to soldering parallels reference materials prepared by the National Aeronautics and Space Administration (NASA) publications, NPC 220-4, NPC 200-4A, and NPC 275-1. You will probably never be certified to NASA standards for soldering; however, you can become a skilled technician equal to anyone who has been certified.

4-8. Soldering and Desoldering. This study of soldering and desoldering contains explanations of (1) terms used in soldering, (2) tools used in soldering, (3) the nature of solder, (4) good and bad solder joints and examination listings, (5) desoldering, (6) preparation, (7) soldering, and (8) special applications when using microelectronic circuits. Because of its length and complexity and because of its limited coverage in technical school, this subject may seem overdeveloped; but if, during the study of this material, you consider the importance and relative impact it may have upon your system, you will agree that you can't learn too much about so vital an area.

4-9. Terms. The following is a list of terms, together with their definitions, that you will need to know:

TERM	*DEFINITION*
ACID	A substance that gives hydrogen ion in solution or which neutralizes bases yielding water, e.g., hydrochloric acid.
ADHESION	Force of attraction between the molecules (or atoms) of two different phases, such as liquid brazing filler metal and solid copper or plated metal and basic metal. Contrast with cohesion.
ALLOY	A substance having metallic properties and being composed of two or more chemical elements of which at least one is an elemental metal.
BIFURCATED (SPLIT) TERMINAL	A terminal containing a slot or split in which wires or leads are placed before soldering.
BLIND JOINT	Concealed or covered joint.
BOND	The junction of joined parts. Where solder is used, it is the junction of the solder and the heat-affected base metal.
BRAID	A machine-woven covering applied over wire. Usually made of textile yarn or fine metallic wires.
BREAKOUT	The point where a wire or group of wires emerges from a cable or laced portion of a wire harness assembly.
BRIGHT DIP	A solution which produces, through chemical action, a bright surface on an immersed metal.

TERM	*DEFINITION*
CHEMICAL CLEANING	Removal, by chemical means, of foreign material or oxide film which would interfere with soldering.
COHESION	Force of attraction between the molecules (or atoms) within a single phase. Contrast with adhesion.
COLD JOINTS	A type of joint that is characterized by nonwetting of one or both of the surfaces being joined. Usual causes are surfaces which are not clean and/or insufficient heat.
FILLET	Excess alloy deposited along the edge or edges of a joint forming a built-up area.
FLOW	Movement of molten solder in and around a joint.
FLOW POINT	That point at which an alloy is completely liquid.
FLUX	In brazing and soldering, a material used to prevent the formation of, or to dissolve and facilitate removal of, oxides and other undesirable substances.
FLUX CONSISTENCY	The degree to which the flux is liquid.
FLUX RESIDUE	Residue left on joint after soldering is completed.
FRACTURE	Irregular surface produced when a metal is ruptured or broken.
FRACTURED JOINTS	Fractured or disturbed joints that are usually caused by movement, relative to each other, of one or both of the surfaces being joined before the solder has completely solidified. This defect may be characterized by strain marks on the surface, by small cracks in the solder, or by a rough, gritty appearance. A lack of electrical continuity may result from this defect, as well as decreased structural strength or loss of a hermetic seal in nonelectrical applications.
HEAT DISTORTION	Deformation of a material caused by the application of heat. Heat distortion temperature is the maximum temperature that a material will withstand without deformation.
HEAT SINK	A device used to absorb or transfer heat away from heat-sensitive parts.
IMPURITIES	Elements or compounds whose presence in a material is undesired.
INSUFFICIENT SOLDER	A defect that is readily identified by the lack of enough solder to properly wet and bond the surfaces being joined. The resulting joints are very weak and highly susceptible to vibration failures.
INSULATING MATERIAL	Material that is any composition primarily adapted for preventing the transfer of electricity, the useful properties of which depend on its chemical composition, or atomic arrangement.
INTERGRANULAR PENETRATION	Process by which solder, by diffusion, penetrates into grain boundaries of parent metal.
IRON SOLDERING	Soldering by means of an iron bit, which heats the surface, stores molten solder, conveys it, and withdraws surplus.
JOINT CLEARANCE	Dimensions between interfaces of the soldered joint.
LAND (or BOSS, PAD, TERMINAL POINT, BLIVET, TAB, SPOT, DONUT)	The conductive area to which components or separate circuits are attached, usually surrounding a hole through the conductive pattern and the base material.
LUG	A metal device that is either soldered or crimped onto a conductor and used for making a termination.
MALLEABILITY	The ability of a material to accept deformation under pressure; i.e., coining.
MELT POINT	The point at which an alloy starts to melt.
MELTING POINT	The temperature at which a pure metal or a compound changes from solid to liquid; the temperature at which the liquid and the solid are in equilibrium (eutectic).
METAL	An opaque lustrous elemental chemical substance that is a good conductor of heat and electricity.
MODULE (ELECTRONIC)	A group of electronic parts whose leads are joined by welding, soldering, or other method to form an assembly which is subsequently embedded, encapsulated, and/or placed in a shell, and has fixed external dimensions.
OVERHEATING	Heating a metal or alloy to such a high temperature that its properties are impaired. When the original properties cannot be restored by further heat treating, by mechanical working, or by a combination of working and heat treating, the overheating is known as burning.
OXIDE	A substance resulting from the combination of metal and oxygen which, though most prevalent on the surface of the metal, is also capable of penetrating the subsurface of the metal. This substance forms at room temperature and its development is greatly accelerated at elevated temperatures.
PASTY RANGE	Region between the solidus and liquidus temperatures.

TERM	*DEFINITION*
POT	1. A vessel for holding molten metal. 2. To embed a component or assembly in a liquid resin using a case, shell, or other container which remains as an integral part of the product after the resin is cured.
PRINTED CIRCUIT	A pattern comprising component parts, wiring, or a combination thereof, all formed in a predetermined design on a common insulating base. Usually the pattern is formed by etching away unwanted material or by depositing the conducting material.
PRINTED CIRCUIT BOARD (or PRINTED WIRING BOARD)	A conductive pattern reproduced on an insulating base material.
PRINTED COMPONENT	An inseparable part of a printed circuit board, intended primarily to provide an electrical and/or magnetic function, other than forming an electrical connection between two locations.
PULL STRENGTH	The amount of force (in pounds) necessary to break a piece of material when loaded or pulled in a straight line at a constant rate. Rate of pull is in inches per minute.
RESIST	A material such as ink, paint, metallic plating, etc., used to protect the desired portions of the printed conductive pattern from the action of the etchant, solder, or plating.
ROSIN CORE SOLDER	Wire solder containing a rosin flux.
ROSIN JOINTS	A defect identified by flux trapped in the solder joint. The entrapment is usually due to insufficient heat or insufficient time at soldering temperature, or both. The flux, under the conditions noted, cannot boil off the surfaces it is protecting and rise to the surface of the solder. The results of this defect are usually insufficient bonding and high electrical resistance.
SEMICONDUCTOR	A material whose conductive ability lies between that of a conductor, e.g., copper and an insulator, e.g., glass. The most common semiconductor materials used in such solid-state devices as transistors, rectifiers, and diodes are silicon and germanium.
SERVICE LOOP	A service loop is a small portion of wire cable which is added to the overall length to facilitate maintenance and servicing. Generally, the lead is long enough to provide for one servicing in the field.
SHEAR AREA or DEPTH OF SHEAR	The distance that two parallel surfaces are overlapped.
SHIELDED CABLE	One or more insulated conductors covered with a metallic outer conductor to minimize the effects of external electrical fields on signals passing along the conductors.
SOLDERING	Similar to brazing, with the filler metal having a melting temperature range below an arbitrary value, generally 800° F. Soft solders are usually tin-lead alloys.
SOLIDUS	In a constitution of equilibrium diagram, the locus of points representing the temperatures at which various compositions finish freezing on cooling or begin to melt on heating.
SOLUBILITY	The amount of solute present in a given amount of solvent or solution.
SOLUTION	A homogeneous mixture, the proportion of whose constituents may vary within certain limits. Solutions may be either liquid, solid, or gaseous.
SOLVENT	The component of either a liquid or solid solution that is present to a greater or major extent; the component that dissolves the solute.
STANDOFF	A terminal insulated from and usually mounted on the chassis for the purpose of bringing two or more wires of similar electrical characteristics to a common point.
STEP SOLDERING	The technique of making a series of soldered joints in sequence. The first joint is made with a solder operating at the highest temperature. Each succeeding joint is made with a solder at such lower temperatures as will not impair the first joint.
STRAIN RELIEF or STRESS LOOP	The forming of component leads in a designated pattern to provide relief from stress between terminations.
SURFACE TENSION	That property, due to molecular forces, that causes liquid to pull away or ball up when applied to a surface. This condition is most prevalent on a very smooth surface or a surface covered with an oily film.
TERMINAL	A tie point device used for making electrical connections. Five basic styles of terminals are: bifurcated, hook, perforated or pierced, solder cup, and turret.
TERMINAL LUG	A cylindrical piece of metal, either solid or hollow, of two or more diameters which can be staked, flared, swaged, or pressed into a hole for the purpose of connecting leads or external wires to the conductive pattern of a printed circuit board.

TERM	DEFINITION
THERMAL CONDUCTIVITY	The property of a material which describes the rate at which heat will be conducted through a unit area of material for a given driving force. It is dependent on the material or upon its temperature.
THRU HOLE CONNECTION (or FEED THRU CONNECTION, PLATED THRU HOLE)	A conductive material used to make electrical and mechanical connection from the conductive pattern on one side, to the conductive pattern on the opposite side of a printed circuit board.
TINNING	Coating metal with a very thin layer of molten filler metal.
TRANSISTOR	A semiconductor device with three or more electrodes commonly used to amplify or switch electric current.
WETTING ACTION	The ability of one metal or alloy, when molten, to flow over or coat another metal or alloy.
WETTING AGENT	A surface active agent that produces wetting by decreasing the cohesion within the liquid.
WICKING	A condition resulting from solder running too far back on a stripped wire and even under the insulation.
WIRE SOLDER	Commercially available form of solder, produced in the shape of a wire.
WIRE STRIPPING	The removal of a predetermined portion of insulation without affecting the mechanical or electrical characteristics of the conductor or the remaining insulation.
WIRE WRAP	An electrical connection made between a wire and a terminal which has sharp corners by wrapping several turns of closely spaced solid wire under tension around the terminal. The connection is held together thereafter by residual stresses in the parts.

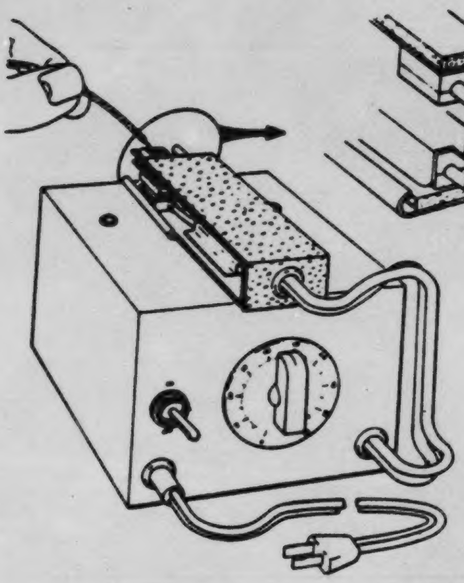


Figure 25. Thermal strippers.

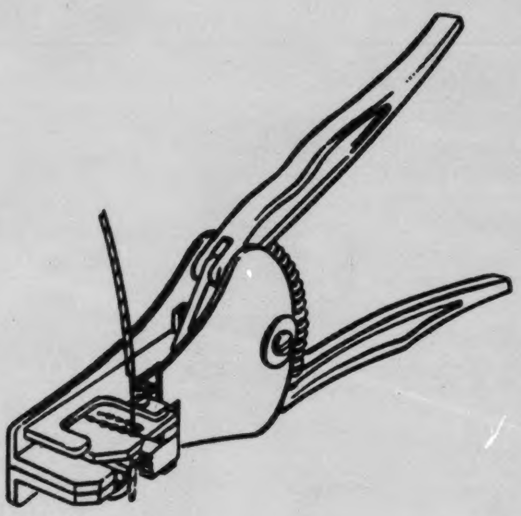


Figure 26. Precision strippers.

4-10. Tools. Tools necessary to perform removal and replacement tasks are listed and described below.

a. Insulation strippers. Thermal strippers, as shown in figure 25, are usually not found in work centers; but if they are used, their operation will be to place the wire to be stripped between the electrodes which will melt the insulation. Heat is applied and controlled by the selection switch. A safety factor must be observed when using this unit, which is an exhaust hood and fan ventilation system used to exhaust toxic fumes, such as polytetrafluoroethylene (teflon) or polyvinylchloride. Another insulation stripper is the precision cutting type, as shown in figure 26. These strippers are designed to accommodate various sizes of wire normally used in electronics. Use the hole provided for the specific size wire to prevent damage to the wire by nicking.

b. Bending tools. Bending tools, as shown in figure 27, are tools which have smooth bending surfaces so that no nicking, ringing,

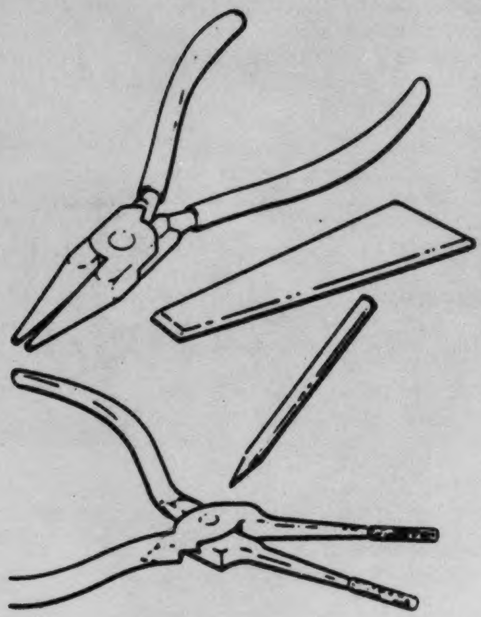


Figure 27. Bending tools.

or other damage to the component can occur. Nonmetallic tools such as a spedger or soldering aid may be used.

c. Soldering irons. Soldering iron size (tip size and shape, voltage and wattage rating) and temperature are selected and controlled according to the work to be performed. Temperature control may be accomplished through the use of a variable power supply, tip selection; or both.

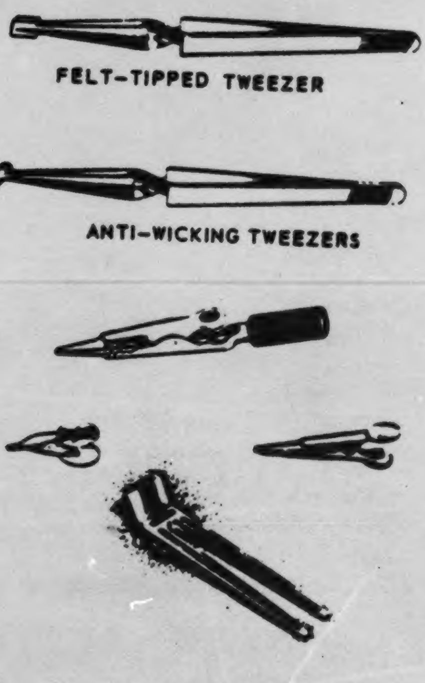


Figure 28. Thermal shunts.

d. Thermal shunts. Thermal shunts, or heat sinks, are used to protect heat-sensitive components such as semiconductors, crystal devices, meter movements, and insulating materials from damage due to heat while soldering. These devices, shown in figure 28, are placed or clamped in place so that they prevent the heat from reaching the component while its leads are being soldered.

e. Tools and materials for cleaning—general. The following are tools and materials of a general nature that relate to the task of removal and replacement:

(1) Braded, shielding tool (refer to fig. 29,A).
(2) Erasures, typewriter (refer to fig. 29,B). This tool can be used effectively for removal of gold plating from solder areas.
(3) Eraser shield.
(4) Alcohol dispenser.
(5) Medium stiff natural or synthetic bristle brush.
(6) Industrial lint-free cleaning tissue.
(7) Soldering iron holder.
(8) Single-cut file.

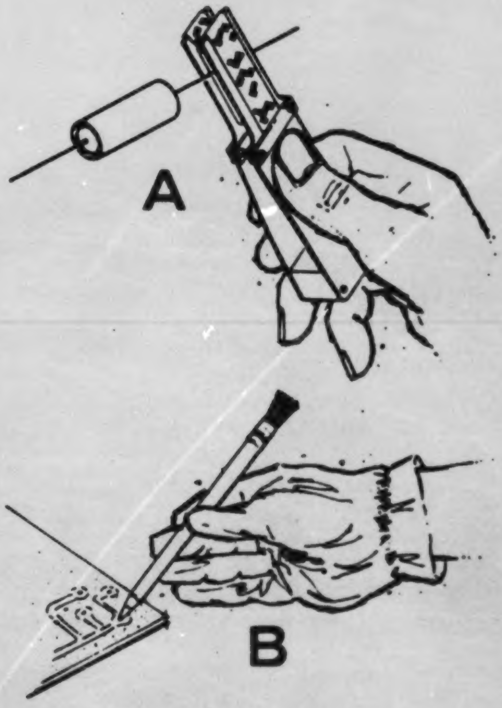


Figure 29. Cleaning tools.

(9) Electrician scissors.
(10) Round-nose pliers (small).
(11) Diagonal pliers (small).
(12) End cutting tweezers.
(13) Small wire brush.
(14) Sponge with holder.
(15) Vice, electrical.
(16) Solder SN60, SN63.
(17) Toe nail clippers.
(18) Antiwicking tweezers, 20, 21, and 22 AWG.

4-11. The Nature of Solder. Any discussion of soldering techniques should begin with an explanation of solder itself. This generally accepted substance is thought to be quite simple in nature, and so it is when proper preparation, materials, and techniques are employed.

4-12. Ordinary soft solder is a fusible alloy consisting essentially of tin and lead and used for the purpose of joining together two or more metals at temperatures below their melting point. In addition to tin and lead, soft solders occasionally contain varying amounts of antimony, bismuth, cadmium, or silver, which are added for the purpose of varying the physical properties of the alloy. However, in many solders, some of these elements are present as impurities. Soft solder secures attachment by virtue of a metal solvent or intermetallic solution action that takes place at a relatively low temperature. The distinction between fusion and solution may be illustrated as follows: Ordinary table salt (sodium chloride) has to be heated to 1488° before it melts. However, when a little water is added, it melts easily without any heat. The action of molten solder on a metal like copper or steel may therefore be compared to the action of water on salt; the solder secures attachment by dissolving a small amount of the copper or steel at temperatures quite below its melting point.

4-13. Since the soldering process involves a metallurgical or metal solvent action between solder and the metal being joined, it is obvious that a solder joint is chemical in character rather than purely physical because the attachment is formed in part by chemical action rather than by mere physical adhesion. The properties of a solder joint are therefore different from those of the original solder because, in the metallurgical process of soldering, the solder is partly converted to a new and different alloy due to a solvent action between the respective metals with the formation of a completely new metallic contact.

4-14. Thus, a soldered connection is contin-

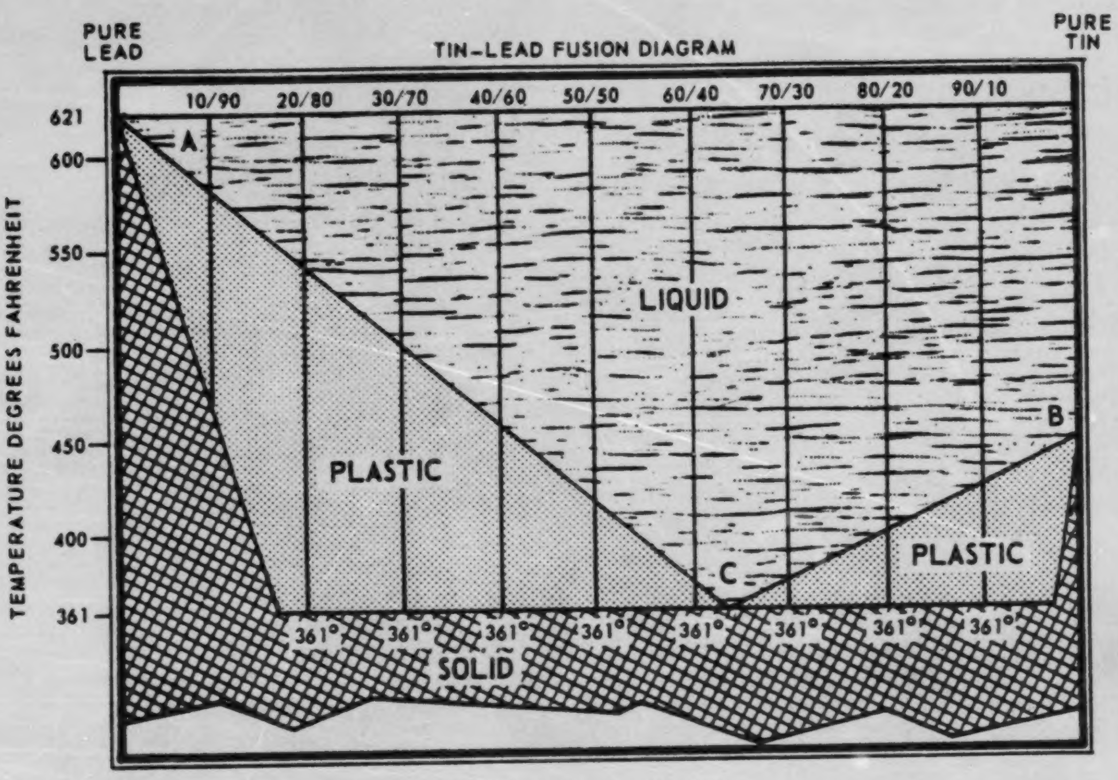
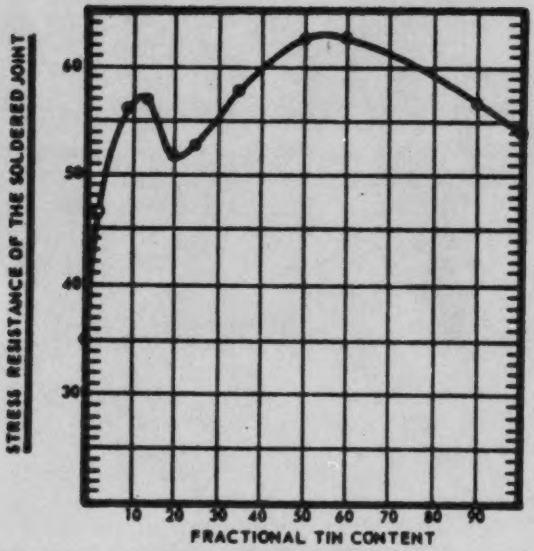


Figure 30. Tin-lead fusion diagram.



Graph showing the change in joining quality of tin-lead solders with increase in tin content, based on resistance of the soldered joint to a simulated bending and torsional stress.

Figure 31. Solder joint quality.

uous in metal continuity while an unsoldered one is discontinuous; when two metals are soldered together, they behave like one solid metal, but when bolted, wired, or otherwise physically attached, there are still two pieces of metal. They are not even in physical contact due to an insulating film of oxide on the surfaces of the metals.

4-15. The permanence as well as the character of the soldered connection is also different. The solder alloy lends itself to stresses and other strains due to temperature change without rupture of the joint, while an unsoldered connection becomes more and more loosened by small differential movement from temperature variations and by the gradual accumulation of an increasingly thick film of nonmetallic oxide barrier on the metal surfaces.

4-16. Soldering also provides a different form of attachment from electroplate in which the metals adhere by physical attachment only. It is important to emphasize that electroplated metals are not successfully soldered by alloying solder to the plating; the metal solvent action must proceed through the thin, physically attached plating to the base metal itself where the alloy action must form. Plating a metal preserves its soldering quality, but does not assist in the soldering itself.

4-17. Since the soldering operation involves the partial creation of a new alloy between the solder and the metal that is soldered, it follows that the physical properties of this new alloy are not necessarily the same as those of the original solder. The tensile strength, shear strength, creep strength, and similar physical properties of a soldered connection, therefore, depend on the extent to which alloy formation has taken place during soldering and are subject to wide variation due to the inherent variables in soldering techniques. It is important to appreciate that the properties of a soldered connection are not necessarily those of the original solder.

4-18. In order to understand fully the alloy or solvent action on molten solder, it is essential to consider the tin-lead fusion diagram, as shown in figure 30.

4-19. From this figure, you can see that when tin is added to lead, which melts at 621° F., it lowers the melting point of lead along the line AC; also, when lead is added to tin, which melts at 450° F., it lowers the melting point of tin along the line BC. At the point C, where these two lines meet, there is an alloy of the lowest melting point of the metals, tin and lead. The alloy at this point, which is known as the eutectic composition, consists of 63 percent tin and 37 percent lead, and has a sharp and distinct melting point of 361° F.

4-20. The characteristic of eutectic solder having no plastic state is very beneficial to the soldering process. (Plastic state—time between changing from a solid to a liquid when heat is applied.) Since it melts at a very low temperature and goes from a solid to a liquid at this point, it is very good for soldering heat-sensitive components or any soldering operation where too much heat could be harmful.

4-21. There are several other alloys which have a eutectic characteristic. However, they also have disadvantages. For instance, a solder of 62.5 percent tin, 36.1 percent lead, and 1.4 percent silver is good but more expensive. Also, 97.5 percent lead and 2.5 percent silver is a good solder; however, this gives a gray dull appearance to the solder joint.

4-22. The advantages of SN63 are further emphasized by figure 31. From the diagram, you can see that the addition of a little tin to lead is reflected in a sharp increase in the quality of the soldered joint which continues until the alloy contains 15 percent tin. Further addition of tin beyond 15 percent lowers the joint quality somewhat, after which it again increases sharply until the solder contains about 60 percent tin. Beyond 60 percent tin, there is again a slight gradual decrease in the overall joint quality of the soldered connection. You can see that the maximum points in the alloy quality curve correspond closely to the critical points in the tin-lead fusion diagram, that it is the lowest usable melting point, and that it has the highest pull strength occurring at nearly the same point.

4-23. Continuing with the analysis of the nature of solder, there is one item which, when present, can destroy solder and its usefulness—dirt or contamination. Every time you make a solder joint, everything including your iron, parts, wire, and solder must be clean. After the joint has been formed it must be cleaned again. The solder joint isn't any better than what you put into it. If at any point in the operation you carry impurities to the joint, it will not be a good joint. You could go even further than that and say that it has no chance of being anything but rejected.

4-24. **Flux.** Flux is a substance used in soldering and is essential to prevent the oxygen in the air from combining with the metals. Without flux, heating a metal causes a combining of the oxygen and the metal, and a film of oxide results. The oxide prevents the solder from fusing with the metal. If, prior to the soldering operation, the metals are thoroughly cleaned and immediately coated with a thin film of flux, oxidation is prevented. Solder then fuses nicely with the surface of the metals. There are two classes of flux—corrosive and noncorrosive. *Zinc chloride, hydrochloric acid*, and *sal ammoniac* are in the corrosive class. Corrosive flux should never be used in electronics repair work, since any flux remaining in the joint, in time, eats through the connection and creates a high-resistance circuit. *Rosin* is a noncorrosive flux, and is available in paste, liquid, or powder forms. All electronics soldering must be done with noncorrosive, nonconductive rosin fluxes conforming to Military Specification MIL-F-14256, Type A, and Federal Specification QQ-S-571, Type RA (refer to table 4 in the workbook for a list of standards which give detailed explanations of all aspects of soldering). Liquid rosin flux should be used only for the following applications:

- Removal of excessive solder from a joint by wicking on a stranded wire.
- Soldering of nickel-plated wire.

When used with flux-cored solder, the liquid flux must be chemically compatible with the solder core flux.

4-25. **Good and Bad Solder Joints.** Figure 32 (in the workbook) shows the difference between good and bad solder joints. Study these illustrations carefully and learn to recognize the faulty joints by comparison with the good. From your study you should have come to these conclusions about good solder joints.

(1) Solder must cover the entire surface of the unit being soldered, but *not* so thick that the unit's shape is indistinguishable.

(2) The solder must be uniformly distributed over the unit and base metal.

(3) No residue such as flux or oxide is left on the surfaces.

(4) No solder reaches the shield of the wire.

This is a fairly short list for a good solder joint, yet it does cover all the important points of inspection necessary to identify a good solder joint. Now study the list which follows and identify the soldering defects you can see in figure 32. Select a defect found in the illustration and write its corresponding letter in the space provided for it on the list. Stay within each group.

GROUP 1

________ Charred insulation
________ Insulation gap too long
________ Broken strand
________ Insufficient solder

GROUP 2

________ Melted insulation
________ Scratches in solder
________ Spilled solder
________ Solder or rosin splattered on surface
________ Insulation gap too short

GROUP 3

________ Lead improperly formed
________ Bird caging
________ No fillet

GROUP 4

________ Fractured joint

GROUP 5

________ Insufficient lead length
________ Bare copper along lead
________ Bare lead length
________ Excessive lead length
________ Lead misplaced

GROUP 6

________ Damaged terminal
________ Foreign material in solder
________ Strands misplaced at cut end
________ Pits in solder
________ Excess solder

GROUP 7

________ Points and/or bumps in solder
________ Solder splattered on component
________ Scraped lead

ANSWERS:

Group 1: A, B, D, C
Group 2: E, H, G, I, F
Group 3: K, J, L
Group 4: Y
Group 5: M, P, O, X, N
Group 6: S, T, R, U, W
Group 7: Z, Q, V

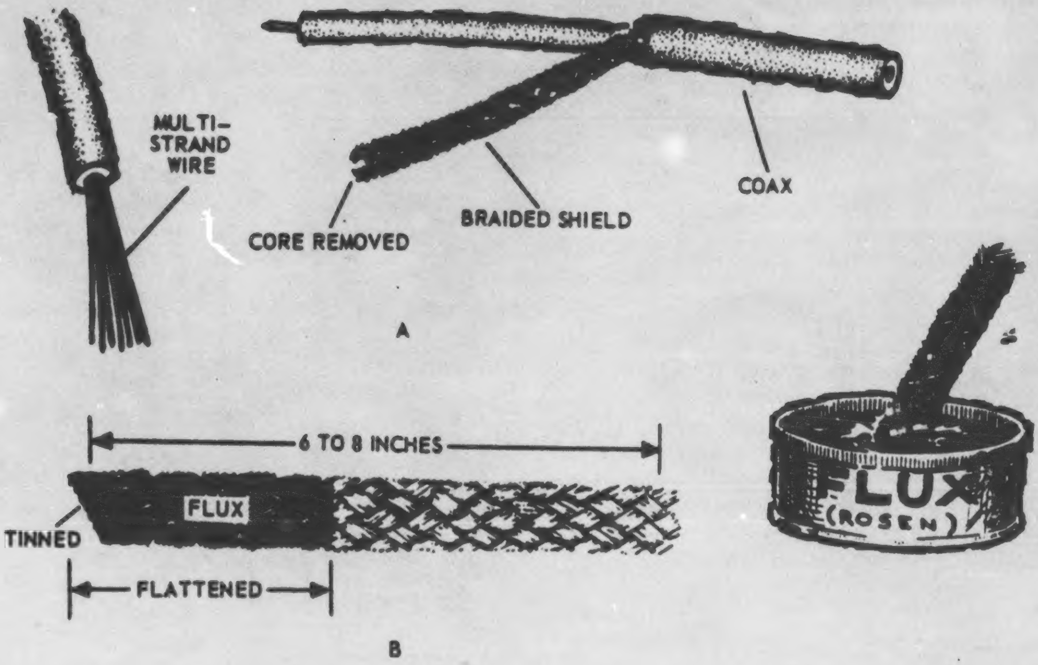

MULTI-
STRAND
WIRE
CORE REMOVED
BRAIDED SHIELD
COAX
A
6 TO 8 INCHES
FLUX
TINNED
FLATTENED
FLUX
(ROSEN)
B

Figure 33. Wicking tools.

4-26. Desoldering. Although there are various techniques which can be used in desoldering, we will explain only the "wicking" and "sniffing" techniques. Each of these techniques is very effective as an aid in the desoldering task. In each process the principle which is employed is that to remove molten solder from a previously soldered joint, some physical force or attraction must be employed. First the principles are examined. Then the steps needed to perform the task are listed.

4-27. *Wicking.* Refer to figure 33,A, and observe where a typical source of wicking material can be obtained. A wicking solder removal unit may consist of a braided shield wire with the core removed, or it may be a piece of wire containing many strands.

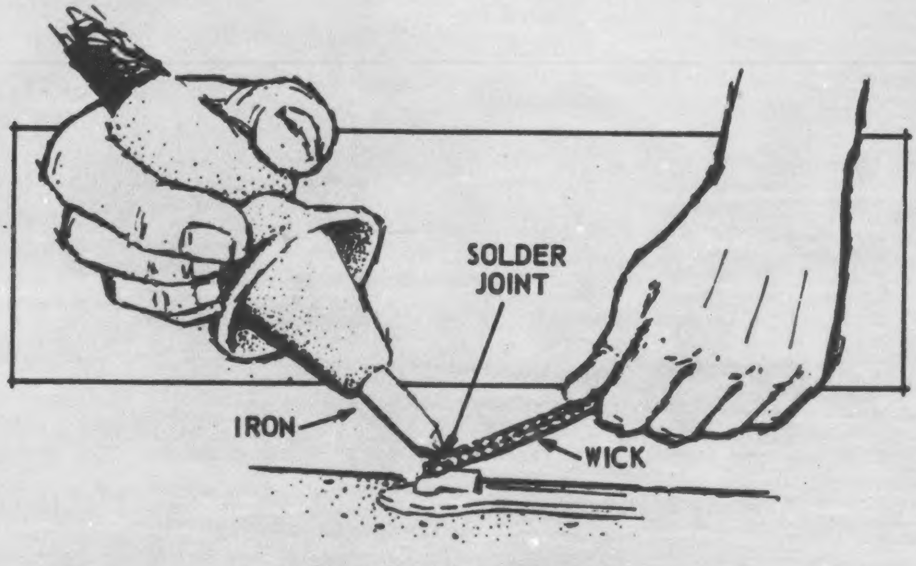

SOLDER
JOINT
IRON
WICK

Figure 34. Wicking application.

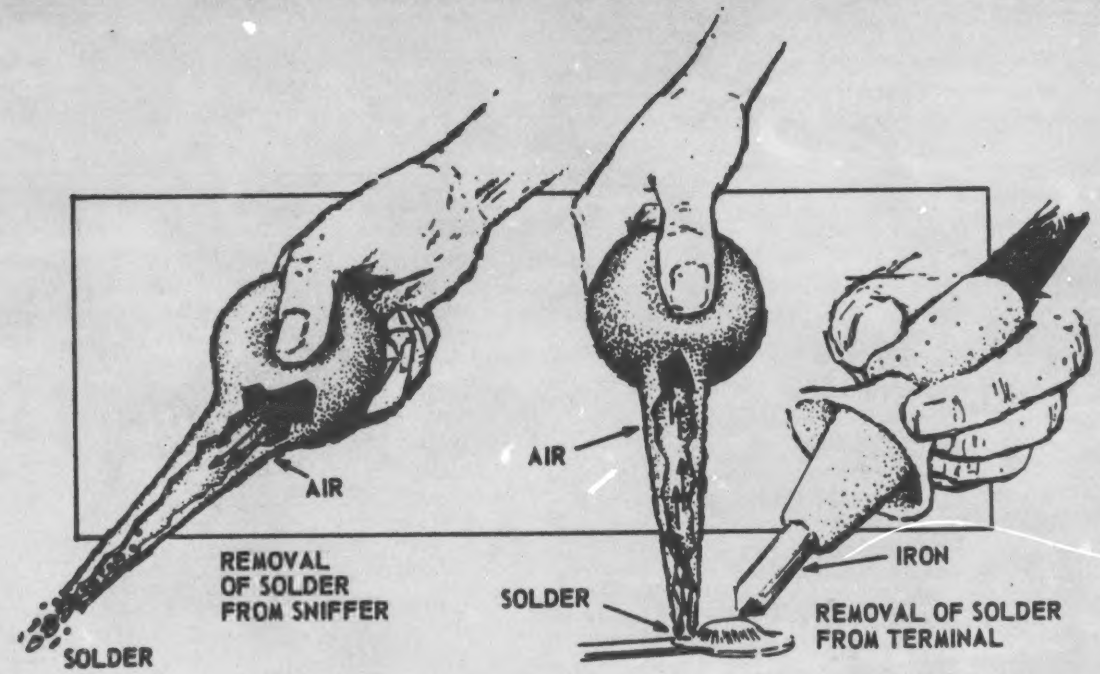


Figure 35. Sniffing application.

4-28. The preparation steps for making an effective wick from these types of materials are as follows and are shown in figure 33,B:

(1) After removing core materials, flatten the shield with a bending tool.

(2) Dip the wick in liquid solder flux of the same type of rosin as was or will be used in repairing operations, to about 2 inches deep.

(3) Tin the end of the wick with solder and a hot iron.

(4) If using a multistrand wire, strip the cover back about 4 inches.

(5) Flatten the wire slightly, keeping the strands uniformly in place.

(6) Dip the wire into liquid rosin.

(7) Tin end of wick.

4-29. The principle of wicking simply explained is that by applying heat to a well-saturated rosin wick, the solder will flow readily into the rosin area, leaving the terminal to which it was previously affixed. It is almost as if by osmosis that the solder travels into the saturated wick.

4-30. When preparing the wicking unit, use a wire size no larger in diameter than the pad size that you will be wicking solder from. This is most important because the wick, if allowed to touch the board, will cause frog-eyeing of the material on the board. Refer to figure 34 for a pictorial application of wicking as listed below.

- Place the wick on top of the solder joint to be removed.
- Place the iron tip on top of the wick. The heat of the iron will melt the solder and the solder will flow into the wick.
- Clip off the wick containing removed solder, and repeat the operation until all solder is removed from the joint.

4-31. *Sniffing.* In this method, a tool fashioned as a syringe is used (refer to fig. 35). This tool is made from a substance which does not form a bond with solder. Its use is not as highly recommended as the wicking method, but it is effective.

4-32. The sniffer or, as sometimes called, "solder sucker," uses the force of air pressure to accomplish the sniffing—removal of solder. This is done as follows:

- Squeeze the air out of the rubber ball at one end of the sniffer.
- While keeping the ball depressed, place the pointed end of the sniffer tube next to the solder to be removed.
- Heat the solder with a solder iron, keeping the tip of the iron in the solder and not on the sniffer.
- Slowly release the pressure on the sniffer ball, allowing air to enter the ball through the ~~sniffer~~ tube. As the air enters, it will pull the molten solder into the tube with it.
- After the solder has been pulled into the sniffer, remove the sniffer from the joint and,

by depressing the ball again, force the collected solder from the sniffer tube.

4-33. Each of these methods is effective for removal of solder from a joint. Caution must always be used because of heat, component reaction to heat, and possible damage to base materials and adjacent components. Prepare the work area and tools properly so that a minimum time of heat application is used when desoldering.

4-34. Preparation. Preparation of both the tools and the surfaces to be soldered must be considered in order to effect a successful preferred solder joint. This discussion includes preparation of the (1) soldering iron, (2) the component leads which are to be soldered, and (3) circuit and pad.

4-35. *Soldering iron tip.* Every time a solder iron is to be used, it must be examined to ascertain its condition for use in the soldering task to be performed. It should be:

- Properly connected or screwed into the holder.
- Clean of oxides.
- Shaped properly for the task it will have to be used on.
- Tinned.

If any one or more of these items is not as it should be, preparation is needed:

- Scale oxides from the tip surface with an abrasive cloth as in the case of *iron* or *plated tips.*
- Form the tip into the proper shape by filing. This must be done on *unplated copper tips* because of pitting, burning, and oxidation to the tip surface.
- Heat iron to the minimum point where solder will melt and coat lightly the entire soldering point.

To maintain a clean tip after the iron has been prepared, prepare a wet sponge, either natural or synthetic, and use it to wipe heated tips to remove dirt, grease, flux, oil, or any foreign matter which could, if present, become part of the solder joint and cause the joint to be classed defective.

4-36. *Component.* Each component, wire, or terminal to be installed in a circuit required physical handling during its manufacture, processing, and shipping. Further handling by you is required to shape its leads properly, cut the leads, etc. After all handling is done:

- Clean the surfaces which must be soldered with the braided cleaning tool.
- Dip the stiff bristle brush in alcohol and brush the surfaces just cleaned.
- Dry with an industrial lint-free rag or paper.

4-37. *Circuit board.* The above list of "do's" for preparation also applies to circuit boards. However, because circuit boards are composed of many substances which can be harmed, the wire braided brush must *not* be used; instead, the white typewriter eraser can be used in its place. This tool is very effective because it can be sharpened to a point and can be controlled. Use it to clean surfaces to be soldered. Remove dirt, contaminants, gold plating, and any other foreign substances from the pad or pads to be soldered; clean with alcohol and brush and then dry.

4-38. *Forming.* Forming leads from components to properly fit the circuit in which they will be installed requires careful consideration and examination. Particular handling must be used in order to have successful application and guaranteed usefulness. Refer to figure 36 (in the workbook) and the steps that follow.

- Bend component leads, using a bending tool in such a manner that the radius of the bend is equal to twice the thickness of the lead wire (refer to fig. 36,A(1)).
- Start the bend no closer than 1/16 inch from the component body (refer to fig. 36, A(1),(2),(3)).
- Center the component between its solder connections unless specifications dictate otherwise (refer to fig. 36,A(2)).
- After insertion into a circuit board, use the bending tool to secure the component by bending the protruding lead 45° (refer to fig. 36,B(1),(2)).
- Cut the lead so that no portion when

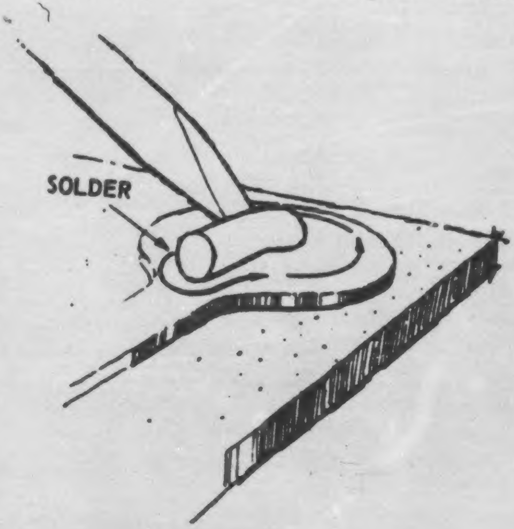


Figure 37. Applying solder.

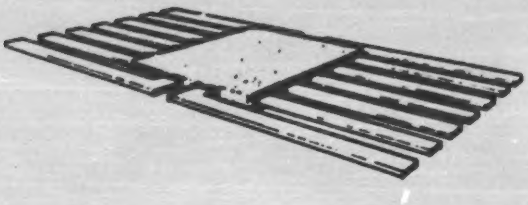


Figure 38. Integrated circuit.

bent flat exceeds the perimeter of the pad (refer to fig. 36,D).

- Press the cut lead firmly against the pad (refer to fig. 36,B(3), D).
- Cut the lead on a turret so that the wrap around the turret will reach 180° past the first point of contact with the turret (refer to fig. 36,C).
- Cut the lead the thickness of an AWG #20 wire on a joint where the lead is not bent.

4-39. In all cases, whether it be leads from components or wires, the forming provides two main functions. These are the (1) securing of the lead to the circuit and (2) providing proper stress relief. This relief is needed to prevent rupture of the component lead from the component itself. In the case of forming a wire, the wire should be able to move slightly without rupture of the turret or terminal, without having stress pull on the solder joint, or without causing rupture of the wire strands.

4-40. The preparation of tools and components is probably the most critical phase in this entire task of removing and replacing components. Its variety of situations and tools makes it extremely important for you to exercise care and observe strict compliance with the rules listed herein. These are not all the rules, but they are the most essential to general applications you will use in your maintenance area. Cleanliness is the watchword.

4-41. Soldering. Each component, wire, or terminal prepared for soldering must have the solder applied in such a manner that:

- The solder will form a bond.
- It will flow readily, providing the complete immersion of all elements of the joint.
- It will cool and solidify into a bright, flake-free surface.
- There will be no obscurity of the shape of the elements in the joint.

4-42. The best way to do this is to place the iron at a 45° angle with the tip touching both or as many elements of the joint as possible, as shown in figure 37, and start the solder flow near the iron. Pass the solder around the joint and end near the iron. Remove the iron, and let the solder (still remaining near where the iron was) flow into that place, completely covering the elements of the joint with solder. This technique is applicable for almost all soldering applications except certain integrated circuits (IC) designed units.

4-43. Soldering of Integrated Circuits (IC). Certain ICs are designed as shown in figure 38. This type of IC does not require any forming and does not protrude through a printed circuit card. It is normally soldered to the component side of the card, as is shown in figure 39. This soldering is accomplished by more than one technique—the electric arc or an electrode supplying current and the method shown in figure 39. You place the iron near the tip of the IC lead and onto the pad. Place solder in the space between the tip of the IC, the iron, and the pad. The heat will allow the solder to flow under the IC tip and

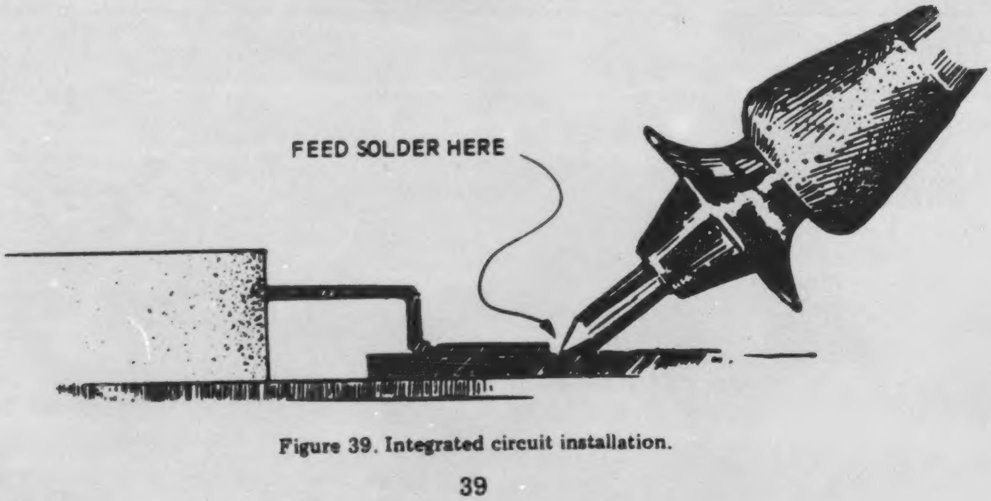


Figure 39. Integrated circuit installation.

lead and form a bond. This technique is called *bridging*.

4-44. **Task Lists for Repair and Replacement.** Let's examine this subject from two viewpoints: first, the general tasks of the preparation and work done prior to desoldering and soldering, and second, the soldering tasks themselves.

4-45. *General Tasks.*

- Observe and record how the component is placed before removing it by observing polarity, placement angle, positioning, insulating requirements, and adjacent heat-sensitive components or substances.
- Label the elements to be removed.
- Remove any assemblies that will facilitate repair.
- Locate replacement procedures in technical orders or manufacturers' manuals.
- Remove power if applicable.
- Prepare work area by removing obstructions, obtaining sufficient light, and obtaining the tools necessary for the job.
- Examine and prepare tools, irons, etc., for the job.

4-46. *Task list for removal of a component.*

- Remove any hermetic sealer from the soldered joint to be worked on with a chemical agent. Refer to instructions in the TO for proper chemical agent. Look for the miliatry or Federal specification listing.
- Clean with isopropyl alcohol.
- Wick solder from joint, using either the wick or sniffer technique.
- Remove element(s) from joint.
- Clean joint.

4-47. *Task list for the replacement of a component.*

- Clean leads of new elements with cleaning tool such as braided tool; use abrasives as applicable.
- Remove insulation if a wire lead.
- Form the strands if multiple.
- Tin to 1/8 inch from insulation.
- Form the element.
- Clean with alcohol.
- Tin elements.
- Place elements in the joint.
- Fasten heat sinks to protect heat-sensitive items.
- Apply solder iron to joint.
- Feed solder into joint, covering all elements to provide a complete sealing. Do not use so much solder that the shape of elements in the joint are indistinguishable
- Remove solder iron and feed solder into space occupied by iron.
- Allow to cool and solidify. Do not disturb.
- Clean with alcohol.
- Apply hermetic sealer if applicable.

4-48. *Checks.* Perform static check before the hermetic seal is applied. (Refer to the technical order for the appropriate sealer.) Perform the check with a VOM by measuring for resistance on the lowest scale. Do this by touching the solder with one VOM lead and the wire or component lead with the other. Any reading except a short reveals a defective joint. After completing the static check on all joints repaired, clean the surfaces again with alcohol, and seal. Perform dynamic checks in accordance with specified standards, or by inserting in an actual circuit in the case of PCB, or apply power in lamp fuse and switch replacement.

4-49. **Special Attention Area.** The subjects in this area are mainly crystal type semiconductors, solid-state devices, and microelectronic, IC components (shown in fig. 40). The discussion consists mainly of identifying the special care needed when installation of a new component is required.

4-50. The primary consideration needed when replacing one of these devices is heat control. Heat will destroy all of these components. Therefore, a heat sink is required while soldering. Excessive heat may melt the internal leads from the component or destroy the solid-state junctions, which the following paragraphs outline.

4-51. Observe how an IC is formed by studying figure 41. See how it is composed of layers or strata of semiconductor material. During the formation of the circuit, each layer is designed to perform a portion of the circuit as a P or an N type material or resistive coupling or bias junction, etc., and from these points, wire of extremely fine AWG thickness is affixed and fed to one of the external connecting wires or leads to which you will solder. If the IC is fairly large and the conductors are side mounted to pass through a PCB, as shown in figure 40, the heat sink may be easily fastened to the component side of the card. The case of a round IC is usually heat sinked when the leads are passed through the PCB and no place for a heat sink is possible on each connector lead. If a flat pack IC is used, a heat sink may be laid close to the body of the IC, and the solder flow from the bridging is effective; no heat damage to the internal connections of the IC will occur. These general rules also apply for crystal units.

36

4-52. Forming of the leads of these components is the same as with other electronic components:

- Start the form no closer than 1/16 inch from the body of the component.
- Center the component between pads.
- Insure that stress reliefs are properly designed.

4-53. If you work on equipment having components like these, then you must—in addition to applying the general informa-

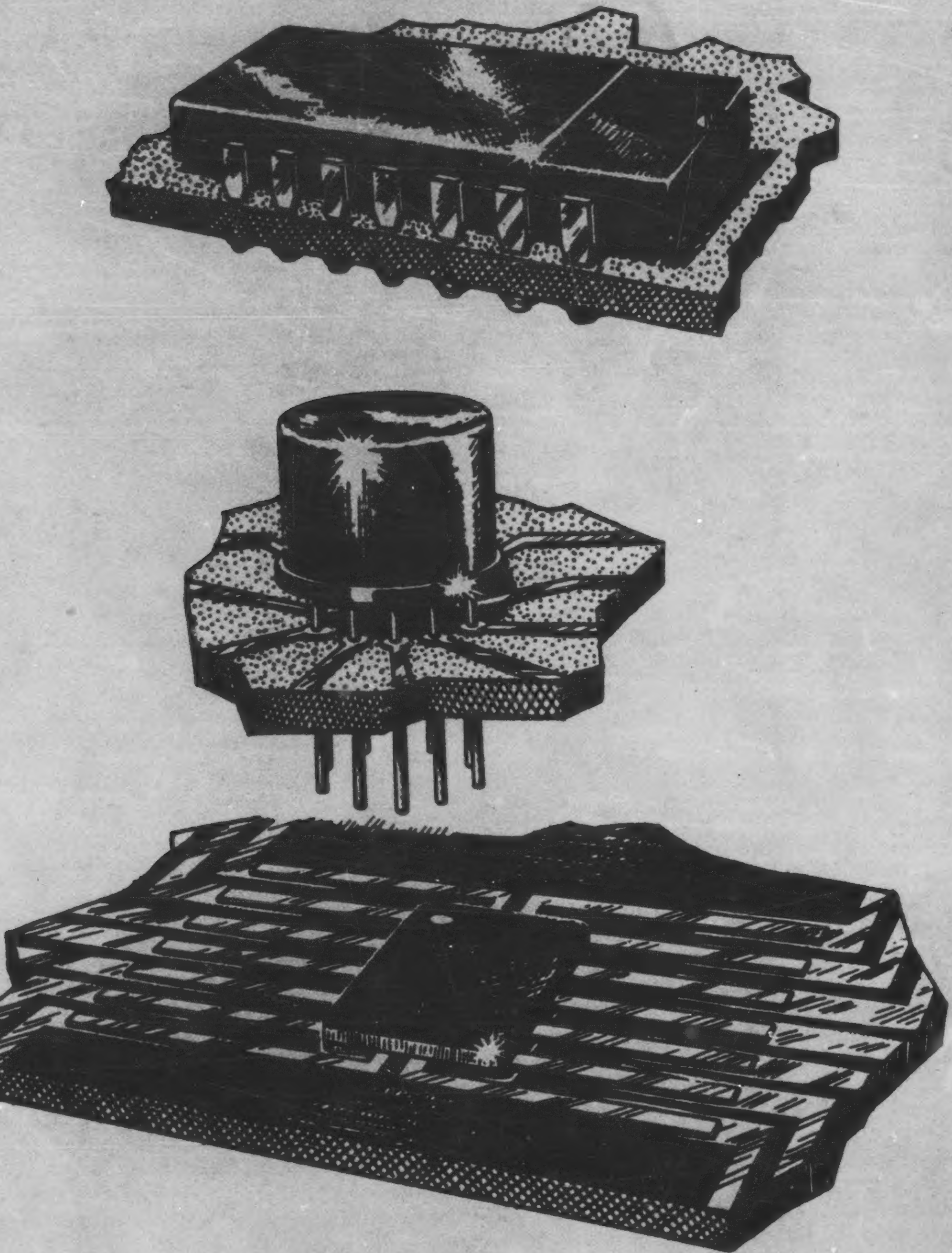


Figure 40. Integrated circuit designs.

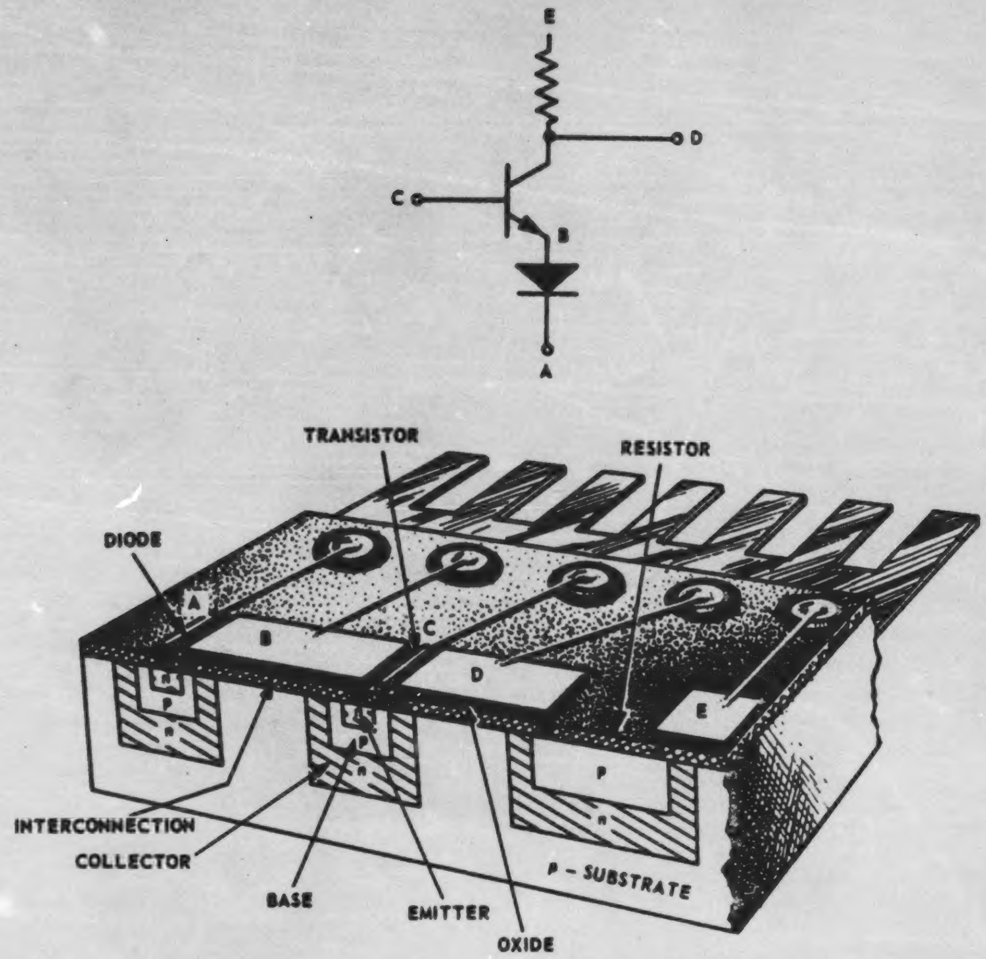


Figure 41. Integrated circuit composition.

tion given here—study the specifications of allowable solder iron sizes, voltage ranges, and other factors related to the placement in circuits. This is so that you thoroughly understand the damage you can do if you improperly repair a unit.

4-54. Conclusions. Replacement techniques always include safety, removal, replacement, and testing. Remove power, mark wires to be removed, remove component leads, and remove component. Clean leads and connector, replace defective component with a good one, install leads, and check by static and dynamic means. Be able to identify where in the -2 TO the chapter that lists the repair and replacement techniques is located. Also remember that the IPB, the -4 TO, lists the component part number and shows its placement in the circuit.

4-55. Secure the proper tools for performing this task; include soldering irons of the proper voltage and wattage rating, bending tools, cleaning tools, and alcohol. Use proper rosin flux. Understand that SN63 is the best type of solder for soldering of electronic components; however, SN60 is acceptable. Recognize defective solder joints as cracked, pitted, cold, stressed, impurities in solder, and excessive flux.

4-56. Wick or solder-suck solder from a joint requiring removal and replacement of a component, and prepare your tools for the job. Be sure your iron is clean and tinned; that all surfaces to be soldered are clean and dry, including the wire, lead, pad, and solder.

4-57. Apply sufficient heat to allow solder to flow, and apply solder so that a complete coating of solder covers the entire joint but does not obscure the definition of the component leads in the joint.

4-58. On crystal devices and microelectronic circuit elements, use heat sinks to protect the semiconductor structures in these units when soldering, whether it be the component lead to a pad type solder joint or the bridging technique.

4-59. Improperly learned techniques can result in equipment deterioration and corrosion. Therefore, you must understand some facts about corrosion in order to be able to prevent it.

5. Controlling Corrosion

5-1. Corrosion—the silent, devastating destroyer of computers and data processors—must be combatted continually. It may be found almost anywhere, and it takes on many forms, shapes, and colors. This section exposes the enemy and identifies the plan of attack used to combat it.

5-2. **General.** *Corrosion*, as defined in AFR 400-44, *Corrosion Prevention and Control Program*, is "Deterioration of metals owing to electrochemical or chemical attack resulting from exposure to natural or induced environmental conditions, or from the destructive attack of fungi or bacteria." Since you are new to the field of electronics, you probably haven't devoted a great deal of thought to the problem of corrosion as it affects electronic equipment. The subject may or may not have been brought out in technical school. In either case, we present a comprehensive study of corrosion and its direct threat to your maintenance record and your equipment. The areas to be covered include responsibilities of maintenance personnel; terms; the requirements needed for corrosion to form; causes of corrosions and types; recognition of corrosion; preventive maintenance, including uses of protective coatings and cleaning; and a partial listing of regulations and military standards you may wish to secure for a deeper study in this problem. First, let's consider responsibilities.

5-3. **Responsibilities.** The problem of corrosion control is acute. The Air Force has established distinct lines of responsibility for its prevention and control. Although not specifically named, these regulations do designate *you* as the man most responsible for the success of the program. For instance, AFR 400-44 lists specific areas for prevention and control of corrosion. The responsibility for compliance rests with you as well as your supervisors. These areas are:

- Selecting component and protective coating materials—to minimize susceptibility.
- Applying protective coatings during or after fabrication—corrective maintenance.
- Eliminating corrosion-inducing conditions such as water retention and corrosive environments.

The regulation also states that corrosion control will consist of minimizing development of and damage from corrosion by properly identifying, isolating, and eradicating corrosion and properly protecting equipment on a timely basis.

5-4. **Terms.** Before proceeding with the requirements for corrosion and other aspects of corrosion control, let's examine some new terms you will see in this study:

TERM	*DEFINITION*
ABRASIVE	Any substance used to wear, scrape, or grind away by friction as for grinding, polishing, etc.
ALKALI	A chemical that gives a base reaction (a substance which neutralizes an acid).
ALKALINE COMPOUND	A compound able to produce hydroxyl ions in solution, or having the properties of hydroxyl ions when in solution.
ALLIGATORING	A condition where cracks in the film are caused by contraction of the coating when a sudden change in temperature occurs during drying.
AMPHOTERIC METALS	Metals having both acids and basic properties.
ANODE	The positive electrode.
ANODE CORROSION	The electrochemical reaction with soluble anodes that causes the metal ions to go into solution at the positive electrode.
ANODIZING	The formation, by electrochemical means, of a thin oxide film on a metal surface.
BOND	A plate held to a basic metal by molecular forces.
CATHODE	The negative electrode.
CATHODE EFFICIENCY	The ratio of actual metal deposited on the cathode to that which is theoretically deposited, based on the amount of current.
CONDUCTIVITY	The ability of a solution to conduct electrical current.
CONDUCTOR	Any substance capable of passing electric current.

TERM	*DEFINITION*
CORROSION	Action or effect of a material being eaten away by degrees through chemical action; also products formed as a result of this chemical action.
CORROSION-RESISTANT METALS	Chromium, nickel, tin, tin-lead, solder, titanium.
ELECTROCHEMICAL PROCESS	A process involving a change in composition as a result of electrical current or production of an electrical current by chemical reaction.
ELECTROLYTE	Any substance which, in solution, is dissociated into ions and is thus made capable of conducting an electric current.
ENCAPSULATE	To coat a component or assembly by dipping, brushing, or spraying. Generally used to protect components from environmental and/or handling processes.
FERROUS	Compounds of iron in which iron is bivalent (combining of atom structures).
FERROUS METALS	Alloys containing iron.
GALVANIC GROUP	A list of metals having the same EMF characteristics.
HERMETIC	Permanently sealed by fusion, soldering, or other means, to prevent the transmission of air, moisture vapor, and all other gases.
ION	Acids (like hydrochloric acid), bases (like sodium hydroxide), or salts (like nickel sulfate) consisting of elements or a group of elements held together by electron attraction. When they are dissolved in water, the elements held together by electron attraction dissociate into particles that bear electrical charges. These charged particles are called ions.
INHIBITOR	A compound which restricts chemical reaction, especially corrosion.
OXIDATION	Combining with oxygen or increase in the positive valence of an element.
OXIDE FILM	An adherent coating resulting from the chemical reaction that occurs when a clean metal surface is exposed to air.
PASSIVATION	Rendering a metal inactive to chemical reaction or activity.
POLYMERIZATION	The reaction of two or more molecules of the same substance to form new products of higher molecular weight and, therefore, of different properties but without changing the chemical composition. The end product is called a polymer.
SCALE	A coating of metallic oxide that forms on a metal surface.
SILVER MIGRATION	The progression of metal from one conductor in a circuit to another which is at a different voltage potential.
SURFACE TREATMENT	Any chemical or physical process which affects only the surface of an object.

5-5. Four Requirements for Corrosion. Corrosion occurs under two conditions but must have four requirements for electrochemical action. The *direct attack*, which is destruction of a metal by a chemical such as acid or salt, can occur if improper chemical cleaning agents are used or if the equipment is exposed to sea air containing high salt content or air containing high amounts of humidity. The *electrochemical reaction* (a cell) is a corrosive attack in which there is an electron flow between an anodic area and a cathodic area which are separated by some electrolyte (see fig. 42). In order for electrochemical corrosion to occur, four elements must be present:

- Anode
- Cathode
- Electrolyte
- Conductor

By studying in figure 42, you can see that the four elements are present. The electrolyte is the obvious element to eliminate to stop corrosion. It is interesting to point out that when you or someone in your shop repairs an assembly and solders, you often have to clean off protective (hermetic) coatings from the parts on the assembly prior to working. This action is similar to opening the door to corrosion. However, if any one of the four elements is absent, no corrosion will occur. So let's study more about this subject of electrochemical corrosion.

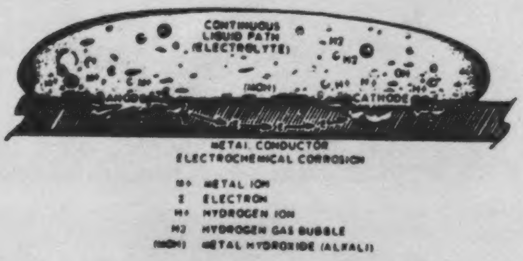


Figure 42. Corrosive cell.

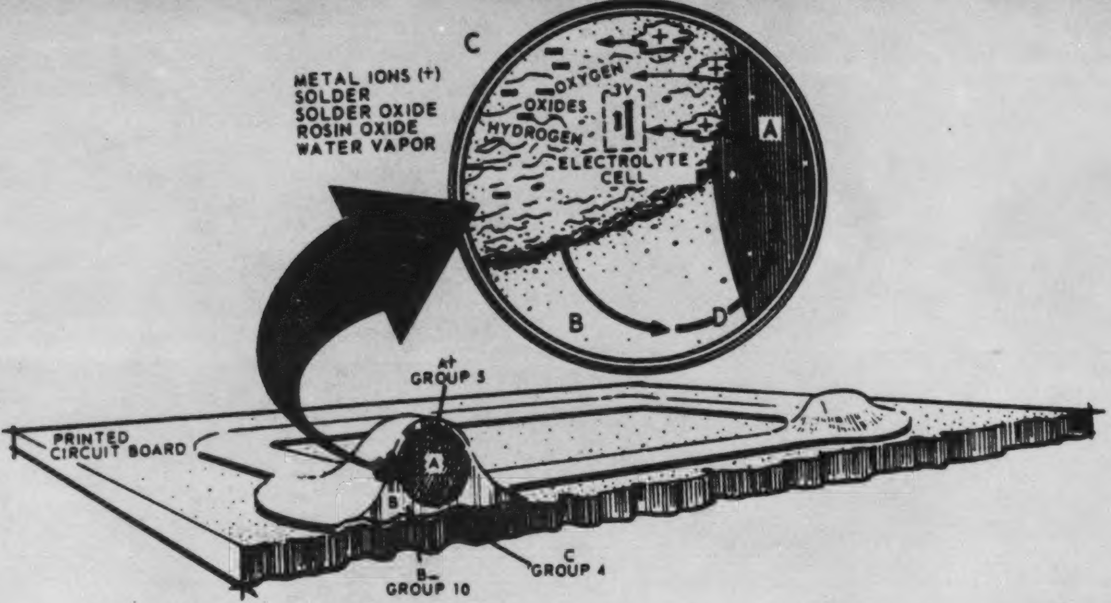


Figure 43. Corrosion process.

5-6. **Electrochemical Corrosion.** Three types of electrochemical cells can form:

(1) Galvanic cell — dissimilar metal electrodes in a common electrolyte.

(2) Concentrated cells — similar electrodes in a dissimilar electrolyte (oxygen concentrate).

(3) Electrolyte cell — an electrochemical cell supplied with an external source of electrical current (low constant potential)

The galvanic cell is created by maintenance personnel during replacement of components, leads, and cable. Therefore, it is explained in depth. The other two types of electrochemical corrosion are not frequently found because engineering in design phases of equipment manufacture account for these. However, you should know of them.

5-7. The galvanic theory, broadly defined, is that corrosion occurs between dissimilar metals when an electrolyte is present. Refer to table 5 (in the workbook) and study it to identify the following data. For instance, note the grouping of metals and conducting substances. Second, observe that each grouping is assigned an EMF value and, last, the permissible coupling combinations. To analyze the data in this table, consider the use of gold with copper—group 1 and group 4. Now the chart shows that these two metals are not permissible for coupling; therefore, a protective measure must be employed to eliminate the corrosive galvanic action. This may be done by interposing of a metal such as silver between the coupling, or designing the gold area (cathodic area) to be small in relation to the copper area (anodic area), or applying an inhibitor, a nonhygroscopic (passive) gasket between the metals. In any event, if your equipment comes from the manufacturer coated with a protective covering, it is because an electrolyte exists somewhere in the design of the equipment and provisions have been applied to prevent its contact with galvanic areas. One example: Gold-plated leads on integrated circuit packages.

5-8. The *rate* of corrosion is determined by the distance between the metals on the galvanic scale. The greater the distance between dissimilar metals as listed on the table, the more corrosive the coupling. Also included in the rate is the relative size of the anode and cathode areas. As the anode area decreased, the corrosion rate increases, and the reciprocal is true.

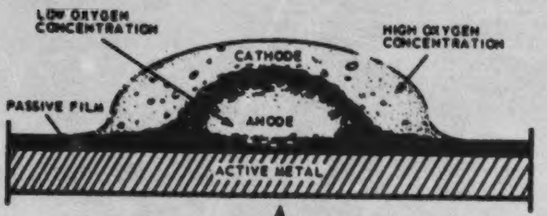
5-9. The corrosion process can be explained with figure 43. The four elements are shown as being present:

(1) The cathodic (A) — the copper and nickel alloy resistor lead (group 5).

(2) The anodic (B) — the solder lead (group 10).

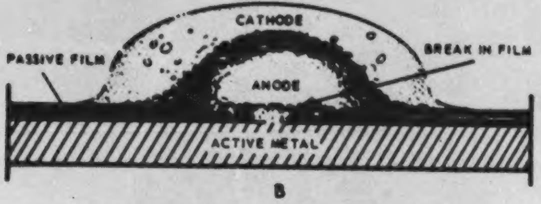
(3) The electrolytic (C) — moisture residue from soldering (oxides) but containing water.

(4) The conductor (D) — current from region B to A.



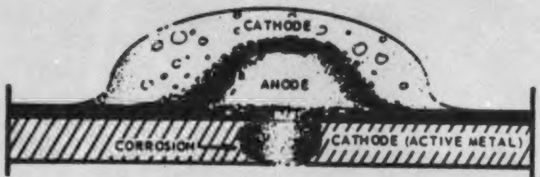
A

A SURFACE DIRT DEPOSIT IS COVERED BY A DROP OF WATER CREATING AN OXYGEN CONCENTRATION CELL.



B

OXYGEN CONCENTRATION CELL PRODUCES A BREAK IN THE PASSIVE FILM AT THE ANODE, EXPOSING THE ACTIVE METAL.



C

THE ANODE CORRODES AT A RAPID RATE BECAUSE IT IS IN CONTACT WITH A LARGE CATHODE.

Figure 44. Passive film rupture.

The corrosive area becomes a cell and assumes the position of a battery in a circuit. Group 10 material, solder, has an EMF voltage rating of -.50, and group 5 material, copper and nickel alloy, has an EMF rating of -.20; therefore, current flows from the negative B area to a more positive A area to the battery (corrosion cell), and a potential difference of .3V exists. Because of the action of the electrolyte, solder atoms from the anodic area break down into alkali particles. This action continues until one of the four requirements is taken away. Since the anode provides the material for the alkali and the cathode does not, the alkali is created at the cathode. A proper solder joint in this example would have provided the coupling sealer between the copper run and resistor lead and provided a smooth finish impervious to moisture, thereby reducing the chance for galvanic corrosion.

5-10. Let's examine a few places where corrosion can occur in data processing equipment.

a. Any time soldering is performed during maintenance anywhere in the system, corrosion must be considered and prevention must be applied.

b. Most pins are alloys; some are hermetically coated with a metal to provide better or greater conductivity. If the coating is scraped or worn away, electrochemical corrosion can start.

c. Human hands contain destructive agents which eat metal. These greases and corrosive chemicals attack unprotected metal surfaces and, with an electrolyte, start corrosion. They also soften encapsulants and allow penetration of electrolytes.

d. High-current-carrying components attract moisture and dirt and form electrolytes which try to and do eat through protective coatings.

e. Corrosion is accelerated by excessive wear on moving parts which are exposed to environmental conditions.

f. A high concentration of dirt containing water is another source of corrosion.

5-11. *Causes of corrosion.* Environmental surroundings provide the majority of electrolyte material needed for corrosion to start. These are water in any form, acids, salts, and alkalis.

a. Change in dew point. Any system employing air for conditioning is subject to variations in humidity. These variations between day and night cause more or less moisture to be taken into the system and cause the dew point in the equipment to vary. A removed and reinserted assembly will affect the humidity level within the unit and will supply the environment with water.

b. Uniform etching. This type of corrosion is caused by chemical attack over the entire surface. A good example here might be the turning black of a soldering iron tip.

c. Galvanic causes. The concentration cell may be one of three forms:

(1) Metal ion — metal ions in water.

(2) Oxygen — a concentration of oxygen trapped in a cell.

(3) Active-passive — metals which depend on a tightly adhering passive film. When a low oxygen concentration is trapped by an electrolyte, as shown in figure 44, the passive film is chemically eaten and corrosion occurs.

d. Pitting. This is evidenced by holes in the protective coating.

e. Intergranular. This is where corrosion starts between grains of metal.

f. Exfoliation. This is a form of intergranular corrosion.

g. Stress and fatigue. These causes are usually found in and around areas supporting high currents, or weights where actual breakdown of cells of metal can occur. Heated elements provide a source activity for this area.

h. Fungus and bacteria. These elements produce a growth of vegetable-like plant life and corrode the metals to which they affix themselves.

5-12. *Recognition.* All areas of data processors are subject to corrosion and the causes just mentioned bear this out. However, certain areas are more prone than others, and these are identified here:

a. Crevices. These exist in any joint where two metal surfaces come in contact.

b. Spot welds. Corrosion usually occurs here because of entrapment of corrosive agents between the layers of metal (see fig. 45).

c. Moisture (boxes, switches, connectors, and other enclosures). Accumulated by condensation through varying dew points, moisture will also allow bacteria and fungi to grow. These agents, if left unattended, can cause electrical shorts. Normally, 6 months to 1 year is required for these agents to cause serious problems. Moisture can accumulate within a sealed unit because condensation is deposited during a cooling period and cannot escape when the temperature rises during the daily temperature variation cycle. Moisture will therefore accumulate as a result of many temperature change cycles.

d. Uncapped conduits. These are especially prone to moisture collection when passed through exterior walls of buildings.

e. Premature paint failings. These include blistering, fish eyes, and flaking.

f. Discoloration of metal and alloys. Normally, metals and alloys are bright in color. When corrosion of these metals starts, distinctive discoloration begins to accumulate. The following list contains certain metals and their reaction to corrosion.

METAL	*DESCRIPTION/REACTION*
ALUMINUM	Normally bright, it becomes dull with a whitish powdery residue.
CARBON and ALLOY STEEL	Rust forms over the exposed surface; it appears in the form of a red-to-black scale.
CADMIUM-PLATED STEEL	Corroding cadmium will form a dull gray coating which can be wiped off.
COPPER ALLOYS	Unfinished copper and its alloys normally take on a dark color like an old penny. Corroded copper will be greenish-white in color. If corrosion is caused by acid such as flux, the color will be more grayish-white and quite voluminous.
TIN-PLATED COPPER	As tin corrodes, a white-yellow product appears on the exposed copper.
MAGNESIUM	Dry areas will have a gray powdery corrosion product. Moist areas will appear green or black when corrosion is present.

5-13. The discussion thus far has revealed that there are many recognizable signs by which the corrosion can be discovered. It therefore becomes all important to study methods for the prevention of corrosion. Preventing corrosion is often less time-consuming and more effective than curing the corrosion and restoring the equipment's reliability and functional capability.

5-14. Preventive Maintenance. Preventive maintenance for corrosion can be divided into two general areas: (1) the uses of *protective coatings,* including types and classes, synthetic binders, and functions, and (2) *cleaning,* including when to clean, what to use, how to clean, and what cleaning methods to use.

5-15. *Protective coatings.* A coating is applied as a liquid and forms a solid, continuous film after it has been applied. Coatings are divided into two main groups—inorganic and organic. These substances retain their basic properties after drying. Two tasks in which these coatings become extremely important are crimping and wire wrapping of leads and solderings. When performing a repair on, or installing a new pin in, a piece of equipment and crimping is used, the protective coating (if dissimilar metals are used) must not be broken. Some pins have elasticity and, if the correct crimping tool is used, the coating will not be broken. Since there is very little stress applied to wires, the crimp usually secures the wire firmly without affecting the protective coating. Soldering of components is performed in accordance with MIL-S-6872, 45743, 46844, and requirement 5 of MIL STD 454. Solder and flux are selected in accordance with QQ-S-571, type R or RMA. Solder joints are to be protected with mois-

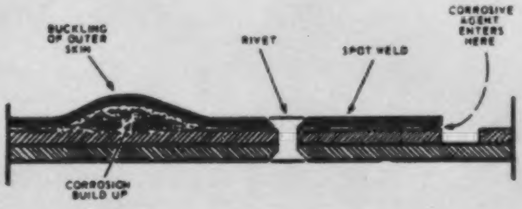


Figure 45. Corrosion in a spot weld.

ture-proofing coatings such as MIL-V-173 or MIL-I-46058, or as specified in the TO for your equipment.

5-16. Classes of coatings. Coatings are basically classified as paints, enamels, varnishes, and lacquers. There are two special forms—dopes and primers. Each coating is composed of a *vehicle*, which is a *binder* and *solvent*, and a *pigment*, the color.

5-17. Synthetic binders (resins). Coatings are commonly classified by the binder on which they are based. The binder is important because it limits the chemical and corrosion resistance of the complete coating. Coatings play an important role in corrosion abatement; however, improper coating substances can result in destructive corrosion acceleration. Two effective binders are acrylics and epoxies. Acrylics are highly durable, have excellent resistance to light and weather, and are an ideal top coat material for epoxy primer. Epoxies have outstanding adhesive properties as well as excellent chemical and corrosion resistance. Epoxies are formed when an oxygen atom is joined with two resin atoms.

5-18. Function of coatings. The primary function of coating is protection of the unit from environmental surroundings. Since most coatings rarely succeed 100 percent of the time, a more direct method is sometimes employed. That is, a primer coat is applied first, and it becomes the cathodic protection surface; or a passive primer may be employed, and it acts as a passive nonreactive agent to the environment. Protective coatings are also used to provide:

a. Surfaces to which other coatings may easily adhere.

b. Identification and/or marking.

c. Beautification.

5-19. *Cleaning.* Recalling that an anode, a cathode, a conductor, and an electrolyte must be present simultaneously for corrosion to occur brings us to a simple fact, but not so simple task. That is, one of the four elements must be removed to prevent corrosion. Cleaning removes surface contamination which, when combined with moisture, forms the electrolyte. These contaminants are dust and dirt and grime and grease, and they are the prime enemies to combat in performance of tasks associated with general maintenance. When performing the tasks already covered in this chapter and any other tasks requiring hands-on work, clean the equipment thoroughly and properly to prevent corrosion.

5-20. When to clean. Today's cleaning techniques for aerospace equipment are no longer a simple matter of applying water, soap, and elbow grease. Each piece of aerospace equipment demands its own unique cleaning techniques. A change of environment—e.g., moving equipment from an arid location, such as Texas, to a hot, humid place, such as SEA—also requires a reassessment of cleaning procedures Periodic inspections must be established on a regular basis to insure that cleaning is properly performed prior to the start of corrosion.

a. The appearance of dirt and grime on air-conditioning ducts indicates that immediate cleaning is necessary.

b. Battery areas require close inspection and prompt cleaning when spillage or corrosion is detected.

c. Oil and grease accumulations and spills should be removed when detected. This is particularly true for spills on painted surfaces because petroleum products will soften paint systems and cause them to fail.

d. High-humidity areas should receive inspections for fungus, and when it is detected, it should be treated immediately. Electronic *black boxes* that are cooled by a refrigerated forced air system are especially prone to fungus attack.

5-21. What to use. Proper selection of a cleaning agent and tools for a given problem depend upon three important factors: *type and amount of soil, condition and composition of parent metal,* and *degree of cleaning desired.* Soils may be placed into three classes:

a. Oily soils—oil, chemical, skin oils.

b. Semisolid soils—greases or heavy rust preservatives.

c. Solid soils—mud, corrosion, lint, dirt.

Each class of soil must be cleaned a specific way. Oily soils are usually removed with alkaline cleaners which are covered by specification MIL-C-25679. Very stubborn areas may be removed with solvent P-D-680, followed by alkaline cleaning. It is important to thoroughly rinse the area after cleaning to insure that no alkali remains. Semisolid soils are also removed from a surface with the appropriate solvent followed by alkaline cleaning. Solids must be removed with solvent followed by alkaline pressure spraying, scrubbing, and rinsing. Remember, aging makes the soil even more difficult to remove, so help establish timely cleaning procedures for the equipment.

5-22. Alkaline cleaners (i.e., MIL-C-25679) remove soil by dispersing it from the surface and holding it in suspension with the cleaning solution. Fatty soils will react with the alkali to form water soluble soaps; in fact, pioneer women produced soap with the same chemical reaction by mixing lye and grease. Alkaline water-base cleaners are the most common type of cleaner used in the Air Force today. When the cleaner is fully mixed, it is basically a water solution of silicates, phosphates, and wetting agents. It is useful in hard water because it tends to prevent the formation of solid hard water deposits. This cleaner performs well on oily and traffic soils. The solution must be thoroughly rinsed when cleaning is finished.

5-23. Solvent cleaners remove soil by dissolving it and usually leave a thin oily film which can easily be removed with an alkaline cleaner. Acid cleaners remove soil by chemical attack and are often used to remove corrosion products.

5-24. Cleaning tools are as follows:

(1) Vacuum cleaners.
(2) Brushes, all types, sizes, and bristles.
(3) Abrasive papers, cloths, emery.
(4) Grinders, belts, disks, rotary files.
(5) Spray units using sand, steel balls, glass beads.
(6) Polish cloths, impregnated silicant cloths, lint-free rags.

5-25. How to clean. Cleaning must be done in logically planned steps to obtain efficient, satisfactory results.

a. Assure that the cleaning apparatus and soiled equipment are close to each other prior to starting the operation.

b. Clean the soiled equipment as specified in appropriate TOs.

c. Clean off contaminants by vacuum or wiping.

d. Apply the cleaner (if applicable) until the soiled area is completely covered, and begin cleaning at the lowest surface.

e. Agitate the compound by scrubbing the surface with a nonmetallic brush.

f. Finally, thoroughly rinse the cleaned area. (Remember, alkali dissolves amphoteric metals.) Inspect areas such as seams and lap joints to insure that the cleaner has been rinsed away. If the cleaning compound dries on the surface, streaking will occur.

g. Apply abrasives or blasting if severe corrosion exists as is specified in the TO or MIL specification.

5-26. Cleaning methods to use. There are two techniques which can be used in cleaning. These are the *chemical* and *mechanical* techniques. Selection of the method to use or combination of methods to use depends upon the type of corrosion detected, the degree of corrosion, and the accessibility to the corrosive area. Consideration must also be made as to the types of metals employed in the system. Some equipments are provided with kits containing acids and dopes for identifying the metal, and then the technical order prescribes the correct cleaning agent and application technique. Listed below are some of the common metals found in data processors and ancillary equipment, and the typical treatment methods and agents.

5-27. The *chemical* technique is generally applied for cleaning and removal of light corrosion. The removal of soil such as oil, grease, dirt, lint, fingerprints, and other foreign residue with various solvents and detergents is an example of chemical cleaning.

METAL OR ALLOY	*TREAT WITH*
COPPER and COPPER ALLOYS	1. Alkaline water-base MIL-C-25769 or P-S-661, Type II, for grease. 2. Vapor degreasing is accomplished using trichloroethylene MIL-T-27602. 3. Generally, no protective coating is required unless specified by the manufacturer in the TO.
ALUMINUM ALLOYS	1. Alkaline water-base cleaner MIL-C-25769, or dry-cleaning solvent P-D-680, Type II. 2. Mechanical methods for removal of corrosion are recommended. 3. Coat surface according to TO specifications.
MAGNESIUM ALLOY	1. Alkaline water-base cleaner MIL-C-25769 and solvent FED SPEC P-D-680, Type II. 2. Use either chemical or mechanical methods to treat metal. 3. Apply protective coating according to TO specifications.
FERROUS METAL	1. Alkaline water-base cleaner MIL-C-25769 or FED SPEC P-D-680, Type II. 2. Mechanical methods are recommended. 3. Prime and paint immediately after cleaning and treating.

METAL OR ALLOY	*TREAT WITH*
STAINLESS STEEL and NICKEL-BASE ALLOYS	**1. Alkaline water-base cleaner MIL-C-25769 or dry-cleaning solvent P-S-661, Type II.** **2. Mechanical methods are used when chemical methods are impractical.** **3. Chemical methods are recommended on installed components.** **4. Methylene chloride or trichloroethylene may be used for wiping surfaces, *but* surface must then be cleaned after chemical corrosion removal with alkaline or dry cleaning agents.**

The application explained here is concerned with light corrosion. Heavy corrosion can exist and, if extremely severe, the corroded components may have to be removed and treated or replaced.

5-28. The *mechanical* technique is usually associated with the removal of heavy corrosion in which abrasive papers, wheels, and disks are used, or blasting is used. However, mechanical techniques can be used when light corrosion exists or especially when electrolyte contaminants are in evidence; e.g., dust, dirt, mud, condensation, humidity, fungus, and silver migration. In this area of control, mechanical means of cleaning, such as using lint-free rags, brushes, or vacuums, represent preventative maintenance as a way to control corrosion by its prevention.

5-29. **AF Regulations, Manuals, and Military Specifications.** The following partial list of military publications is presented here for your use in becoming knowledgeable to the threat of corrosion. A study of these publications will benefit you and improve your technical competence.

a. AFR 66-8, *Maintenance Evaluation Program.* This regulation explains and assigns responsibilities for a Maintenance Evaluation Program. Change 1, 8 March 1968, explains ground C-E-M responsibilities.

b. AFR 400-44, *Corrosion Prevention and Control Program.* This regulation explains the program and assigns responsibilities for attaining the objectives.

c. MIL-STD-1250 (MI), 31 March 1967, *Corrosion Prevention and Deterioration Control.* This standard is designed to establish minimum requirements for the control of corrosion. It also lists all military and Federal specifications which apply to electronic and electromechanical components and electronic equipments.

5-30. **Conclusions.** The more we study corrosion, its control, prevention, and treatment, the more we begin to realize the impact it has on the reliability of the system and the vast areas it may strike. The threat is real and acute. The manufacturer of the equipment studied the problem and provided, as best he could, a product which should not corrode, but he cannot present you with a 100-percent sealed unit unless it is in a vacuum. Therefore, you must use the knowledge gained from this text in the performance of your tasks which expose areas to corrosion. Remember, when dissimilar metals, an electrolyte, and a conductor are present, corrosion will occur. Preventing corrosion is easier than treating it. So clean thoroughly with proper solutions and use filter paper, filters, etc., to reduce the area where moisture can collect. Clean off grease deposited from hands, oils, and other chemicals which may perform a direct attack. Also, remember that grease deposits may trap oxygen, and the chemical action resulting could be that a protective epoxy coating could be softened and penetrated and corrosion could result. Poorly repaired assemblies with improper solder joints, flaked solder residue, burned or charred flux, impurities in cleaning solvents, phenolic flaking (PCB base material) or burned residue all lead directly to corrosion.

MODIFICATIONS

Pages 51-55 of this publication has (have) been deleted in adapting this material for inclusion in the "Trial Implementation of a Model System to Provide Military Curriculum Materials for Use in Vocational and Technical Education." Deleted material involves extensive use of military forms, procedures, systems, etc. and was not considered appropriate for use in vocational and technical education.

7. Interpreting Wiring Diagrams and Correlating the Diagrams with Connectors, Interconnecting Cables, Cabinets, and Remote Equipment.

7-1. Interpreting wiring diagrams is an extremely important task of any qualified maintenance technician. This is especially so when you realize that your equipment is often made by different contractors and is linked together through cables. Each unit, OA (operational amplifier) group, assembly, or subassembly has some form of interconnecting wiring. Each unit contains interconnecting cables within the unit. It therefore follows that a complete understanding of the data flow between units and within units and a comprehensive knowledge of the techniques employed by contractors to interconnect components is essential for you. You have been through school and have learned to read logic. You probably received some explanation on rack jack signal tracing. You may have heard of the *main distribution frame*, *filter panel*, or *junction box*. In this section you will study (1) the equipment and terms of the system, (2) the technical order references, and (3) vertical and horizontal methods used to form lists of data and voltage signal distribution routes.

7-2. **Elements.** In Section 6 we discussed the various numbering systems employed for Air Force equipment, and we brought out that by using a numbering system you identify a specific location in your equipment. In Chapter 2 we analyzed connectors and learned exactly what a jack is, what a plug is, and what a fixed connector is. Both of these subjects are brought into focus in this section. Each one is directly related to the discussion on interpreting wiring diagrams because you must identify and understand the layout of the equipment in order to effectively trace data or voltage through cabinets and units. The following list of terms will aid you in understanding the explanations that follow.

TERMS	*DESCRIPTION*
BAYS or RACKS	1. Assemblies usually reaching from the floor to the ceiling within a cabinet. 2. They may be fixed or hinged. 3. They usually contain chassis, drawers, or subassemblies. 4. They generally have a distinctive identifying location number. 5. They generally provide a major function for the overall unit or system.
CABINETS	1. A unit or OA group consisting of a functional group of assemblies designed for a specific purpose. 2. Examples: Console, printer, data processor, memory unit, input device.
CABLE	1. A length of wire, either single or multiple leads, usually covered with a protective outer weather-resistant coating. 2. Generally, the cable is labeled with a "W" and number, identifying it. 3. The label often contains the length of the cable and the connecting units to which it is attached.
CHASSIS	1. Assemblies or subassemblies within a unit designed as a logical assembly which normally provide a function for the unit.
DRAWER	1. Similar to a chassis, only designed to be rapidly removed and replaced.
FILTER PANEL	1. Usually an assembly panel affixed to the outer shell of a unit for the purpose of filtering data leaving the cabinet. 2. A filter panel may be remote from the unit, but it still provides the same function.

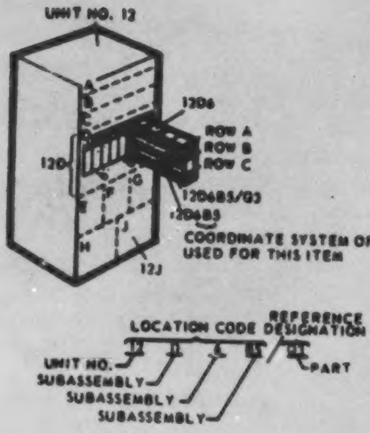


Figure 51. Location coordinate coding.

TERMS	*DESCRIPTION*
JACK	1. The more fixed connector of a mating pair. 2. Designated by the letter "J" or "X."
MAIN FRAME (MAIN DISTRIBUTION FRAME)	1. A common focal point where cables from units and assemblies are joined to elements within the frame in order to allow passage of signals between units. 2. This unit reduces the need for extensive cabling; allows for greater distribution of signals and greater variety of equipment configuration. 3. This term is *not* to be confused with the definition of a main frame used in computer terminology.
PLUG	1. The most movable connector of a mating pair. 2. Identified by the letter "P."
TERMINAL BOARD	1. A rectangular unit consisting of multiple connectors, usually screw type. 2. Designed to connect two or more lines to a specific source. 3. Quite often found in high-voltage power units, high-voltage couplers, filter panels, main frames, and circuit breaker boxes. Usually designated "TB."
UNIT	1. A major assembly. It may be a cabinet or an AN item; it may be an OA group; in any event, it is a numbered item.

7-3. **Technical Orders.** Two technical orders which are used most extensively while working with equipment numbering are the -2 and -3 TOs (service manual and circuit diagrams manual). The service manual, the -2 TO, provides in Chapter 2 the technical data for installation of equipment. This chapter defines:

- Installation layout.
- Requirements for power and environment.
- Site considerations.
- Inspections of installations.

In the descriptions and tables in this TO, the data needed to interpret wiring diagrams is:

- Cable identification — cable number.
- Routing data.
- Termination.
- Jack and plug pin lettering and wire color coding.
- Component part number.

7-4. The circuit diagrams manual, the -3 TO (unless Sections III and IV of the -2 TO are used), provides the technical data for point-to-point signal tracing of data. This may be accomplished in various forms. It may be in the form of a wiring table as used in the 416L and 465L systems, or it may be in the form of a plug and jack layout as in the 416L or 412L systems. This TO also provides data on cable numbers between units, between units and main distribution frames, and between units and filter panels. Quite frequently the "J" number on the unit or component is shown on a block diagram along with the "W" wire number. We will examine some of the methods most commonly employed, and you must determine which method is used in your system and where it is used. NOTE: See comment in Preface about TOs.

7-5. In the following paragraphs you participate in the identification of connecting points of signals in a problem-solving type of presentation. After the titles Data Signal Flow I, Data Signal Flow II, and Data Signal Flow III, carefully study the italicized objective of each problem; then proceed with its solution.

7-6. **Data Signal Flow I.** *Identify the interconnecting connectors of a data signal from its origin to its point of use.* This situation presents one signal which is routed through components, jacks, cabinets, and cables so that you can visually trace the signal as it proceeds from point to point. The objective here is to identify each connecting point and, by forming the alphanumeric code, relate the number to a real place in the equipment. By proper full alphanumeric formulation and sequential listing of the numbers, you will easily know when you have exited a chassis, rack, bay, or cabinet.

a. Before making your wiring list, follow along as we show you how the range marks are routed. Refer to figure 52,B (in the workbook) and locate module location XA22 in cabinet 45. This is the origin of the range marks. Follow the connecting lines through XA13, 12, and 14, out of the rack jack J2, out of the cabinet jack J17, through cable W6060 into connector panel A14, jack J2 of cabinet 46, through rack jack J2, into module XA2, then to module XA1, to the HVC (high-voltage coupler), out of the coupler into the rear of the CRT and to the displayed range marks on the CRT face. When you, as the man who has to identify this routing data, compile it as shown in figure 52,A, it is complete. However, when you physically try to locate these points and the signal is routed, as you can see, from chassis to racks to cabinets to other cabinets, your wiring list takes on a physical dimension and you must translate these physical characteristics into knowledge and understanding of the nomenclature of the connectors as well as their physical placement. Now complete the list below.

b. Refer to figure 52,A. List, by using full alphanumeric code and the vertical listing method, the assemblies, jacks, plugs, and cables in order from the range mark generator to the CRT.

(1)________________
(2)________________
(3)________________
(4)________________
(5)________________
(6)________________
(7)________________
(8)________________
(9)________________
(10)________________
(11)________________
(12)________________
(13)________________
(14)________________
(15)________________

c. List the jack/plug and terminal board connectors for *chassis* and *cabinets* using the full alphanumeric code.

Chassis	*Cabinet*
(1)________________	(1)________________
(2)________________	(2)________________
(3)________________	
(4)________________	

d. Your responses to paragraph *b* above should have been:

(1) 45A2A1XA22-7
(2) 45A2A1XA13-16/4
(3) 45A2A1XA12-17/6
(4) 45A2A1XA14-19/6
(5) 45A2J2/A1P202-J
(6) 45A1J17-6
(7) W6060
(8) 46A1A14J2-6
(9) 46A2A1P3/A2J2-G
(10) 46A2A2XA2-16/6
(11) 46A2A2XA1-8/6
(12) 46A1A10TB2-6
(13) 46A1A10
(14) 46A1A10TB1-1
(15) V1-3

e. Your responses to paragraph *c* above should have been:

Chassis	*Cabinets*
(1) 45A2J2/A1P202-J	(1) 45A1A1J17-6
(2) 46A2A2J2-G	(2) 46A1A14J2-6
(3) 46A1A10TB2-3	
(4) 46A1A10TB1-1	

7-7. **Data Signal Flow II.** *Identify and list the connecting points of a multi-used signal, using the chart and accompanying figures 53 and 54* (printed as a foldout and placed at the back of the workbook). In this problem, data generated from module 611 is to be used in various portions of the FGD (fine grain data) equipment. It is also routed to two remote units, the SIF (selective identification feature) unit and the SM-137 Simulator. Again this circuitry must be studied with the approach that data transferred to other areas and units must be routed by cables through connectors, and all the connecting points must be identified.

a. Refer briefly to figure 53 and observe that the original generator 611 is distributing its output to five main paths. Three paths complete their action in the FGD cabinet, and of the other two, one goes to the SIF and one to the SM-137.

b. Now follow along and observe from the pictorial view in figure 54 how the physical routing of the signal is accomplished. Find card location 611, *the darkened rectangle in the FGD cabinet, bay 600,* subassembly 601-640:

(1) Follow the solid line from 611 to 629. This is the termination of this leg which generates a new data signal (RM6).

(2) Also from 611 to a pin on 613, the signal is fed through 613 to 623, where it generates another signal (TP1).

(3) Follow again from 611 the line to 613 (another pin) to 614, through 622, through jacks and plugs, to bay 800, through more jacks and plugs, out of the FGD cabinet, into the SIF cabinet, and more jacks and plugs in the top of bay 400, to drawer 503, and jacks and cards in rows 3 and 1 of drawer 503. This signal terminates in card 503103 of the SIF unit.

(4) Again follow another output from 611 to 616 through the jack and plug 602119, out of bay 600 into the lower portion of bay 800/900 to location J/P980112. This signal exits bay 800 here and is routed by coax lead to lower rack jack 4960 of bay 4800. From there it goes to jack plug 4682117, and then into card 4693018. The signal is terminated at A4693.

(5) Locate 611 again and trace the line leading from it to J/P602113 and 114. Note that two circuits on module 611 are used before the connection at 602113 is made. J/P602113 coax lead is fed to the 3 units A641, A641, A701. The "CP" connections are coax "T" connectors.

(6) The lead from J/P602114 goes to bay 800 and 900. In bay 800 it is tied at CP841,

and one line is fed to J/P842104 which feeds two modules, 844 and 846, and the other branch of the tie is fed to J/P902105 and feeds four modules, 884, 886, 904, and 906.

c. Now use chart 1 (horizontal method) in the workbook and list in order the connecting points of each separate path. Do this by indentifying the jacks, plugs, cables, and assemblies in each path. Identification of input and output pins on jacks is indicated at the rear of the jack number as follows:

in out
J611014/018

d. Your responses on the chart should have been as follows:

(1) RM3 to RM6
J611015 - J629018/015
(2) RM3 to TP1
J611015 - J613014/018 - J623017
(3) RM3 to SIF
in out
J611015 - J613005/004 - J614002/010 - J622014/013 - J/P602101 - J/P800119 - cable 5622 - J/P403703007 - J/P503405001 - J50332053/050 - J503103004 (HFF-1)
(4) RM3 to SM-137
J611015 - J616005/004 - J/P602119 - J/P980112 - cable 5623 - J/P4960 - J/P4682117 - J4693018
(5) RM3 to assemblies in bay 600
J611015 - J611002/003 - J/P602113 - CP642; branch A - J/P701109 - A701; branch B - CP682; branch A - J/P641109 - A641; branch B - J/P681109 - A681
(6) RM3 to bay 800/900
J611015 - J611002/003 - J/P602114 - CP 841; branch A - J/P842104 - J844018 and J846016; branch B - J/P902105 - J884002 and 018, and J886016, and J904002 and 018, and J906016

7-8. In this exercise you compiled individual lists of a multipath signal. In real application on line, possibly only one or two of the paths would have had to be checked. However, in our objective we had to prove that in interpreting wiring diagrams, connectors are used to route data. The figure and your completed lists have proven this. A signal which started in a card in a bay has been distributed to chassis, other bays, and other cabinets each time a connector, jack, or connecting point was used. This is the second application of interpretation of wiring diagrams, and some very definite characteristics are becoming evident:

- Originating signals are generally fed to a connecting point such as a jack.
- Multiple routing of a signal is accomplished with jacks and connectors.
- Each point of a junction is identifiable by a location number.
- The data for making a complete signal wire list may have to be extracted from various technical orders (such as the TO on the FGD, SIF, and SM-137 equipments in this example) and, within the TOs, from selected chapters or sections providing connecting point listings (jack listings).

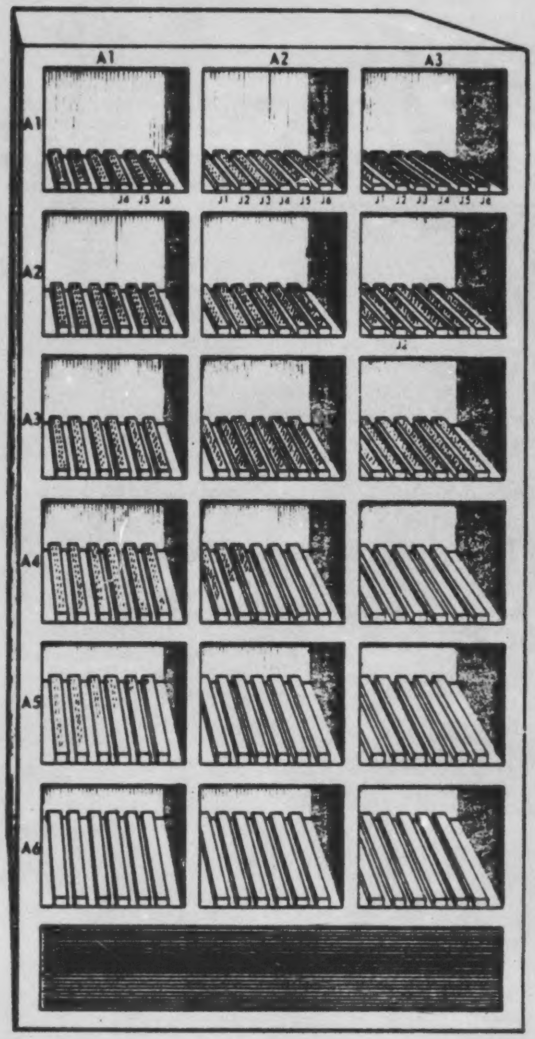


Figure 55. Main distribution frame.

7-9. Data Signal Flow III. *Use the wiring table to identify and locate interconnecting cables between the main distribution frame and units.* In performing this task we will have to identify what a main distribution frame is and show its relative position in a system wiring scheme. It was defined in paragraph

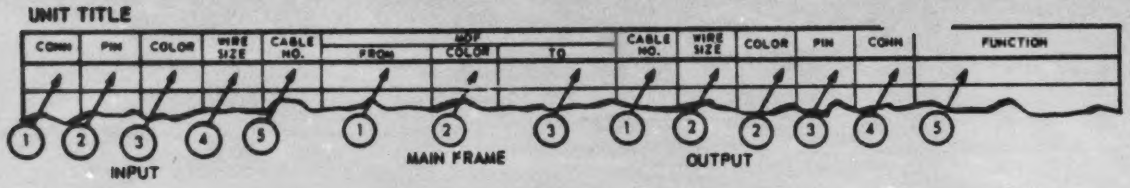


Figure 56. Table layout.

7-2, and if you observe figure 55, you can see a pictorial representation of a typical frame. This discussion is based upon the use of a main frame, but the principles of usage are the same if, instead of a frame, a filter box or junction box is used. The frame is the most complex of the three, so it is selected for this study.

a. Refer again to figure 55 and observe how this unit is made of rows and columns and tiers or planes. Each location is identifiable by a coordinate number consisting of a row, a column, and a plane number usually given a "J" prefix. Each pin connection on each jack further identifies the exact point connection. Generally, all connections from a unit are located within specific groups of rows and columns. Signals are transferred to another unit usually by use of single-strand wire from point to point within the frame. In order to facilitate the installation and tracing of signal paths, tables are formed, with the main frame being the focal point of the table.

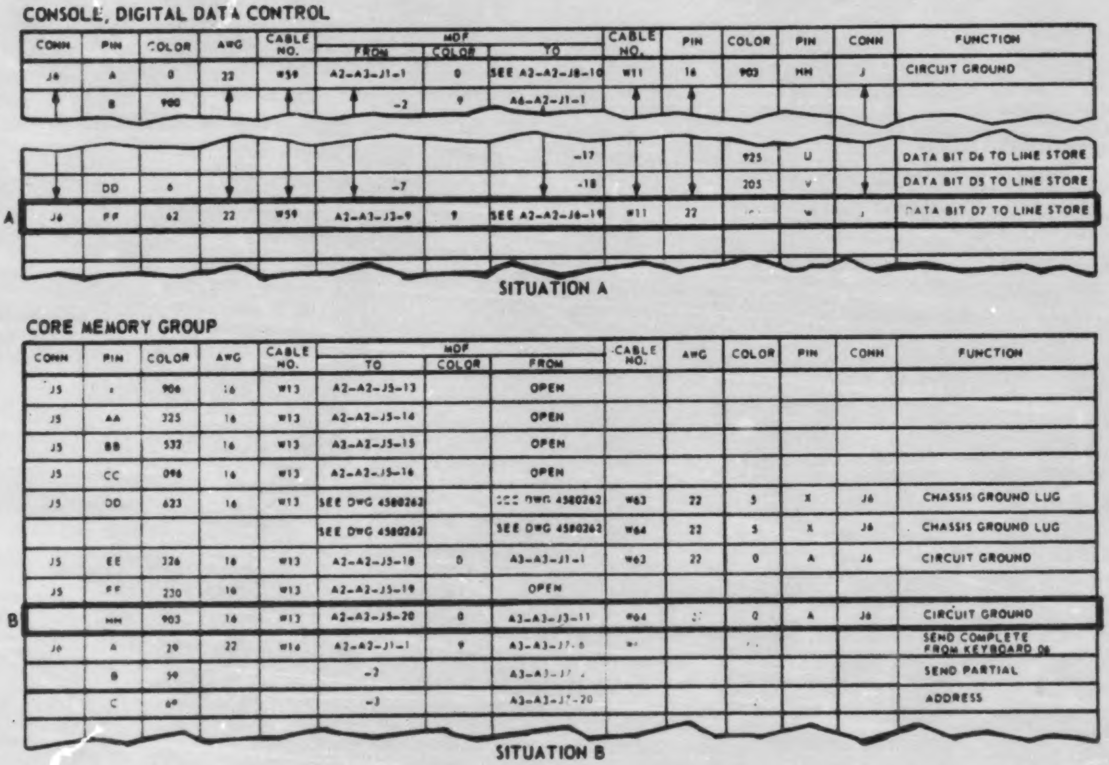
b. Refer to the table layout in figure 56. The table will very likely contain these columns and this data:

Input

(1) A connector point.
(2) A pin number in the connector.
(3) Color of wire.
(4) Size of wire.
(5) A cable number.

Main Frame Connectors

(1) Point of connection of input cable.
(2) Color code of wire.



CONSOLE, DIGITAL DATA CONTROL

	CONN	PIN	COLOR	AWG	CABLE NO.	MDF			CABLE NO.	PIN	COLOR	PIN	CONN	FUNCTION
						FROM	COLOR	TO						
	J6	A	0	22	W59	A2-A3-J1-1	0	SEE A2-A2-J8-10	W11	16	903	HH	J	CIRCUIT GROUND
	↑	B	900	↑	↑	↑ -2	9	A6-A2-J1-1	↑	↑			↑	
								-17			925	U		DATA BIT D6 TO LINE STORE
	↓	DD	6	↓	↓	↓ -7		↓ -18	↓	↓	205	V	↓	DATA BIT D5 TO LINE STORE
A	J6	FF	62	22	W59	A2-A3-J3-9	9	SEE A2-A2-J6-19	W11	22	[illegible]	W	J	DATA BIT D7 TO LINE STORE

SITUATION A

CORE MEMORY GROUP

	CONN	PIN	COLOR	AWG	CABLE NO.	MDF			CABLE NO.	AWG	COLOR	PIN	CONN	FUNCTION
						TO	COLOR	FROM						
	J5	[illegible]	906	16	W13	A2-A2-J5-13		OPEN						
	J5	AA	325	16	W13	A2-A2-J5-14		OPEN						
	J5	BB	532	16	W13	A2-A2-J5-15		OPEN						
	J5	CC	096	16	W13	A2-A2-J5-16		OPEN						
	J5	DD	623	16	W13	SEE DWG 4580262		SEE DWG 4580262	W63	22	5	X	J6	CHASSIS GROUND LUG
						SEE DWG 4580262		SEE DWG 4580262	W64	22	5	X	J6	CHASSIS GROUND LUG
	J5	EE	326	16	W13	A2-A2-J5-18	0	A3-A3-J1-1	W63	22	0	A	J6	CIRCUIT GROUND
	J5	FF	230	16	W13	A2-A2-J5-19		OPEN						
B		HH	903	16	W13	A2-A2-J5-20	0	A3-A3-J3-11	W64	[illegible]	0	A	J6	CIRCUIT GROUND
	J6	A	29	22	W16	A2-A2-J1-1	9	A3-A3-J7-6	[illegible]		[illegible]			SEND COMPLETE FROM KEYBOARD 06
		B	59			-2		A3-A3-J7-[illegible]						SEND PARTIAL
		C	69			-3		A3-A3-J7-20						ADDRESS

SITUATION B

Figure 58. MDF routing.

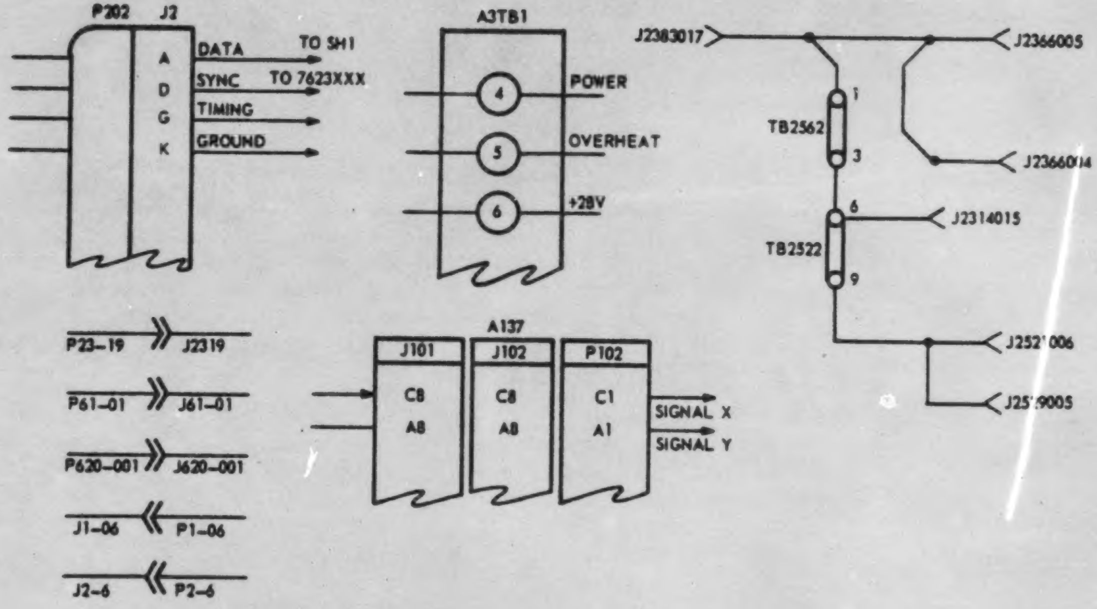

P202
J2
A
D
G
K
DATA
SYNC
TIMING
GROUND
TO SH1
TO 7623XXX
A3TB1
4
5
6
POWER
OVERHEAT
+28V
J2383017
J2366005
J2366014
TB2562
1
3
6
9
TB2522
J2314015
J2521006
J2519005
P23–19
J2319
P61–01
J61–01
P620–001
J620–001
J1–06
P1–06
J2–6
P2–6
A137
J101
J102
P102
C8
A8
C8
A8
C1
A1
SIGNAL X
SIGNAL Y

Figure 59. Jacks.

(3) Point of connection to output cable.

Output

(1) Output cable.
(2) Size and color of wire.
(3) Pin number
(4) Connector number.
(5) Functional requirement of the signal.

c. With this information we can begin to apply the analysis to a situation/problem. To do this we will use figure 57 (in the workbook). Our task, once again, is to use the table to identify and locate the interconnecting cables between the main frame and the units.

d. Follow along once again as we use views A and B, and the routing data table on figure 57. Let's suppose that we are required to determine where data bit "DO" was routed to understand a modification change, or for some other reason. Look at the table and observe the expanded area (fig. 57). The "DO" data signal is transferred from J6, pin r, of the console through cable W59 to the main frame where wire little r is connected to A2-A3-J1-15—vertical row A2, horizontal row A3, first terminal row J1, and contact 15. From that point it is routed by a color #9 wire to A2-A2-J8-12. Pin 12 has one lead from W11 with a color #209 wire connected, and the other end of cable W11 wire color #209 is connected to J1, pin N, on the line store (memory unit) functional assembly. It is actually quite easy to perform this task once analysis is applied.

e. Perform situations A and B which follow by using the vertical listing method, and by listing in order, connector points, cables, jacks, etc., of each signal path. Start at the console in situation A and at the memory group in situation B. Use figure 58; refer to figure 57 for routing.

Situation A	*Situation B*
(1)________	(1)________
(2)________	(2)________
(3)________	(3)________
(4)________	(4)________
(5)________	(5)________
(6)________	(6)________
(7)________	(7)________
(8)________	(8)________

f. Your responses to situation/problem A and B should have been:

Situation A	*Situation B*
(1) J6, Jack 6 at console	(1) J5 at memory unit
(2) Pin FF in J6	(2) Pin HH on J5
(3) Cable W59	(3) Cable W13
(4) A2-A3-J3-9 (MDF)	(4) A2-A2-J5-20 (MDF)
(5) A2-A2-J6-19 (MDF)	(5) A3-A3-J3-11 (MDF)
(6) Cable W11	(6) Cable W64
(7) Pin W on J1	(7) Pin A on J6
(8) Jack J1 at memory unit	(8) J6 at the console

7-10. In this analysis we examined how the main frame is used as a connecting point between units. It is easy to understand how useful this unit is because of its great flexibility. Tracing connectors and connector connections is simplified when the pictorial view is associated with the tables and cable layout drawings. If a filter box layout or distribution box layout were used in the analysis just completed, the following data would have been needed:

- Cable numbers for incoming and outgoing signals.
- Jack and plug numbers.
- Pin numbers on jacks.
- Filter or terminal board connectors points.

7-11. **Jacks.** Figure 59 shows a few examples of how jacks and plugs are laid out in logic diagrams and wiring diagrams. These symbols have been used in each of the situation/problem analyses just completed.

7-12. We have described some of the typical wiring situations found in data processors, where the task of interpreting wiring diagrams is employed. We have identified the components necessary for a list to be compiled so that a complete picture of the signal path can be obtained. Some terms were identified and explained. It should be noted here that when using wiring diagrams and tables in forming a list or tracing a signal to find its connecting points, you sometimes may double back upon yourself. This means that while going from jack to jack, etc., and flipping pages of logic, you can reverse your direction and return to the starting point. To prevent this, a complete understanding of jack/plug nomenclature and a complete nomenclature of all connectors must be recorded in your list. This data will reveal any reversal trend. We have identified and used the vertical listing technique and the horizontal listing technique in the three situations. Adaptations of these techniques should be developed by you after a study of your equipment configuration so that you completely understand the signal routing.

7-13. Let's list once more the points that we have identified which will aid in interpreting wiring diagrams:

- Cables are numbered with "W" on both incoming and outgoing lines.
- Jacks and plugs each have numbers prefixed with J or X or P.
- Jacks are indicated at the *point* of the double arrow or the rectangle on schematics.
- Plugs are indicated on the *back side* of the double arrow and on the *rounded corner* rectangle on schematics.
- Each pin has a letter or number or both on jacks and plugs. All letters are used except i, o, and q.
- Upper- and lower-case letters are used.
- Terminal boards normally use numbers in preference to letters for connecting points.
- Main frames, filter boxes, and junction boxes provide the same basic functions, except that the filter box also provides isolation by filtering.
- You will need logic and wiring diagrams and wiring tables, cable listings, and rack jack listings to perform this analysis.

54

CHAPTER 4

Test Equipment

AS A DATA processing equipment repairman, you know that you have the responsibility for the maintenance of complex equipment--not complex because of the individual circuits, but complex because of the vast number of circuits. Your ability to maintain this equipment depends largely upon your knowledge of the use and care of test equipment. Since you have already completed an apprentice-level training course, you have a good knowledge of the principles of test equipment. However, you must continue to work with and study your test equipment to develop a thorough understanding of its uses and capabilities.

2. Do not limit yourself to thinking of the standard pieces of test equipment such as scopes, voltmeters, and counters. Expand your knowledge of specialized test circuits as well. Specialized test circuits are not limited to auxiliary units. They also include test circuits and error indicators that are built into the data processors and function as an integral part of the equipment.

3. Electronic test equipment is designed and constructed to perform a wide variety of tests. These tests are used to determine the proper operation or alignment of electronic sets, circuits, or parts. The performance of data processing equipment depends in a large measure on the accuracy of the test equipment and on the integrity of the repairman who does the job. Without test equipment, very few electronic devices could be kept in operating condition; therefore, you must use test equipment properly.

4. A piece of test equipment can be as simple as a light bulb or as complex as the Electronic Circuit Plug-In Unit Test Set AN/GPM-50 used in the 412L Weapons System. The test equipments and circuits discussed in this chapter are limited to the ones that are now being used in the maintenance of data processors used by the Air Force. The more simple-to-use test sets are not discussed in this chapter, and no attempt is made to include theory beyond that necessary to describe the use of the test set under discussion. When you use a piece of test equipment that is new to you, always consult the technical order or the manufacturer's instruction manual on that particular piece of test equipment. This chapter covers these three main topics: (1) operating standard test equipment, (2) operating special AGE equipment, and (3) calibrating test equipment using Category I and II procedures.

8. Operating Standard Test Equipment

8-1. In this section we discuss various pieces of test equipment used in maintaining data processing equipment. The test sets described are examples to show applications. The section is broken down into areas. First we identify the controls and operation, then the applications of standard test equipment: the oscilloscope, differential voltmeter, and multimeter.

8-2. **Oscilloscopes.** The oscilloscope is as indispensable to the data processing maintenance man as the stethoscope is to the doctor. In fact, the oscilloscope is one of the most widely used test sets in the electronics career field. The uses of an oscilloscope are many, but you will use it primarily to troubleshoot and align data processing equipment. You will do this by observing and analyzing waveforms as to shape, amplitude, coincidence, and duration, and compare the waveform with those presented in technical orders for your particular data processor, which designate what waveforms are to be observed at various test points throughout the system.

8-3. Front panel controls of most oscilloscopes are very similar. Therefore, we shall review controls and their functions, using a model commonly used in data processing maintenance. Figure 60 (in the workbook) is a front view of the type 545A with a type CA plug-in unit installed. Like most test equipment, its controls are grouped into numerous sections and subsections which have specific

55

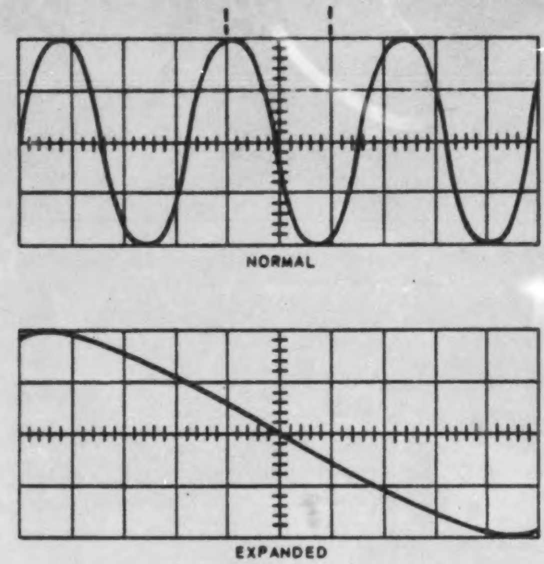


Figure 61. 5X expanded view.

functions to perform. We shall discuss these, along with controls associated within a section.

8-4. **Controls.** The front panel of the scope in figure 60 can be divided into three main areas of control: (1) the horizontal display controls, (2) the vertical position and deflection (plug-in preamplifier), and (3) the indicator controls. The other controls and inputs that do not fall in any particular area will be grouped under a title of (4) miscellaneous controls.

8-5. **Horizontal Controls.** Horizontal controls are groupings of controls located for the most part on the upper right side on the front of the oscilloscope. They include Time Base A and Time Base B and the Delay-Time Multiplier.

8-6. *Time base A.* Time base A will provide complete control of the horizontal circuits within the scope and will provide a variety of selections to cover displaying of signals from DC to 2 megahertz. It is made to work by selection from the Horizontal Display selection switch, the time base A selection. An external trigger is gated into the circuitry by use of trigger input and selection of EXT on the Triggering Mode selection switch.

a. Horizontal Display selection switch. This switch is used to select the desired sweep function. It is a three-section switch that may be set to one of three areas—time base A, time base B, or External. The 5X magnifier section of this switch, when turned on, expands the waveform that occupies the middle two divisions to occupy the entire graticule length. This provides for closer inspection of a specific display as illustrated in figure 61.

b. Triggering Mode selection switch. This switch arranges the circuits to provide the kind of triggering you need. This is the smaller outside knob, and its selections are labeled in red on the panel.

(1) AC and DC. Slowly changing waveforms work best on the AC and DC positions. In the AC position, a capacitor removes the DC component of the triggering waveform and makes triggering on the vertical signal independent of trace position. This position is suitable for signals from 20 hertz up to about 5 to 10 megahertz. The DC position is the same except that it responds to DC as well.

(2) AC LF REJECT. In the AC LF REJECT position, the circuit includes an RC filter, useful for preventing 60-hertz, or other low-frequency components, from triggering the sweep when both high- and low-frequency components are present in the triggering waveform. The low-frequency limit is about 2 kilohertz. In either of these three positions, if the Stability control is properly set, the sweep will not run unless triggered by a signal.

(3) AUTOMATIC and HF SYNC. The AUTOMATIC and HF SYNC switch positions both arrange synchronizing circuits, rather than strictly triggering circuits.

(a) AUTOMATIC. The AUTOMATIC circuit provides a free-running multivibrator having a normal repetition rate of about 50 hertz. This locks in, and runs synchronously with, recurrent triggering waveforms from 60 hertz to about 2 megahertz. The synchronized multivibrator then triggers the sweep-gating multivibrator.

(b) HF SYNC. The HF SYNC setting arranges a circuit which connects the triggering source directly to the sweep-gating multivibrator so that it can synchronize with the triggering waveform. The sweep-gating multivibrator must be free-running for this type of operation. It free-runs at advanced settings of the Stability control. It will synchronize with frequencies as high as 30 megahertz, at a sweep repetition rate up to 200 kilohertz.

c. Trigger Slope selection switch.

(1) Positive (+) selections. The + (positive) positions of the Trigger Slope switch (black knob) cause triggering to occur during the rising portion of the triggering waveform. The level may be either negative or positive.

(2) Negative (-) selections. The - (negative) positions cause triggering to occur during the falling portion of the waveform. Thus, the triggering point can be caused to occur at almost any point in the waveform.

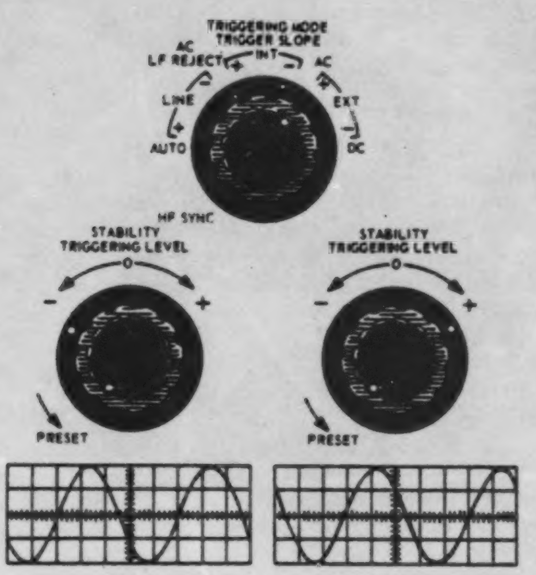

TRIGGERING MODE
TRIGGER SLOPE
AC
LF REJECT
INT
AC
LINE
EXT
AUTO
DC
HF SYNC
STABILITY
TRIGGERING LEVEL
0
-
+
PRESET
STABILITY
TRIGGERING LEVEL
0
-
+
PRESET

Figure 62. Negative and positive triggering level with + triggering slope.

(3) Source of trigger. An additional function of the Trigger Slope switch selects the source of trigger signal sources. These are:

(a) External (+ or -), where an external trigger is supplied to internal circuits to provide triggering of the display.

(b) Internal (+ or -), which triggers the scope from the waveform to be displayed.

(c) Line (+ or -), which triggers the scope from a power line voltage waveform.

d. Stability control. The Stability control adjusts bias level on the sweep-gating multivibrator near the level at which it will free-run. Three principal settings of the Stability control are used: the first setting is with the control advanced to the right, just past the point where the sweep-gating multivibrator free-runs; the second, retarded to the left about 5° or 10° left of the point where free-running ceases; and the third, retarded all the way left, to make the multivibrator inoperative.

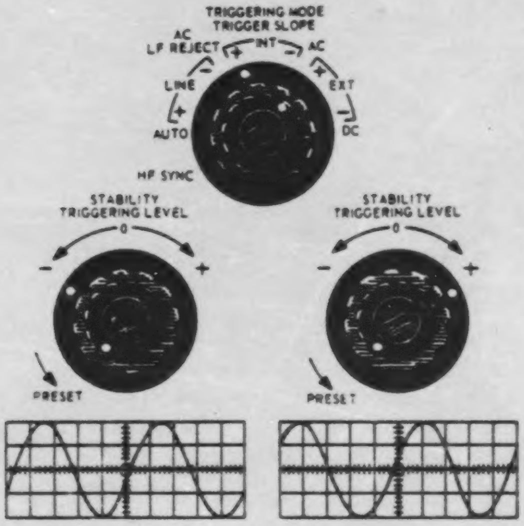

TRIGGERING MODE
TRIGGER SLOPE
AC
LF REJECT
INT
AC
LINE
EXT
AUTO
DC
HF SYNC
STABILITY
TRIGGERING LEVEL
0
-
+
PRESET
STABILITY
TRIGGERING LEVEL
0
-
+
PRESET

Figure 63. Negative and positive triggering level with triggering slope.

e. Triggering Level control. The Trigger Level control selects the point on the triggering waveform at which triggering will occur. To trigger on small signals, this control must be set near 0, or near the DC level with DC triggering. The levels are indicated on the panel as positive to the right and negative to the left. Negative positions of the Level control (as shown in fig. 62) cause triggering to occur during negative level of the triggering waveform, and positive positions cause triggering during positive levels. Reversing the Trigger Slope control inverts the polarity of the waveform, as shown in figure 63; however, the Level control reacts the same. This control is not used in the AUTOMATIC and HF SYNC positions of the Triggering Mode switch. Preset is also a function of this control. When used, it selects a predetermined DC voltage to cause triggering to occur. Refer to figure 64 and observe how the variable and preset functions are identical except that the preset is obtained by closing switch S1.

f. Time/CM control. The Time/CM control selects horizontal sweep time per centimeter; from .1 microsecond to 5 seconds may be selected. The setting of the Time/CM control determines the time base sweep speed and horizontal size on the displayed waveform.

g. Variable Time/CM control (inner knob). This control permits you to vary the sweep speed continuously between .1 microsecond and 12 seconds per centimeter. When the

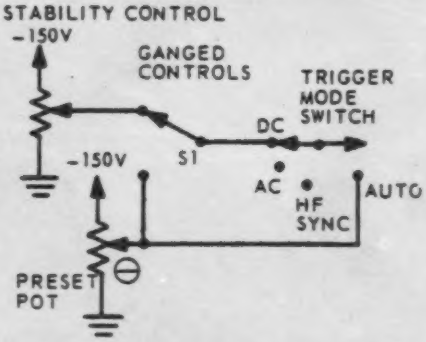

STABILITY CONTROL
-150V
GANGED CONTROLS
TRIGGER MODE SWITCH
DC
S1
-150V
AC
HF SYNC
AUTO
PRESET POT

Figure 64. Preset control.

control is in the calibrated position, the Time/CM reading is accurate. The uncalibrated position is inaccurate for determining an unknown frequency. However, the position is very useful in obtaining a desired number of pulses when frequency is not important.

8-7. *Time base B similarities and differences.* The controls under time base B have the same basic function as those of time base A. With the Horizontal Display switch in the B position, time base B may be displayed on the screen instead of time base A. Notice in figure 60 that time base B has three triggering modes—AUTO, AC, and DC—while time base A has five. Not available for time base B are the HF SYNC and AC LF REJECT triggering modes. In addition, time base B has 18 calibrated sweep speeds while time base A has 24. The Length control adjusts the sweep length between 4 and 10 centimeters.

8-8. *Delay-time multiplier.* This is a ten-turn control. When the Horizontal Display switch is in the "B" INTENSIFIED BY "A" or the "A" DEL'D BY "B" position, time base A is held inoperative until after a delay time following the triggering of time base B. This delay time is the product of the settings of the Time/CM or Delay-Time control and the Delay-Time Multiplier control. Use of this control with time base A and time base B is covered in more detail later.

8-9. **Use of Horizontal Controls.** Let's go back now and discuss the Time Per Centimeter control in a little more detail as it applies to period and frequency measurements. As a maintenance man, you will measure pulse widths, periods, frequencies, and any other events that may be a function of time. It should be relatively simple for you, as an operator, to determine the number of centimeters that the beam is deflected horizontally and then, with a little mathematics (number of centimeters times the setting of the Time Per Centimeter control), determine the time for any event associated with the displayed signal. As for frequency measurements, frequencies can be readily determined by the use of the following formula:

$$\text{Frequency} = \frac{1}{\text{time per hertz}}$$

8-10. For an example of frequency measurements, look at figure 65. Here a 50-kHz

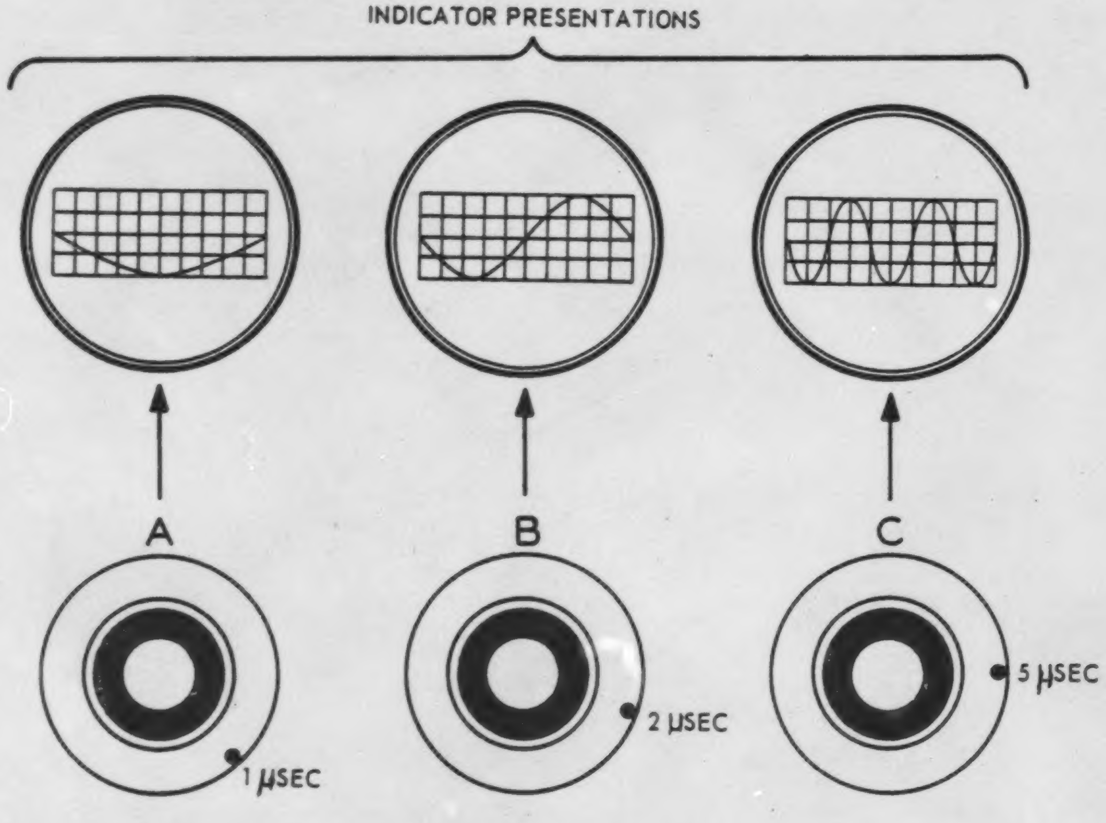


Figure 65. 50-kHz sine wave.

sine wave is an input to the oscilloscope shown in figure 60 with the Trigger Level and Trigger Slope controls set to develop sweep triggers at the 0-volt level of the negative slope. Now consider three different settings of the Time Per Centimeter control as shown in A, B, and C of figure 65. The sweep length is always 10 centimeters. Frequency determination under these conditions is as follows: The A setting of the Time Per Centimeter control is 1 microsecond; therefore, a full 10-cm sweep takes 10 microseconds. Note that 1/2 hertz occupies the full sweep. The time per hertz would thus be 20 microseconds. You can calculate the frequency by using the following formula:

$$\text{Frequency} = \frac{1}{\text{time per hertz}}$$

$$(F = \frac{1}{t})$$

$$F = \frac{1}{20 \times 10^{-6}} = 50{,}000 \text{ Hz}$$

8-11. One trouble encountered with this method of frequency determination is that it is very difficult to determine when the scope displays exactly 1/2 hertz. If you err in determining the time for a half hertz, this error is compounded by doubling the value to determine the time per hertz. When possible, you should not use settings of the Time Per Centimeter control that present less than 1 hertz.

- The B control setting, as shown in figure 65, of 2 microseconds results in a 1-hertz presentation. Here, again, it is difficult to determine when exactly 1 hertz is presented; however, this time the error is not compounded by multiplying.
- The C control setting, as shown in figure 65, of 5 microseconds results in a display of 2 ½ hertz. Here the point at which the signal crosses the zero reference line is much more definite because of the steepness of its slope; therefore, a more accurate calculation can be made.

8-12. There are several ways you can calculate the frequency in this case; the following method is recommended: 1 centimeter represents 5 microseconds; therefore, the full 10-cm sweep represents 50 microseconds (5 × 10 = 50). The time for 2 ½ hertz is then 50 microseconds, and the time per hertz is 20 microseconds ($\frac{50}{2.5} = 20$).

$$F = \frac{1}{t} = \frac{1}{20 \times 10^{-6}} = 50{,}000 \text{ Hz}$$

In practice you will find that the most accurate frequency determinations are obtained by setting the time controls for presentations of 2 to 10 hertz.

8-13. Before discussing the next subject, let's be sure you know how to determine the frequency of a waveform. In figure 66, there are three problems. We will go through figure 66,A, together, then you can complete 66, B and C.

Figure 66,A:

Step 1. We can determine that a Time/CM control setting of 5 microseconds results in a 1-hertz presentation.

Step 2. With a 5-microsecond Time/CM setting, the time for 1 hertz is 50 microseconds (5 × 10 = 50).

Step 3. Using the formula $F = \frac{1}{\text{time,}}$ we have $F = \frac{1}{t} = \frac{1}{50 \times 10^{-6}}$ or a frequency of 20,000 hertz.

8-14. Now refer to figure 66,B, and complete the following statements.

a. The Time/CM is ______________ microseconds.

b. The full 10-cm sweep represents ______________ microseconds.

c. The time for 1 hertz is ______________ microseconds.

d. The frequency of the displayed waveform is ______________ hertz.

8-15. Before checking your answers, refer to figure 66,C, and complete these statements.

a. The time for 5 hertz is ______________ microseconds.

b. The time for 1 hertz is ______________ microseconds.

c. The frequency of the displayed waveform is ______________ hertz or ______________ kilohertz.

8-16. Let's review each problem and see if your answers are correct. (Refer to fig. 66,B.)

a. 10 microseconds.
b. 100 microseconds.
c. 40 microseconds.
d. 20,000 hertz.

Figure 66,C:

a. 20 microseconds.
b. 4 microseconds.
c. 250,000 hertz or 250 kilohertz.

8-17. Use of B Sweep. The B SWEEP position of the Horizontal Display switch shown in figure 60 selects another set of circuits containing a trigger generator and sweep generator that operates similarly to the A sweep and triggering circuits. Look at the B sweep time base controls in figure 60 and note the similarity to the A sweep time base controls. Since their functions and operations

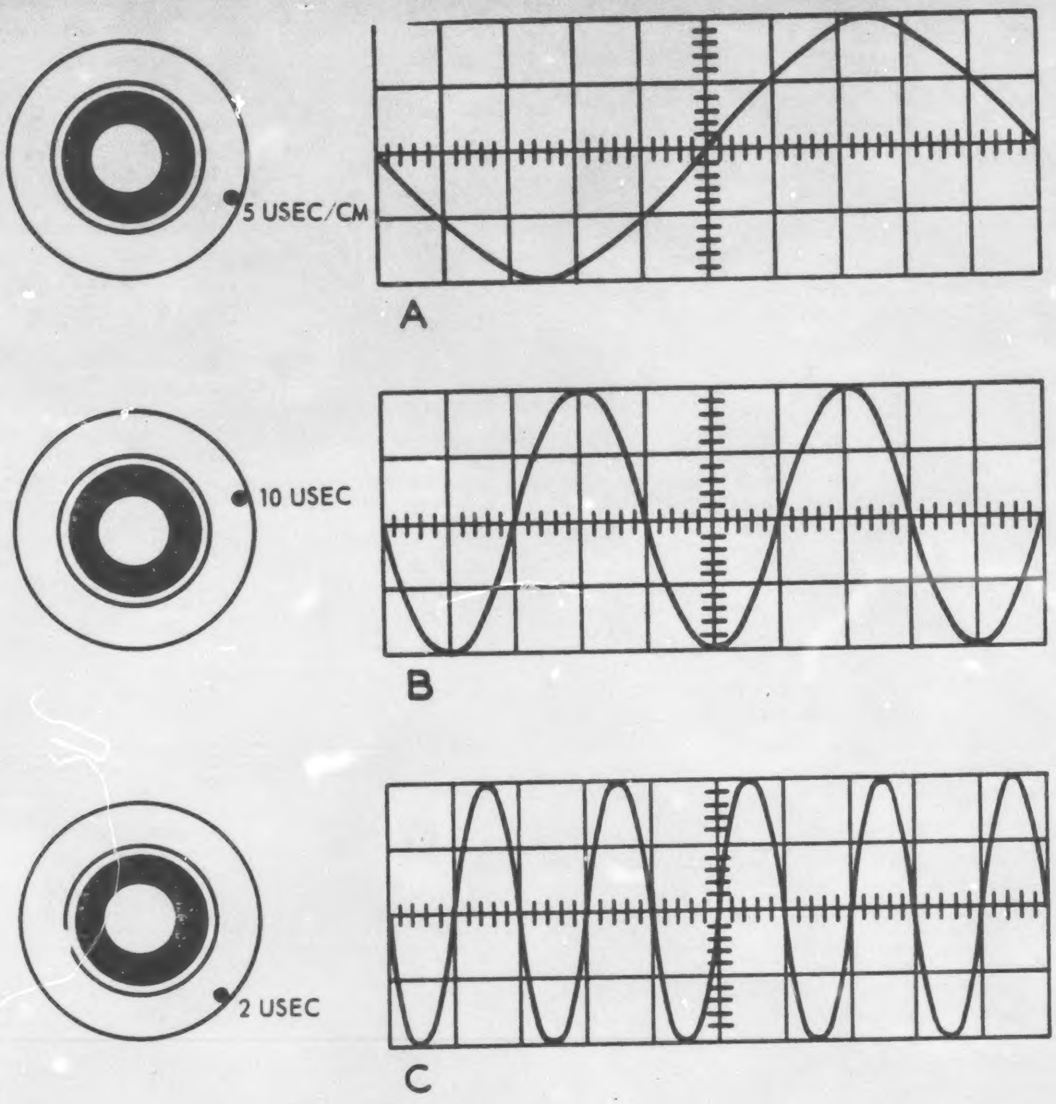


Figure 66. Sine-wave problems.

are similar, it is not necessary to cover them again.

8-18. *"B" INTENSIFIED BY "A."* Until now we have discussed a single sweep function with its associated triggering circuits. Used alone, the addition of another sweep generator and its associated circuits adds nothing to the capability of an oscilloscope. However, when one sweep is used to modify the other sweep, much is added to the scope's capabilities.

8-19. The two sweep generators in the oscilloscope can be triggered by the same synchronizing signal or by separate signals. Regardless of the trigger source, there are two sweep voltages and two unblanking voltages that can be applied to the indicator. This particular scope uses the unblanking voltage of the A sweep to intensity-modulate a portion of the B sweep. The intensified portion may be expanded to give you an enlarged presentation.

8-20. In the "B" INTENSIFIED BY "A" position of the Horizontal Display switch, the B sweep generator functions normally. When triggered, it develops a sawtooth horizontal sweep voltage and a positive unblanking signal. These signals are coupled to the indicator, and a normal sweep pattern begins. The sawtooth sweep voltage is also sent to a trigger pickoff circuit. The trigger pickoff circuit is set to produce a trigger pulse when the B sweep sawtooth voltage rises to some predetermined (pickoff) point. The bias on the pickoff circuit can be varied so that the pickoff point can occur at any desired amplitude of the sawtooth voltage. In the oscilloscope shown in figure 60, the pickoff point is controlled by the Delay-Time Multiplier control. This is the second control from the bottom on the right-hand side. Regardless of the slope of the sweep voltage, it always takes the same voltage to deflect the beam 1 centimeter; therefore, the delay control which sets the voltage of the pickoff point can be calibrated in centimeters. The delay time (the time between the beginning of the sweep and the start of the intensified portion) is then calculated by multiplying the setting of the "B" Time Per Centimeter control times the number of centimeters on the Delay-Time Multiplier control.

8-21. Now let's see how this sweep intensification works, using a practical example. Look at figure 67 (in the workbook). Signal A is a 40-kHz input that is applied as a vertical input and as an input to trigger generator B. Time base B controls are set as follows:

- Triggering Source to INT.
- Triggering Level to 0.
- Trigger Slope to positive.

Signal B in figure 67 shows the output of trigger generator B. Note that a trigger is produced when the input signal (signal A in fig. 67) reaches point X. This trigger is fed to the B sweep generator. It initiates a sawtooth sweep voltage (signal C) and a positive unblanking pulse (signal D). The sawtooth sweep voltage and the unblanking pulse are coupled through appropriate circuits to the indicator to unblank and sweep the electron beam horizontally across the scope.

8-22. Let's assume that the A sweep generator is set for a 5-microsecond-per-centimeter sweep, the Stability control is fully clockwise, and the B sweep generator is set for a 20-microseconds-per-centimeter sweep. Also, assume that the indicator beam is deflected 1 centimeter for every 15 volts of sweep signal (signal C). The operator has set the Delay-Time Multiplier control to 3 ⅓ centimeters, which means that the delay pickoff circuit will produce a trigger (signal E, fig. 67) when the sweep has moved 3 ⅓ centimeters. Now let's look a little closer at how the pickoff trigger is produced. The sweep voltage (signal C) is fed to the pickoff circuit. Remember that the delay time was to be 3 ⅓ centimeters. If horizontal deflection takes 15 volts per centimeter, then 3 ⅓ centimeters require 50 volts. What the delay control actually does is set the pickoff circuit bias so that the sawtooth (signal C) must rise to 50 volts before the pickoff circuit is triggered. Now the trigger from the pickoff circuit (signal E) is fed to the A sweep generator. The A sweep generator is triggered and produces a sawtooth sweep voltage (not shown in fig. 67) and an unblanking pulse (signal F, fig. 67). The indicator circuits combine the A and B sweep unblanking pulses (signal G, fig. 67). This combining of the unblanking pulses results in an increase in CRT current, thus intensifying the trace for a period equal to the unblanking pulse time of sweep A (pattern H of fig. 67).

8-23. Look again at the A sweep unblanking pulse in figure 67 (signal F). Note that it lasts for 50 microseconds. Now, if the Time Per Centimeter control is set to 5 microseconds per centimeter as previously stated, then the A sweep generator produces a sawtooth of the same amplitude as the B sweep sawtooth, but in a shorter time:

- A sweep time = 5 microseconds/cm × 10 cm = 50 microseconds
- B sweep time = 20 microseconds/cm × 10 cm = 200 microseconds

In this application, the A sweep sawtooth is not used but its unblanking pulse is used. The A sweep unblanking pulse is equal in duration to the A sweep sawtooth, so its duration must also equal 50 microseconds. The indicator sweep is the result of the much slower B sweep signal, so the 50-microsecond A sweep unblanking pulse intensifies the B sweep for only 2 ½ centimeters (50 microseconds/20 microseconds per centimeter = 2 ½ centimeters).

8-24. Let's see now if you can solve some problems on the "B" INTENSIFIED BY "A" sweep function. Figure 68 is a display obtained with the Horizontal Display switch in the "B" INTENSIFIED BY "A" position. The "A" Time/CM control is set to 10 microseconds/cm, and the "B" Time/CM is set to 20 microseconds/cm. Using the information given and figure 68, solve the following problems:

a. The setting of the Delay-Time Multiplier control in centimeters is ____________ cm.

b. The time between the beginning of the

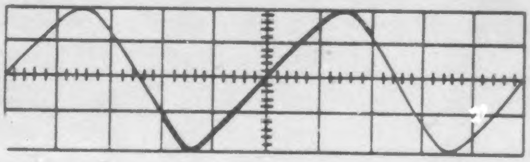


Figure 68. Intensified sweep problem.

sweep and the start of the intensified area is ______________ microseconds.

c. The duration of the A sweep unblanking pulse is ______________ microseconds.

8-25. In *a* above your answer should have been 3 centimeters. This is the time between the beginning of the sweep and the intensified portion, which is controlled by the setting of the Delay-Time Multiplier switch.

8-26. The "B" Time/CM setting is 20 microseconds. The time between the beginning of the sweep and the start of the intensified sweep is 3 centimeters. Therefore, 3 cm × 20 microseconds/cm = 60 microseconds—the answer for *b*.

8-27. The "B" Time/CM setting is 20 microseconds/cm. The sweep in figure 68 is intensified for 4 cm; thus, 20 microseconds/cm × 4 cm = 80 microseconds, the duration of the A sweep unblanking pulse—the answer for *c*.

8-28. Now let's summarize what we know about the "B" INTENSIFIED BY "A" function.

- The B sweep is triggered and functions just like the A sweep.
- The B sweep sawtooth voltage is fed to a pickoff circuit that produces a trigger for the A sweep generator at a time determined by the Delay-Time Multiplier control.
- The A sweep unblanking pulse intensifies a portion of the B sweep.
- You can select the portion of the B sweep that you wish to intensify by varying the setting of the Delay-Time Multiplier control.

8-29. *Delay-time frequency measurement.* There are times when you may wish to use this intensification principle to determine the frequency of the signal being displayed, the period or pulse width of the signal, or the signal rise time. To do this, reduce the setting of the A sweep Time Per Centimeter control until the A sweep unblanking pulse is so short that the intensified portion of the trace appears as a small intensified dot.

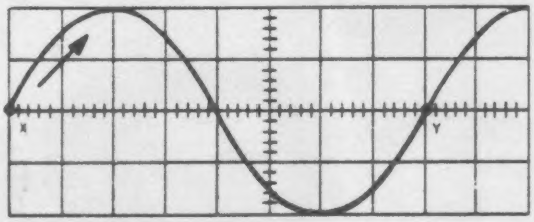


Figure 69. Measuring time with the intensity dot.

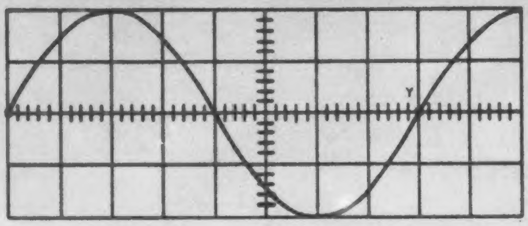


Figure 70. Measuring time problem 1.

8-30. Now look at figure 69. This figure shows an example of how the intensified dot can be used. In figure 69 the frequency of the displayed signal can be determined in the following manner:

- First, place the dot at point X by setting the Delay-Time Multiplier control to zero centimeters.
- Rotate the Multiplier control until the dot moves to point Y, a distance that represents 1 hertz, and record the control setting.
- Subtract setting X from setting Y (the result in this case should equal setting Y, since setting X was zero). Now multiply this difference by the setting of the "B" Time Per Centimeter control to obtain the time per hertz. Convert the time per hertz to frequency by formula $F = \frac{1}{t}$.

8-31. For example, let's say the "B" Time/CM control is set to 5 microseconds/cm. The setting of the Delay-Time Multiplier control is 8 centimeters when the intensified dot is positioned at Y in figure 70. What is the frequency of the signal in figure 70?

8-32. First we multiply the Multiplier control setting (8 cm) by the "B" Time/CM setting (5 microseconds/cm). Thus, we have 8 cm × 5 microseconds/cm = 40 microseconds, the time for 1 hertz. The frequency then is 25,000 hertz.

8-33. You may be thinking that it's not necessary to use the Delay-Time Multiplier control to determine the frequency. In this case it is not because the signal completes 1 hertz at exactly 8 centimeters. Now refer to figure 71. In this illustration it is difficult to tell at exactly what point in time the hertz is complete. By setting the Delay-Time Multiplier control with the dot at point Y, the time for 1 hertz can be read directly from the multiplier dial; reading, 94.1 = 9.41 centimeters.

8-34. You may use the same procedure to determine the width of a rectangular pulse as shown in figure 72,A, or the time between pulses as shown in figure 72,B. You may

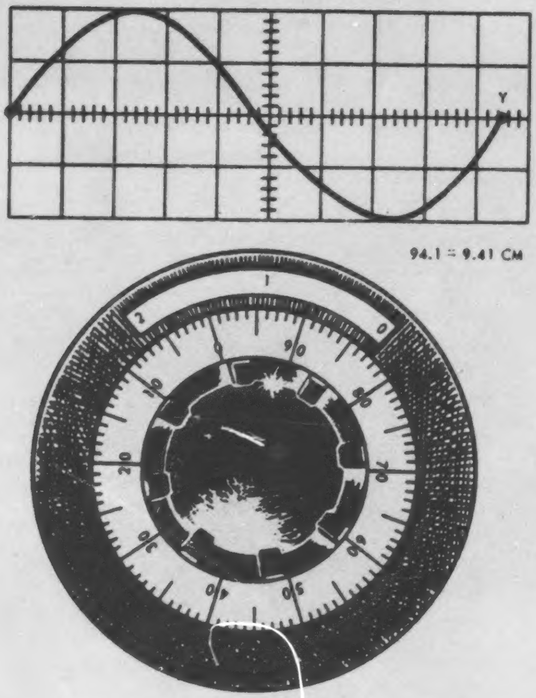


Figure 71. Measuring time problem 2.

wonder why it may be necessary to do this when you can simply count the number of centimeters directly off the face of the indicator. True, you can count them but you cannot be as accurate as possible. Therefore, by using the micrometer type Delay-Time Multiplier control you can obtain the exact values. These are only a few examples of how the intensified sweep can be used; however, in your day-to-day performance of maintenance, you will find many other useful applications.

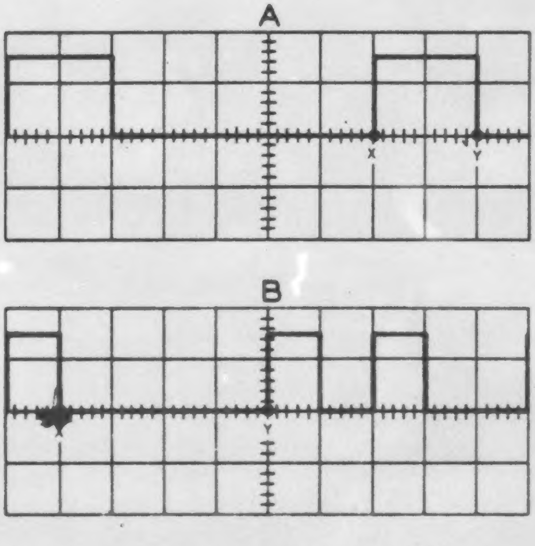


Figure 72. Measuring pulse width problem 3.

8-35. *"A" DELAYED BY "B."* You will find it convenient at times to be able to obtain an expanded view of one particular part of a display. This is probably the most important application of the intensified sweep. This can be done by intensifying the area you wish to expand and switching the Horizontal Display control (fig. 60) to the "A" DELAYED BY "B" position.

8-36. The "A" DELAYED BY "B" sweep function is relatively simple. The only difference between it and the "B" INTENSIFIED BY "A" is that the indicator receives only the A sweep unblanking pulse and the A sweep sawtooth. The B sweep circuits are triggered just as they were in the "B" INTENSIFIED BY "A"; however, the B sweep outputs are not used by the indicator. The B sweep sawtooth triggers the pickoff circuit, which in turn triggers the A sweep. This happens at a time when the part of the input signal to be intensified is present at the vertical plates. The A sweep sawtooth and A sweep unblanking pulses are coupled to the indicator circuits and allow the intensified area to be displayed over the entire 10 cm.

8-37. Figure 73 (in the workbook) shows more clearly what happens. The intensified sweep shown in figure 73,F, is obtained while the Horizontal Display switch is in the "B" INTENSIFIED BY "A" position. The Horizontal Display switch is then switched to the "A" DELAYED BY "B" position. The very next trigger received results in the generation of a B sweep sawtooth (fig. 73,B) and a B sweep unblanking pulse (fig. 73,C). The B sweep unblanking pulse is not used. However, the B sweep sawtooth is fed to the pickoff circuit, and when it rises to the pickoff point (fig. 73,B), the A sweep is triggered. The A sweep sawtooth (fig. 73,D) and the A sweep unblanking pulse (fig. 73,E) are coupled to the indicator. Thus, the intensified area between X and Y of figure 73,F, is displayed across the entire face of the indicator, as shown in figure 73,G.

8-38. *Intensity modulation.* The intensity-modulation principle can also be used to compare parts of a serial pulse train. Look at the display in figure 74,A. If you want to compare pulse A and pulse B, the best way is to superimpose one upon the other. Let's see what steps are necessary to do this with the

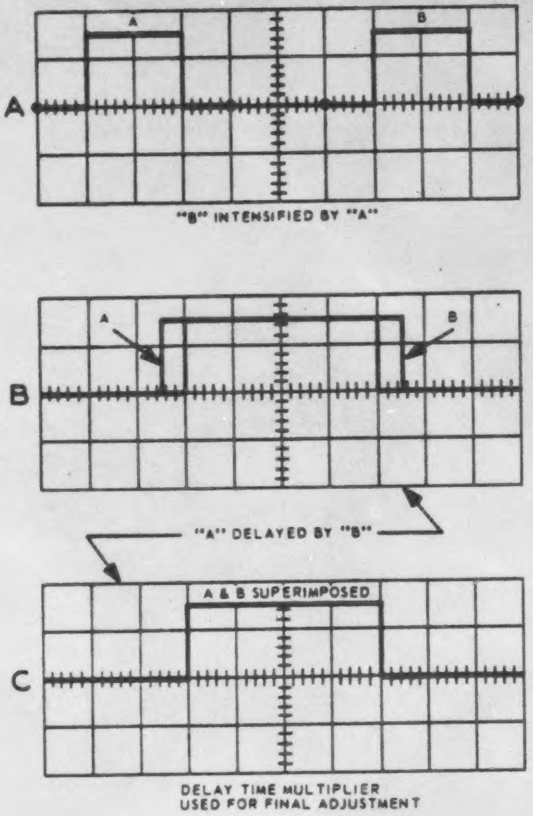


Figure 74. Pulse comparison.

oscilloscope shown in figure 60:

- Set the Horizontal Display switch to the "B" INTENSIFIED BY "A" position and adjust the A Time/CM and the Delay-Time Multiplier controls until pulse B is intensified.
- Connect a small capacitor (approximately 100 micromicrofarads) between the B sweep unblanking pulse (fig. 60, + GATE B jack) and the pickoff trigger output jack (fig. 60, DEL'D TRIG jack).

8-39. When the B sweep unblanking pulse starts, it will be coupled via the DEL'D TRIG jack to the A sweep generator. The A sweep generator is triggered and its unblanking pulse will intensify the pulse A area on the indicator. The pickoff circuit was already set to trigger the A sweep, so the pulse B area will be intensified. Now think about what is happening. Each B sweep triggers the A sweep twice, once at the beginning of the sweep and once at the pickoff point. Now switch the Horizontal Display switch to the "A" DEL'D BY "B" position. The first time the A sweep is triggered, it displays pulse A, and the second time it is triggered, it displays pulse B. This display is shown in figure 74,B, with the two pulses not quite matched. A slight adjustment of the Delay-Time Multiplier control will move pulse B from where it is shown in figure 74,B, and position it directly over pulse A as shown in figure 74,C.

8-40. The oscilloscope shown in figure 60 is capable of two other sweep applications that are not a function of the dual-sweep generator principle, so let's take a look at them.

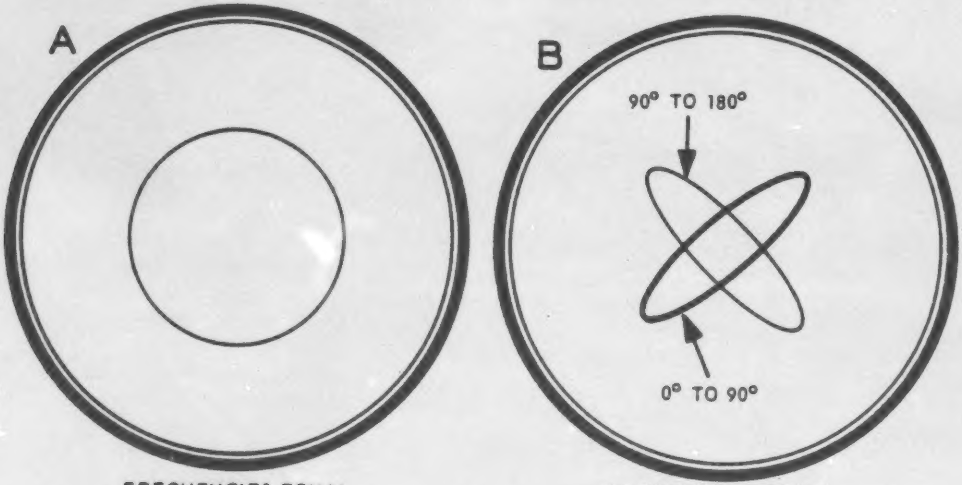
8-41. Use of "A" Single Sweep. Look again at figure 60 and note the Horizontal Display switch position that is labeled "A" SINGLE SWEEP; also observe the RESET button above and to the right of the display switch. With the switch in this position, a single sweep (one time across the scope) can be obtained each time the RESET button is depressed. Your eyes and mind can obtain very little knowledge from seeing a signal for so short a time; however, with a camera and high-speed film, a picture can be taken of this single trace. This picture then becomes a permanent record of the function displayed, and the function can be analyzed at your leisure.

8-42. Use of External Sweep. Most oscilloscopes have provisions for the direct application of an external signal to the horizontal amplifiers. The External sweep function is especially applicable if you are to compare the phases of two sine waves. One signal is applied to the vertical input and the other signal is applied to the horizontal circuits via the Horizontal Input jack (fig. 60, just to the right of the Horizontal Display switch). With the Horizontal Display switch in the X1 position, the horizontal input signal is fed directly to the horizontal amplifiers. In the X10 position, the horizontal input signal is attenuated by a factor of ten before application to the horizontal amplifiers. Figure 75,A, shows the display obtained when applying two sine waves of equal frequency but 90° out of phase. This pattern and the other patterns of figure 75 are based on equal horizontal and vertical deflections (the vertical input attenuator must be adjusted to make the vertical deflection equal to the horizontal deflection). An oval pattern such as shown in figure 75,B, is obtained when the phase difference is between 0° and 90° or between 90° and 180°. A single line presentation as shown in figure 75,C, is obtained when the signals are in phase or 180° out of phase. Figure 75,D, is the display obtained when the horizontal and vertical input signals are not of the same frequency. These are only the basic patterns, but they are the ones most important to you. For further detail on these patterns, refer to TO 31-1-141, Chapter 10, Section III.

8-43. **Vertical Controls.** Vertical amplifiers in all type 545 scopes have separate input-amplifier units that can be plugged into the main unit. The various plug-in units provide a variety of pass bands and sensitivities, a differential amplifier, and a channel-switching unit to provide dual-trace presentations.

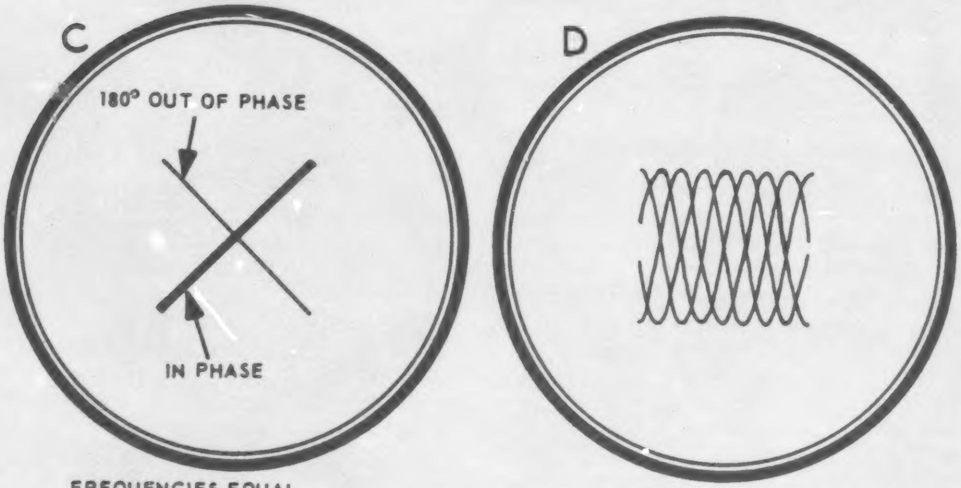
8-44. *Plug-in unit.* The oscilloscope shown in figure 60 has a type CA dual-trace plug-in unit installed. This plug-in unit is just one of many that can be installed in the oscilloscope. All of these plug-in units provide preamplification and/or attenuation of the vertical input signal. Other functions performed by the various plug-in units are as follows:

- Vertical positioning of the display.
- Acceptance of two vertical input signals.
- Display of either of two vertical input signals separately.
- Alternate display of two vertical input signals on separate baselines.
- Chopped display of two input signals alternately selected and displayed on separate baselines while the sweep is in progress.



FREQUENCIES EQUAL
90° OUT OF PHASE

FREQUENCIES EQUAL
PHASE RELATION
0° TO 90° OR 90° TO 180°



FREQUENCIES EQUAL
IN PHASE OR 180° OUT OF PHASE

FREQUENCIES
NOT EQUAL

Figure 75. Lissajous patterns.

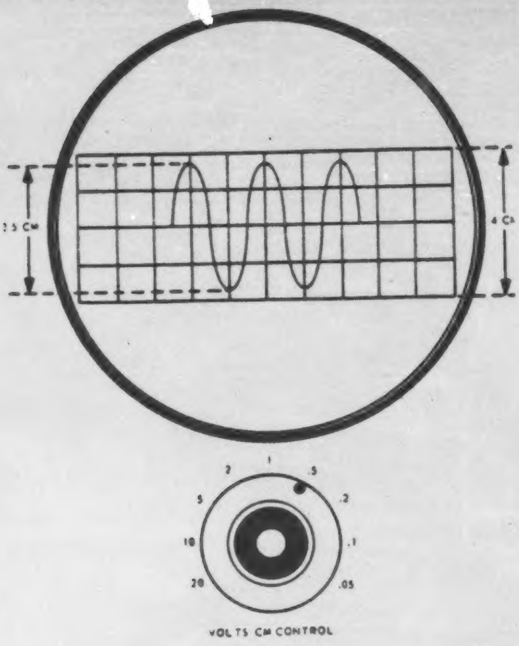


Figure 76. Volts/CM control.

- Display of the algebraic sum of two vertical input signals.

8-45. Choosing the plug-in unit you wish to use is dependent on the frequency response necessary, pulse characteristics, and the type of display that provides the most convenient analysis of the signal. You will learn of many needs through practical experience. To aid you in making the proper choice, let's discuss the plug-in unit functions that are listed above.

8-46. *Vertical positioning.* All plug-in units have front panel vertical positioning controls. This control references the input signal so that it can be moved vertically on the indicator. The input signal is applied to a paraphase amplifier, which produces two outputs that are 180° out of phase. These two signals are amplified and each is applied to a vertical plate. One signal is applied to the upper deflection plate to produce a push-pull vertical deflection. The Vertical Position control varies the DC reference level that these two signals ride and thus positions the signal in the vertical plane.

8-47. *Input attenuation.* All vertical input signals are applied to an input attenuator network. The amount of attenuation is a function of the Volts/CM control (see fig. 60 in the workbook). The positions of this control indicate the amplitude of the input voltage necessary to deflect the beam 1 centimeter vertically; thus, if the switch is in the 5-volt position, an input signal will deflect the beam 1 centimeter for every 5 volts amplitude. Look at the Volts/CM control and the display shown in figure 76. The signal displayed occupies 3.5 cm vertically, and the Volts/CM control is set at the .05-volt position. You can calculate its peak-to-peak voltage amplitude as follows:

Volts/cm × cm of deflection = amplitude (peak to peak)

$$0.5 \times 3.5 = 1.75 \text{ volts}$$

8-48. *DC and AC level measuring.* To measure the amplitude of a DC signal, you first set the sweep baseline to some logical reference level before applying the signal. You use the Vertical control to do this. When you apply the signal, you need only determine the distance in centimeters that the baseline moved, and then multiply this figure by the setting of the Volts/CM control. An example of a DC voltage measurement is shown in figure 77. Note where the baseline was set prior to the application of the input signal. If you count the number of centimeters, you

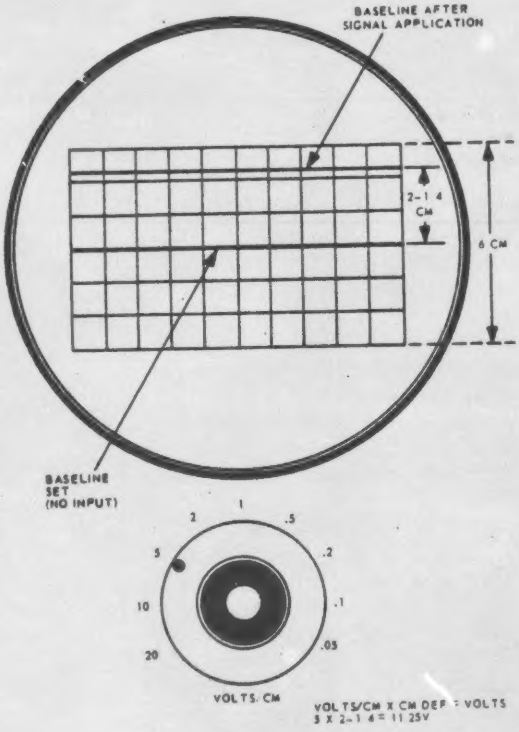


Figure 77. DC level measuring.

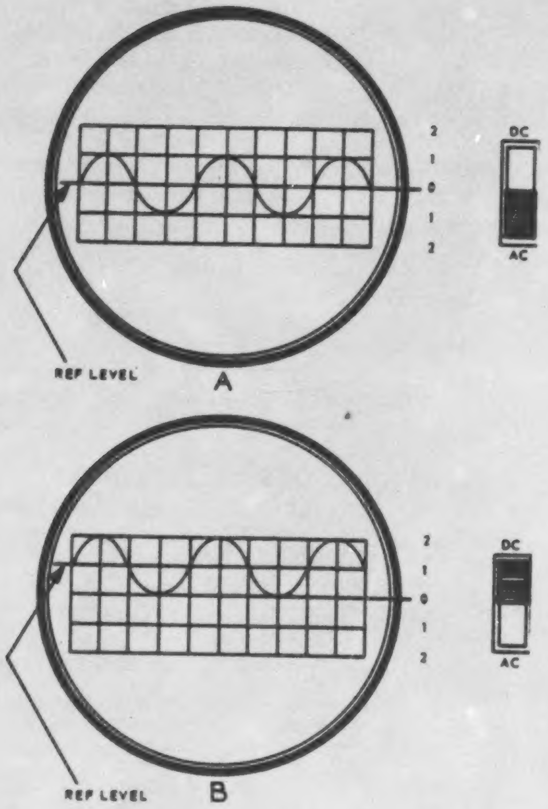


Figure 78. DC reference of an AC signal.

can see that the input signal moved the baseline 2¼ centimeters. The Volts/CM control in the figure is set to the 5-volt position; therefore, the amplitude of the DC input equals 11.25 volts (5 × 2¼ = 11.25).

8-49. You may at times be required to determine the DC reference level of an AC signal. To do this, place the AC-DC switch in the AC position. With the Vertical Position control, set the signal to some reference level. Place the AC-DC switch to the DC position, and determine the number of centimeters that the reference level shifted. In figure 78,A, the signal is shown set to a zero reference level with the AC-DC switch in the AC position. Figure 78,B, shows that the reference level shifted 1 centimeter when the switch was set to the DC position. The DC reference voltage of this signal can be determined by multiplying the setting of the Volts/CM control by 1 centimeter. If the Volts/CM control was set to its 20-volt position in the example in figure 78, the DC reference level would be: 1 cm × 20 volts/cm = 20 volts.

8-50. *Dual trace.* The principles discussed thus far apply to all types of preamplifiers. In dual-trace preamplifiers (the one shown in fig.

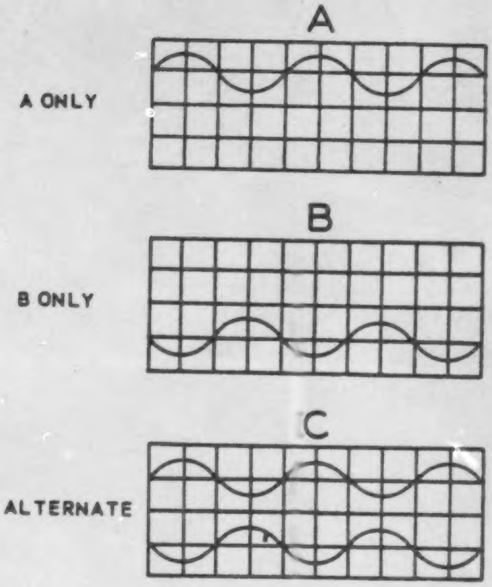


Figure 79. Dual trace, alternate mode.

60) these functions are duplicated and, in addition, there is an input attenuator and a vertical control for both the A and B sections of the preamplifier. In addition to dual controls, the dual-trace plug-in unit has two vertical input jacks and a switching multivibrator. The switching multivibrator and its associated circuits are used to alternately select one of the two vertical inputs on a time-sharing basis for application to the vertical amplifiers.

8-51. If you wish to compare two signals for phase, amplitude, shape, or any other reason, connect one input to the B section and the other input to the A section (see fig. 60). For a two-sweep comparison, you perform the following setup procedure:

- Place the Mode switch (see fig. 60) in the "A" ONLY position and adjust the A vertical positioning and the A attenuator controls until the presentation occupies the upper half of the display area (see fig. 79,A).
- Place the Mode switch in the "B" ONLY position and adjust the B vertical positioning and B attenuator controls until the B input occupies the lower half of the display area (see fig. 79,B).
- Place the Mode switch in the ALTERNATE position, and the dual-sweep display shown in figure 79,C, is obtained.

8-52. With this setup, the A vertical input signal triggers the sweep circuits, is coupled to the vertical plates, and is displayed. When the first sweep is completed, the switching multivibrator in the plug-in unit is triggered. The output of the switching multivibrator is then used to select the B vertical input. The next sweep displays the B vertical input signal. This switching action is repeated at the end of each sweep. If you wish to use this type of display to check the phase relationship of two signals, use an external trigger source of known relationship to the signals under test. Internal triggering should not be used because each signal would trigger its own sweep and the phase relationship could not be checked.

8-53. In the CHOPPED mode of operation, the multivibrator in the plug-in unit switches the vertical inputs continuously as the indicator is swept. If two sine waves that are equal in frequency but opposite in phase (as shown in fig. 80,A) are applied as vertical A and B inputs, a display similar to the one shown in figure 80,C, is obtained. The output of the switching multivibrator is shown in figure 80,B. The A input is displayed each time the output of the multivibrator is at its high level, and the B input signal is displayed each time the output of the multivibrator is at its lower level. The resultant display is shown in figure 80,C.

8-54. *DC balance.* The need for adjustment of the DC BAL control is indicated by a vertical shift in the position of the trace as the Variable Volts/CM control is rotated. This adjustment is not difficult and can be done as follows:

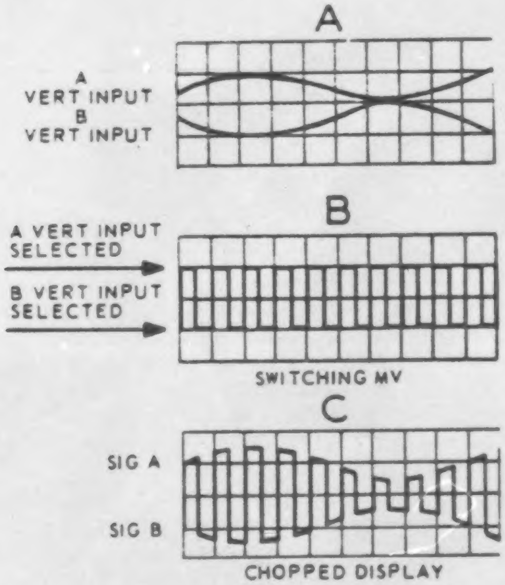


Figure 80. Dual trace, chopped mode.

- Adjust the oscilloscope controls for a free-running trace with no input signal.
- While rotating the Variable Volts/CM control back and forth, adjust the DC BAL control until the trace position is no longer affected by the Variable Volts/CM control.

8-55. *Gain adjust.* This adjustment determines the gain of the vertical amplifier and therefore the calibration of the Volts/CM switch. To make the adjustment, set the oscilloscope controls as follows:

- Triggering Mode to AUTO.
- Trigger Slope to + INT.
- Horizontal Display to A position.
- Time/CM to 1 millisecond.
- Preamp Mode selector switch to desired channel.
- Volts/CM of selected channel to .05 volt.
- Variable Volts/CM control to calibrated.
- Amplitude calibrator to .1 volt.

8-56. Now connect a lead from CAL OUT to the input jack on the selected channel. Adjust the Focus, Intensity, Astigmatism, and Position controls for a suitable trace and, finally, adjust the GAIN ADJ on the selected channel for a deflection of exactly 2 centimeters.

8-57. We stated previously that the choice of plug-in units for a particular application is dependent on many factors—factors that you will learn through continued use of the oscilloscope in the performance of day-to-day maintenance. Sometime, after you have attained your 7 level, you may be called upon to set up a maintenance shop, and you will have to decide what plug-in units your shop will need to best accomplish the assigned tasks. When this happens, you will have to apply principles learned in this CDC plus knowledge acquired on the job in making the selection. Before leaving the oscilloscope and going on to other test sets, let's discuss built-in calibration and indicator control circuits.

8-58. **Use of Square-Wave Calibrator.** In the performance of your job, there are many times when you must measure signal levels and signal excursions. Logic gating circuits make up a large part of your data processing equipment. The inputs to these gates are, for the most part, either DC levels, rectangular pulses, or square waves. In displaying these signals to see if they meet proper specifications, it is necessary to know that your scope is properly calibrated. There are two calibration check procedures that you must perform frequently. These are:

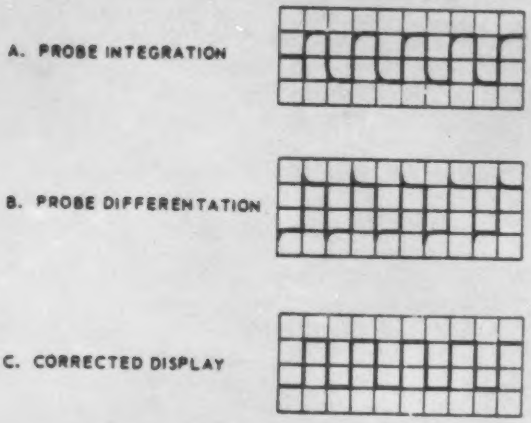


Figure 81. Adjusting the attenuator probe.

- Volts per centimeter.
- Attenuator probe.

8-59. To perform these checks, you will need a standard that can provide a square wave of known amplitude. In the case of the oscilloscope shown in figure 60, such a source is provided as a built-in feature. This circuit is called the amplitude calibrator. Its control and output jacks are located in the lower right corner of the front panel (see fig. 60). The various positions on the calibrator control provide, at the CAL OUT jack, a square-wave signal ranging from 0.2 millivolt peak to peak to 100 volts peak to peak. This output can be applied as a vertical input to determine whether the Volts/CM control is accurately calibrated. After you have checked the Volts/CM control and found it to be accurate, the attenuator probes can be placed between the CAL OUT jack and the Preamp Input jack to determine their accuracy.

8-60. When checking the attenuator probes, it is also necessary to check them to see if they cause any differentiation or integration of the input signal. If, when the CAL OUT is connected directly to the vertical input, a perfect square wave is presented on the oscilloscope indicator, but distortion is noted with the probe in the line, then an adjustment of the probe is necessary. Two common types of probe distortion are shown in figure 81, A and B. The distortion shown in figure 81,A, is due to integration, and that shown in figure 81,B, is due to differentiation. This distortion can usually be eliminated by adjusting the capacitor within the probe until the display appears as shown in figure 81,C. There is no set schedule for performing these calibrations, but you will find it good practice to check your scope in this manner before each use of the probes.

8-61. **Indicator Controls.** There are four front panel controls associated with the indicator of the oscilloscope shown in figure 60. The Scale Illum controls the intensity of a light that illuminates the centimeter markings on the etched scale in front of the indicator face. The Focus and Astigmatism controls are used together to obtain a clearly defined horizontal trace across the face of the indicator. The Intensity control sets trace brightness by varying the emission of the indicator cathode. Once set, the Scale Illum, the Focus, and the Astigmatism controls will usually need no readjustment; however, the Intensity control may need resetting for each new signal measured. This is due to the fact that the illumination of the trace is a function of both the strength of the electron beam and the frequency of the sweep. It may also be necessary to adjust the intensity when you wish to look at the leading and trailing edges of pulses that have very short rise and fall times. It is a good practice to turn the intensity down when you leave your oscilloscope for extended periods because a high-intensity beam will burn the coating on the indicator face.

8-62. **Differential Voltmeter.** The differential voltmeter is a compact, highly accurate instrument designed for precise measurement of DC voltages. It may be used as a vacuum-tube voltmeter, as a differential DC voltmeter, or as a megohmmeter for measurement of high resistance. It is possible to make precise measurements of stable voltages, or to observe and measure voltage excursions about some nominal value.

8-63. When used as a differential voltmeter, the voltmeter operates on the potentiometric principle wherein an unknown voltage is measured by comparing it against an adjustable known reference voltage, and the difference is read on a sensitive null detector. When zero displacement current flows in the null detector, the unknown voltage is exactly equal to the known voltage. When the meter is zero, the unknown voltage value can be read directly from the dials.

8-64. There are several models of the differential voltmeter. The one you use may be a model 800 or 801 series; however, the operation and the applications are basically the same. The voltmeter shown in figure 82 (in the workbook) and discussed in the study is the model 801B.

8-65. **Preliminary Setup.** As with other test sets you use, there are some preoperation checks to be made before making any measurements. For example, if an unknown volt-

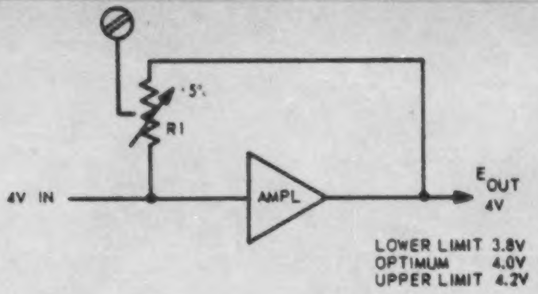


Figure 83. DC amplifier.

age is to be measured, you should always set the Range switch to the highest range position. This, of course, is to prevent overload and possible damage to the instrument. To assure accurate readings, make sure that the meter is zeroed before it is turned on. The adjustment screw on front of the meter case is for this purpose.

8-66. Now let's consider the differential voltmeter controls, what they do, and how they are used by referring to figure 82 and studying the following paragraphs.

8-67. *Range.* This control permits selection of highly regulated reference source voltages of 500, 50, 5, and 0.5 volts. When measuring unknown voltages, the selection should be 500. If the voltage is known approximately, 40 volts for example, the selection then would be the next higher position, 50 volts.

8-68. *Null switch.* This switch, when in the VTVM position, is used for selecting an internal calibrated multirange VTVM which is used as a conventional VTVM for determining the approximate value of an unknown voltage. It can also be used as a calibrated null detector for measuring the difference between an unknown voltage and a known voltage derived from the 5-decade calibrated attenuator.

8-69. *Voltage dials.* These dials are labeled A through E and are preset to zero. These controls consist of a calibrated 5-decade precision attenuator for dividing the internal reference voltage down to the exact level of the unknown voltage.

8-70. *Calibration knobs.* The meter calibration check should be made after the instrument has warmed up for at least 10 minutes. To calibrate the model 801B shown in figure 82, turn the spring-loaded Operate switch to the CALIBRATE position. Then adjust the CALIBRATE knob for zero—no deflection of the meter needle. The CALIBRATE control knob adjusts an internal 500-volt reference supply.

CAUTION:

If you are using the model 801 differential voltmeter and wish to recalibrate the instrument, follow this rule: "NEVER CHECK CALIBRATION WITHOUT FIRST DISCONNECTING THE VOLTAGE BEING MEASURED FROM THE PLUS (+) BINDING POST." The reason for this is to prevent a momentary surge/impression of approximately 500V or 450 microamperes on the voltage source being measured. This overload could cause damage to the circuit being measured and to the meter. A charge on two capacitors within the meter will cause the meter to be inoperative until the capacitors discharge; usually this is only a matter of minutes.

Now that we have explained the preliminary control settings and calibration of the meter, let's analyze some of the uses of the meter.

8-71. **Measurement of DC Voltages.** We already know from reading the introduction that the meter can be used as a VTVM and a differential meter. The following few paragraphs illustrate the meter used as a VTVM and difference meter.

8-72. *Using the meter as a VTVM.* The first step in using this meter is to determine the approximate voltage. This is done as follows:

- Set Range switch to 500 position; Null switch to VTVM position; and connect the voltage which is to be measured to the positive and negative binding posts.
- If the meter needle deflects to the left, the polarity is wrong and the connections should be reversed by changing the Polarity switch.
- Set the Range switch to the lowest range which will give an on-scale reading. For example, if the voltage is 3.5 volts, the Range switch should be set to 5.

8-73. We have now determined the approximate value of the voltage. To determine the precise value, proceed as follows: Refer to figure 83 which is the DC amplifier circuit. This circuit is designed to provide a constant DC voltage output with a given input voltage. Notice that the Gain control shows a gain variation of ±5% from the reference voltage. For this analysis we will apply 4 volts at the input. First, we will measure the precise output. Then we will use the meter to set the output so that the amplifier has a gain of unity.

8-74. By connecting the meter as shown in figure 84 and determining the approximate range as 4 volts with the Null switch in the VTVM position, Range at 5V, and switches A, B, C, D, and E at 0, we are now ready to determine the exact voltage output:

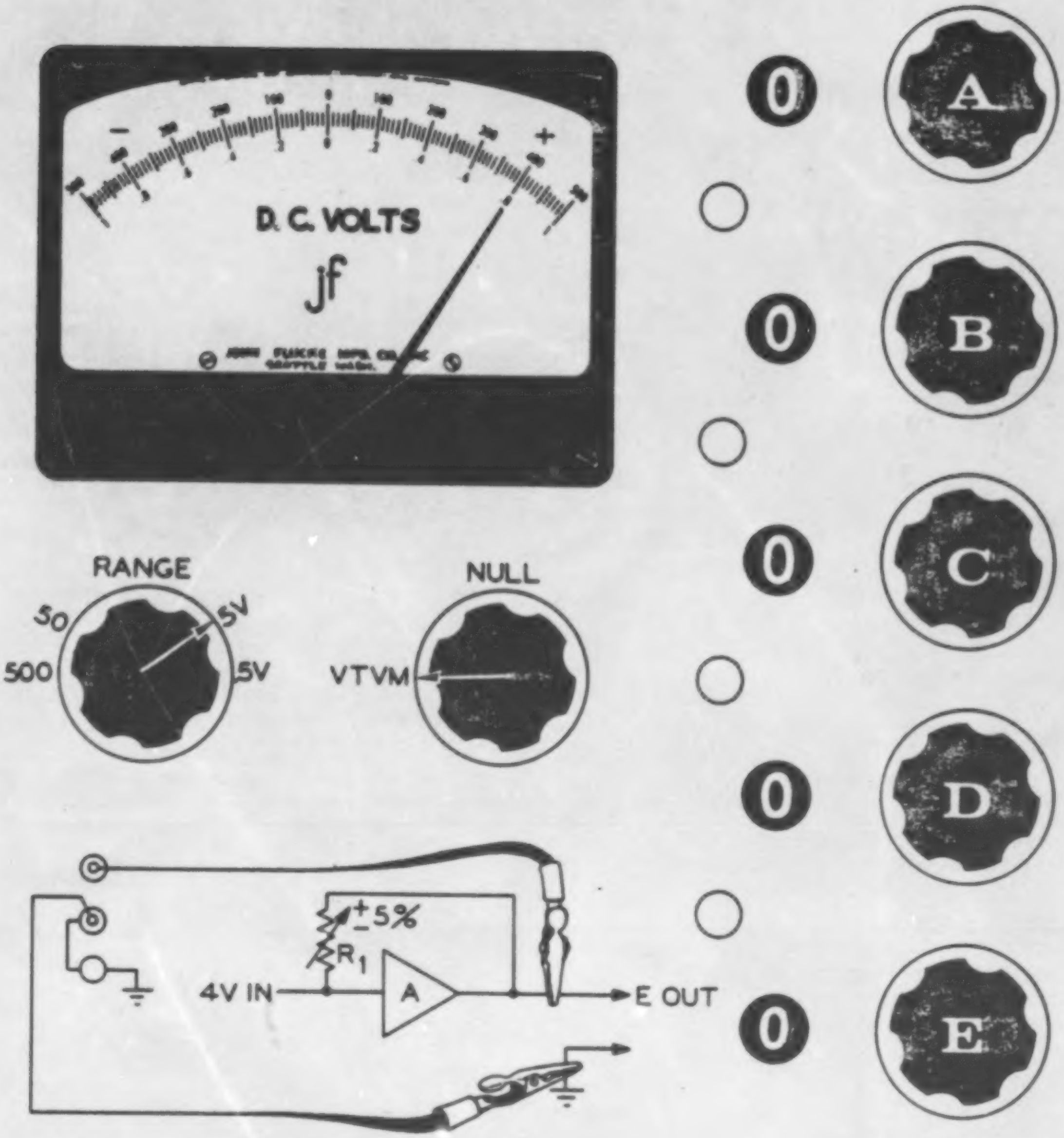


Figure 84. Meter/circuit connecting and recording.

- Turn switch A, shown on figure 85, to 4.
- Turn Null switch to 1 from VTVM. The neon just below the 4 will light, indicating the unit's range. The light represents a decimal point.
- Observe indicator B.
- The reading shows that the voltage is less than 4V (negative deflection).
- Place Null switch to VTVM.
- Decrease voltage to 3.8000 by using knobs A and B (refer to fig. 86).
- Place Null switch to 1V.
- Observe meter indicator (C).
- The exact voltage is *not* 3.8 volts.
- Increase indicator knob C to move indicator to null position.
- Reading is 3.88V.

8-75. *Using the meter to set circuit voltage output.* Using the same connections, set the output of the amplifier to 4V ± .01. Since the measured output is 3.88V and the gain adjust on the amplifier is capable of adjusting ±5 percent, the amplifier can be adjusted to 4V output. (.05 × 4 = 0.2V ±.) Refer to figure 87 (in the workbook) for the following analysis:

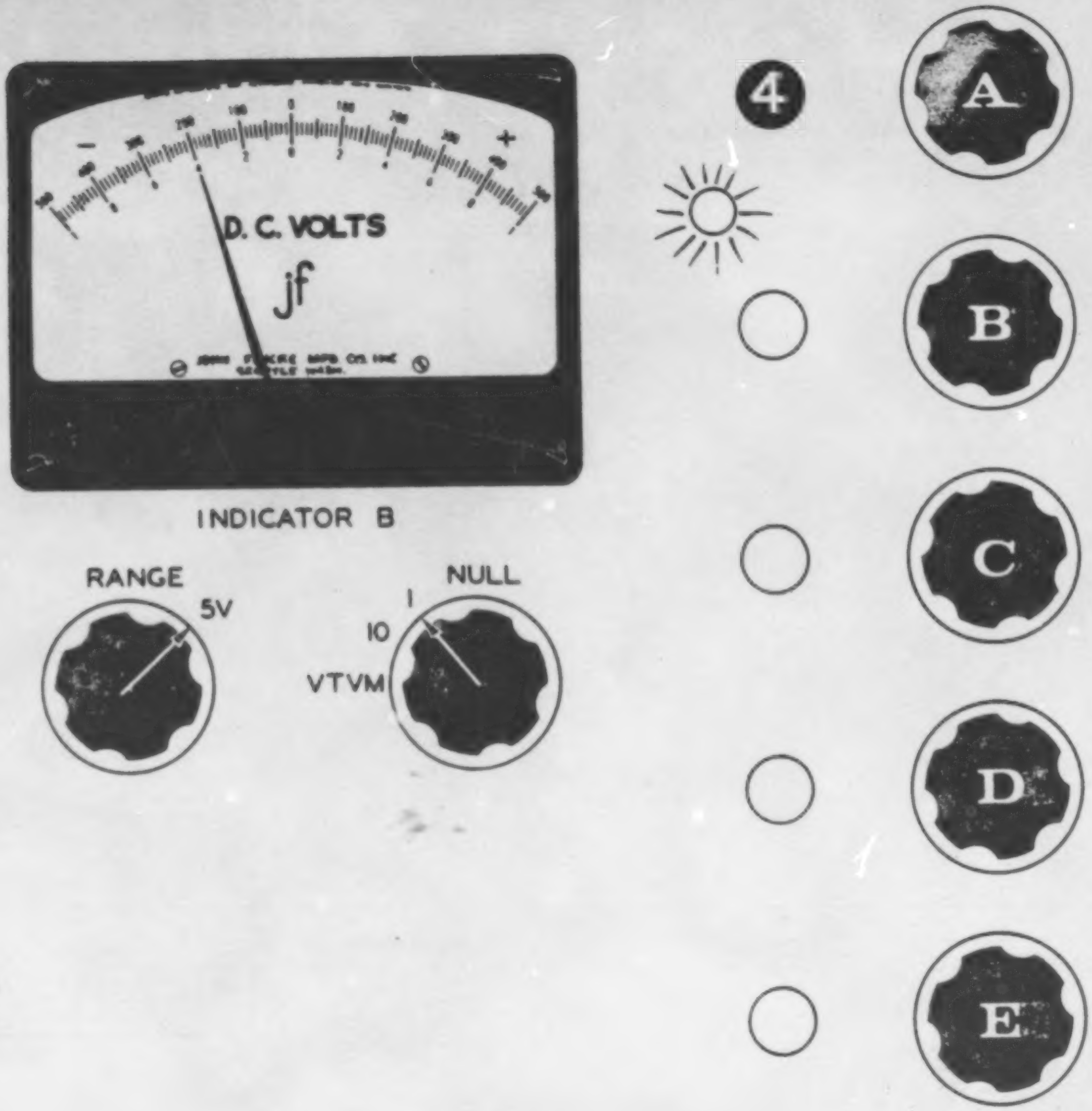


Figure 85. Voltage reading.

- Place the meter controls as follows: (Refer to fig. 87,A.)
  - (1) Turn the Null control to 1V. (Refer to fig. 87,A.)
  - (2) Adjust the Gain control until the needle indicator moves to null. (Refer to fig. 87,C.)
- Move the Null control to .1V (Refer to fig. 87,D.)
- Read the meter.
- If the needle indicator moves to the right, reverse the Gain control slightly to center the indicator. (Refer to fig. 87,E.)
- If the needle moves to the left, continue turning the Gain control in the same direction you did to bring the needle to center. (Refer to fig. 87,E.)
- Move the Null control to .01V. (Refer to fig. 87,F.)
- Using the Gain control on the amplifier circuit, adjust the control for a null. (Refer to fig. 87,E.)
- The output is now 4V ±.01V.
- Move the Null control to VTVM.
- Remove the probes.

This completes this exercise.

8-76. Measurement of Voltage Excursions About a Nominal Value. Although you may not use this meter in this application very

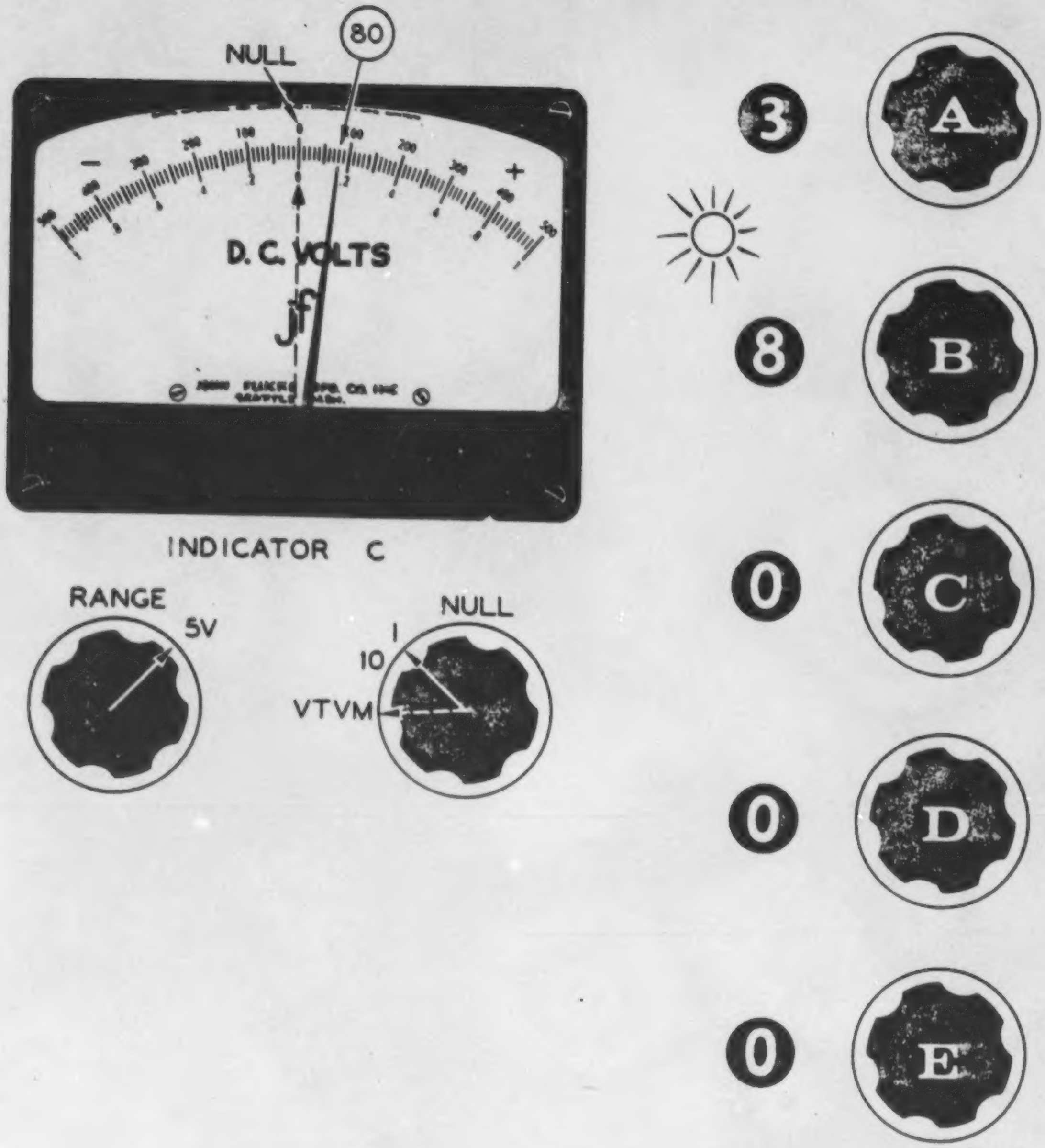


Figure 86. Calibrated voltage preliminary reading.

frequently, it is a useful device for you to understand. The primary result to be obtained from this application is the measurement of the amount of excursion or change from a specified value or, stated in more common terms, the amount of drift a voltage reference source has. An example of such a situation could be a regulated power supply output which is supposed to maintain exactly -15 VDC. However, because of a defective internal component, the voltage is not stable. To measure and check for this possibility, connect the meter as follows:

- Refer to figure 88 (in the workbook) for pictorial views of instructions.
- Connect leads from the voltage output and equipment ground to the meter terminals, as shown in figure 88,A.
- If the meter reads to the left, the voltage being measured is negative; set the polarity switch to the negative position. Refer to figure 88,B.
- Set the Range switch to the lowest range which will give an on-scale reading, and note

CHART 2
HIGH RESISTANCE MEASUREMENT GROUP ANALYSIS

GROUP	METER RANGE	SETTINGS NULL	COMPUTATION FACTOR	DIRECTIONS
I 1 to 500 mΩ	500	10	Subtract 10 from the voltage readout dials.	1. Adjust voltage readout dials for full-scale deflection.
II 500 to 5000 mΩ	500	1.0	Subtract 1.00 from voltage readout dials and multiply the result by 10.	1. Repeat step 1 above. 2. Result of computation is the resistance in megohms.
III 5000 to 50,000 mΩ	500	0.1	Multiply the amount set on the voltage readout dials by 100.	1. Repeat steps 1 and 2 above.
IV 50,000 to 250,000 mΩ	500	0.1	Apply the formula Em = ... Substitute the meter reading in volts.	1. Adjust voltage readout dials for a convenient meter deflection.

the nominal value of voltage indicated. Refer to figure 88,C.

- Set the five voltage Readout dials to the nominal voltage—in this case to 15 volts. Refer to figure 88,D.
- Turn the Null switch to the lowest position that will allow voltage excursion to remain on the scale. (Refer to fig. 88,E.)
- Read the excursions from the meter. Note that full-scale deflections are equal to the NULL voltage setting. Full-scale deflection with NULL at 1V = 1V. In our example, the excursion is approximately ±.4 volt.

NULL = 1V full deflection
EXCURSION = ±200 = ±.4V.

The voltage requirements at power supply output require regulated - 15 VDC. The actual output varies from - 15.4 VDC to - 14.6 VDC. This condition would indicate a defective power supply and would require you to change it and repair it.

8-77. **Measuring High Resistances.** The differential voltmeter may be used to measure resistances between 1 megohm and 500,000 megohms. The following equation is used when determining these resistances:

$$Rx - 10\left(\frac{E}{EM} - 1\right)$$

where:

Rx = unknown resistance in megohms.
E = the voltage setting of the 5 voltage knobs.
EM = the meter reading on the appropriate scale as determined by the Null switch setting.
10 = megohms of input resistance of the VTVM circuit on 10-, 1-, and 0.1-volt null ranges.

8-78. There are four different routines for measuring resistances. Each routine is designed to provide a result based upon a grouping of resistance values.

- Group I must be used to measure resistances from 1 megohm to 500 megohms.
- Group II must be used to measure resistances from 500 megohms to 5000 megohms.
- Group III must be used to measure resistances from 5000 megohms to 50,000 megohms.
- Group IV must be used to measure resistances from 50,000 megohms to 250,000 megohms.

8-79. The primary differences in the routines for the groups are the null settings and the computation directions. Rather than list each one, study chart 2 so that you can recognize and interpret the differences.

8-80. **Multimeters.** In resident training you studied the basic principles of meters used in performing maintenance in the data processing field. Our discussion here will deal with one meter that is a good representative of the multimeters used with the different types of equipment. Some of the different multimeters

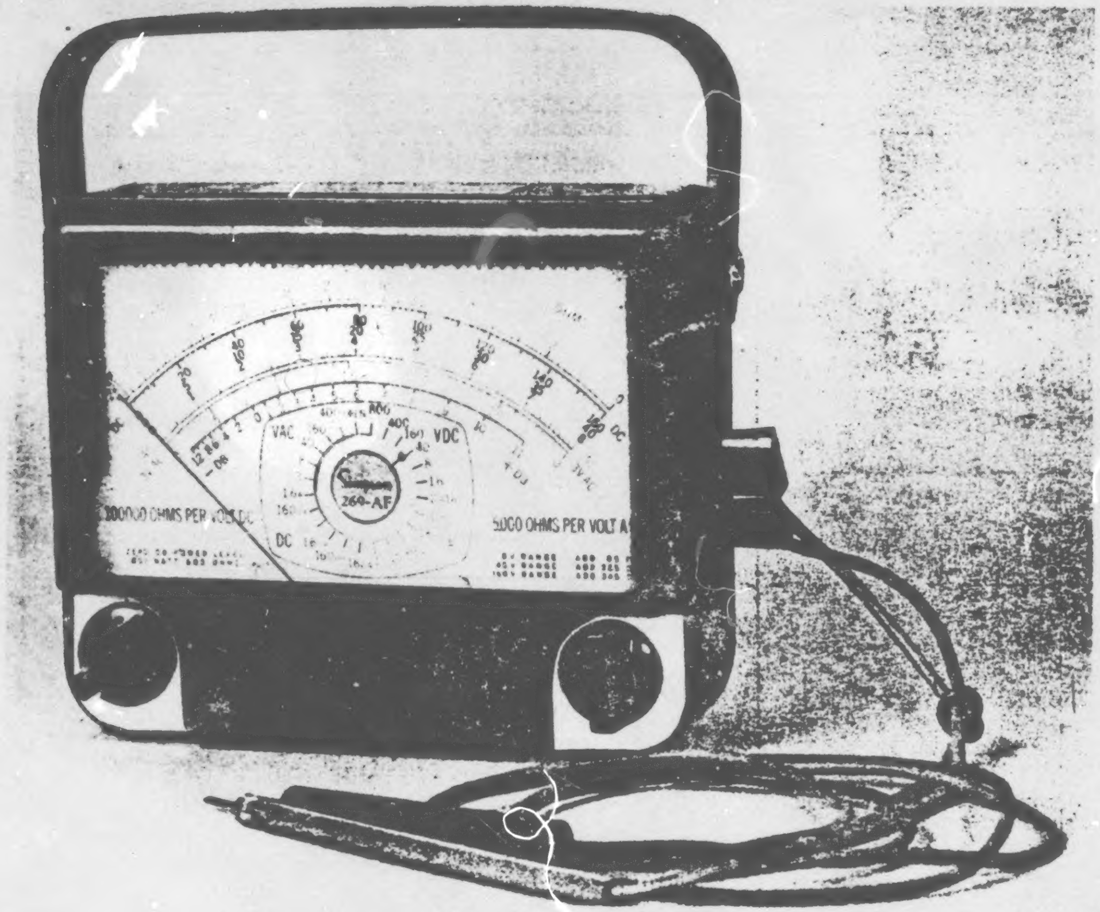


Figure 89. Multimeter.

used are the PSM-6, PM-7, and models 260 and 269. Of these we have selected the model 269 (fig. 89) for discussion.

8-81. General Description. The model 269 is designed to measure DC and AC voltage, direct current, and resistance in the ranges most commonly encountered in electronic equipment. Let's first discuss the different ranges available and the maximum values that can be measured.

8-82. *DC voltage measurement.* DC voltages may be measured in the range of 0 - 4000 volts at a sensitivity of 100,000 ohms per volt sensitivity on all ranges. The different DC range selections available are:

0 - 1.6 volts
0 - 8 volts
0 - 40 volts
0 - 160 volts
0 - 400 volts
0 - 1600 volts
0 - 4000 volts

8-83. *AC voltage measurements.* AC voltages may be measured in the range of 0 - 800 volts at a sensitivity of 5000 ohms per volt on all ranges. AC measurements, including output and decibel reading, are made by rectifying the AC voltage with an internal recitfier, and then applying the resulting DC voltage to the meter circuit. The different AC range selections are:

0 - 3
0 - 8
0 - 40
0 - 160
0 - 800

8-84. *DC resistance measurements.* Resistance measurements may be made in the range of 0 - 200 megohms. Two internal batteries furnish the required power for making resistance measurements. A 1.5-volt battery furnishes the power for the lower four ranges which are 0 - 2 megohms. A 22.5-volt battery supplies the power for the highest two ranges —0 -20 and 0 -200 megohms.

8-85. *DC measurements.* Direct currents from 0 - 16 amperes may be measured directly on the multimeter. The different DC ranges available are:

0 - 16 microamperes
0 - 160 microamperes
0 - 1.6 milliamperes

0 - 1.6 amperes
0 - 160 milliamperes
0 - 16 amperes

8-86. **Typical Uses of a Multimeter.** A good habit to develop when making voltage or current measurements is to turn off all power to the circuit under test, connect the test leads, and then turn on the power to take the reading. Then, turn off the power before disconnecting the test leads. If this is not feasible, be sure you do not touch the uninsulated part of the test leads.

8-87. *Zero adjust.* Before making any measurements with a multimeter, the first step is to make certain that the needle indicates zero when the meter is in its operating position. If the pointer is not on zero, adjust the screw that is normally located below the center of the meter scale until the pointer is exactly on zero.

8-88. *DC voltage measurements up to 1600 volts.* When measuring any voltage you are not sure of, always start with the highest range as a protection for the meter. After observing the first reading to determine that a lower range may be used, set the range selector to a lower range for a more accurate reading. To measure DC voltages, turn the selector switch pointer to the desired range in the VDC area. Plug in the black test lead or connect it to the common (COM), and the red lead to the positive (POS) jack of the meter. Then connect the other end of the black lead to the negative side and the other end of the red lead to the positive side of the circuit under test. This should be done with the circuit under test deenergized. Once power is applied, though, the meter pointer may deflect off scale past zero. The polarity in this case is wrong and the leads must be reversed.

8-89. The voltage is read on the black arc marked DC, which is the second line of numbers from the top of the dial. The scale is read as follows:

- For the 1.6-volt range, use the 0 - 160 figures and divide by 100.
- For the 8-, 40-, and 160-volt ranges, read the figures directly.
- For the 400-volt range, use the 0 - 40 figures and multiply by 10.
- For the 1600-volt range, use the 0 - 160 figures and multiply by 10.

8-90. *DC voltage measurements from 1600 - 4000 volts.* When measuring voltages this high, you must be extremely careful. Make sure that the power is off and all capacitors in the circuit have been discharged before making meter connections. Do not touch the meter leads while taking the reading or while power is still applied. A high-voltage probe (X100) is normally supplied with meters that are capable of measuring high voltages. If a high positive voltage is to be measured, connect the probe to the red terminal, or to the black terminal if a high negative voltage is to be measured. Take the reading from the 0 - 40 DC scale; then multiply this reading by 100.

8-91. *AC voltage measurements.* Again, if you are in doubt about the value of voltage being measured, always use the highest range.

- First, turn the Range selector switch until the pointer indicates the appropriate VAC range.
- Second, connect the test leads across the voltage source to be measured. AC voltages will read correctly regardless of polarity.
- Third, take the reading from the red numeral AC scale as follows:

(1) For the 3-volt AC range only, read the voltage on the red arc marked 3 VAC, which is the second from the bottom of the dial, using the red figures below the arc.

(2) For the other ranges use the red arc marked "AC," which is third from the bottom of the dial. Read the black digits between the AC and DC arcs.

(3) For the 8-, 40-, and 160-volt ranges, use the figures as they are marked.

(4) For the 800-volt range, use the figures 0 - 8 and multiply by 100.

8-92. *Resistance measurements.* Before you make any resistance checks, you should always make sure that all voltage to the circuit under test is turned off. Then, turn the selector switch to the desired range. The ranges are marked with red figures in the Rx area. Each reading on the ohms scale is to be multiplied by the quantity indicated at each range position.

- The first step is to zero the meter on the ohms scale. This is done by shorting the test leads together and rotating the Zero Ohms knob to indicate zero ohms on the top scale.
- The next step is to connect the leads across the resistance to be measured. Take the reading from the OHMS arc at the top of the dial. The meter is calibrated so that the most accurate reading is obtained at the center of the scale. Therefore, you should select the range that gives a deflection nearest the center of the scale.
- Third, take the reading from the ohms scale and multiply by the quantity indicated by the range pointer. For example, suppose the indicator of the meter, as shown in figure 89, on the ohms scale reads 20 and the range pointer indicates the Rx 100K range. The

resistance is 20 times 100,000, or 2 million ohms, which is the same as 2 megohms.

8-93. When you complete your resistance checks and the meter is no longer in use, turn the Range switch to a position other than "Rx." If the switch remains in the Rx range and the leads become shorted together, the batteries will be drained.

8-94. *DC measurements up to 1.6 amperes.* A word of caution: The leads should *never* be connected *across* any voltage source when measuring current. The meter should *always* be connected in *series* with the voltage source. Position the Range switch to the current range desired. When in doubt about the current value, use the highest range. The current ranges are marked in black in the DC area. Then make sure that there is no power applied, open the circuit in which the current is to be measured, and connect the meter in *series* with the circuit with the red lead toward the positive side and the black lead toward the negative side.

8-95. Turn on the circuit power and read the value on the black scale marked DC, which is the second from the top of the dial. If the meter deflects off scale past zero, turn the power off and reverse the test leads. Read the scale on figure 89 for the different values of current as follows:

- For the 16-MA range, read the figures 0 - 160 and divide by 10 for microamperes.
- For the 160-MA range, read the figures 0 - 160 directly for microamperes.
- For the 1.6-MA range, read the figures 0 - 160 and divide by 100 for milliamperes.
- For the 16-MA range, read the figures 0 - 160 and divide by 10 for milliamperes.
- For the 160-MA range, read the figures 0 - 160 directly for milliamperes.
- For the 1.6-A range, read the figures 0 - 160 and divide by 100 for amperes.

8-96. For DC measurements up to 16 amperes, observe the same precautions taken in measuring currents up to 1.6 amperes and proceed as follows:

- Position the selector switch so that the range pointer indicates 16 MA-AMP.
- Plug the black test lead into the COM jack on the left side of the meter. Plug the red test lead into the 16 AMPS jack on the right side of the meter.
- Connect the test leads in series with the source to be measured; then turn on the power.
- Read the current value from the DC scale. Use the figures 0 - 160 and divide by 10 for amperes.

8-97. **Applications.** We have already discussed how the volt-ohm-milliammeter is used to measure AC and DC voltages, current, and resistance. Now let's discuss some other applications in which you will find the multimeter a very handy tool.

8-98. *Checking capacitors.* The ohmmeter circuit can be used to identify good, open, or short conditions of most capacitors. For best results you should use the highest Rx range. The ohmmeter supply voltage is applied to the capacitor to see if it will charge. A good capacitor will permit current to flow, deflecting the meter pointer, while it is charging up to the applied voltage. This produces a swing of the meter pointer, with a gradual return to infinity at the left-hand side of the scale. The greater the capacity, the more the pointer will swing and the longer it will take for it to return to infinity.

8-99. If the capacitor is open, there will be no pointer deflection. However, on very small capacitors the pointer deflection is very slight with a rapid return to infinity. So you must watch the meter closely when checking the smaller capacitors. If the capacitor is shorted, the pointer will remain deflected on the ohms scale and will not return, even slowly, toward infinity.

8-100. When making checks on electrolytic capacitors, connect the positive lead of the meter to the positive lead of the capacitor. If you have the leads reversed, the meter pointer will peg off scale.

8-101. *Checking diodes.* The resistance of copper oxide, selenium, and crystal rectifiers can normally be measured in both directions. The forward and back resistance can be measured at a voltage determined by the battery potential of the ohmmeter and the resistance range at which the meter is set. When the test leads of the ohmmeter are connected to the crystal diode, a resistance is measured which is different from the resistance indicated if the leads are reversed. The smaller value is called the *forward resistance*, and the larger value is called the *back resistance.* If the ratio of back-to-forward resistance is greater than 10:1, the diode should be capable of functioning as a rectifier. However, you should keep in mind that this is a limited test and does not take into account the action of the diode at voltages of different magnitudes and frequencies.

8-102. *Checking transistors.* An ohmmeter can be used to test transistors by measuring the emitter-collector, base-emitter, and base-collector forward and back resistances. A back-to-forward resistance ratio on the order of 500:1 should be obtained for the collector-to-base and emitter-to-base measurements. The forward and back resistances between the emitter and collector should be nearly equal. All three measurements should be made for each transistor tested, since experience has shown that transistors can develop shorts between the collector and emitter and still have good forward and reverse resistances for the other two measurements.

8-103. Because of shunting resistances in transistor circuits, you will normally have to disconnect at least two transistor leads from the associated circuit for this test. You must exercise caution during this test to make certain that current during the forward resistance test does not exceed the rating of the transistor. Ohmmeter ranges which require a current of more than 1 milliampere should not be used for testing transistors.

9. Special Test Equipment

9-1. This section is devoted to specially built test equipment. Special-purpose test sets are designed to isolate problems down to the defective component with you, the operator, simply following a set of instructions that exercise the test set. You will probably be told at some time that certain pieces of special test equipment are no good and it's a waste of time to use them. But, you must remember that *to insure that circuit components meet the design specifications, you must use test equipment designed to test these specifications.* During this discussion we will analyze the use of several pieces of test equipment that you may use, with emphasis on certain pieces that are representative of others. The first type is the drawer tester.

9-2. **Drawer Tester.** The drawer tester shown in figure 90 (in the workbook) is used for testing and troubleshooting drawer assemblies of the RCC and EDLCC portions of the 465L equipment. There is another similar tester (AN/FYM-13) for testing and troubleshooting other portions of the 465L system.

9-3. The cabinet on the left in figure 90 is the control and display console, and the one on the right is the programmer and storage console. A detailed breakdown of the common name and reference designations is shown in figure 91 (in the workbook). By studying figure 91 for a few moments, you can see that the control and display console is made from fixed assemblies and drawers. Assemblies A1 (time lapse panel) and A4 (display controller panel, also shown in figure 93 as a closeup) are two fixed panels. Assemblies A2, A3, A5, A6, A7, A8, and logic power supply A9 are all drawers. Looking at the programmer and storage console on figure 91, you can see a shelf extended out from the front. The drawer to be tested is placed on this shelf, and the connectors on the rear of the drawer mate with the receptacles on the test shelf unit A8. Assmebly A1 accepts each individually selected programmer panel. The choice of panels depends upon the type of drawer under test.

9-4. When a system malfunction has been isolated to a particular drawer assembly, the suspected drawer is mounted on the test ledge and an appropriate pluggable programmer is

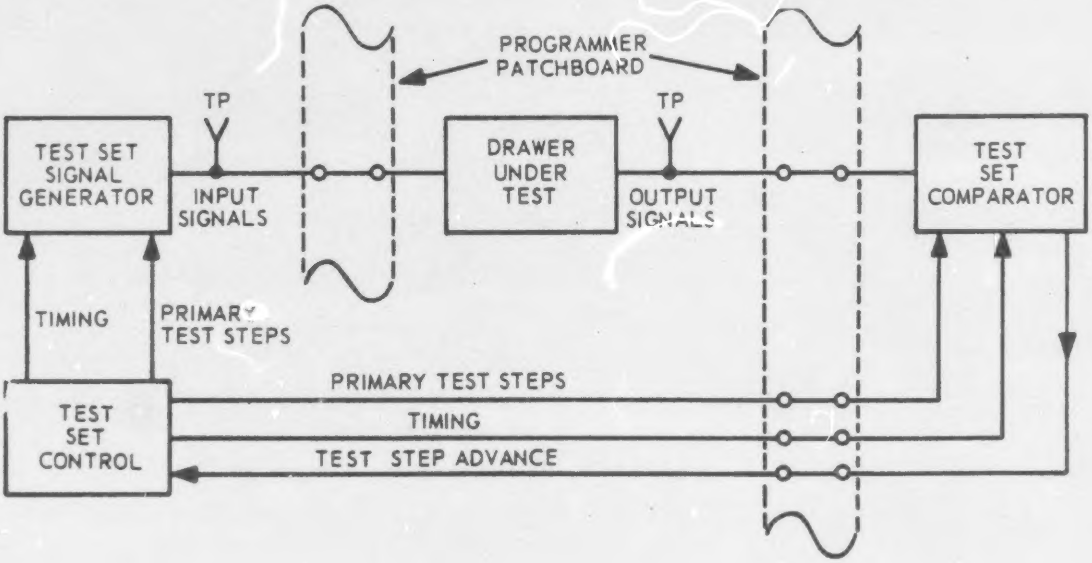


Figure 92. Automatic test, block diagram.

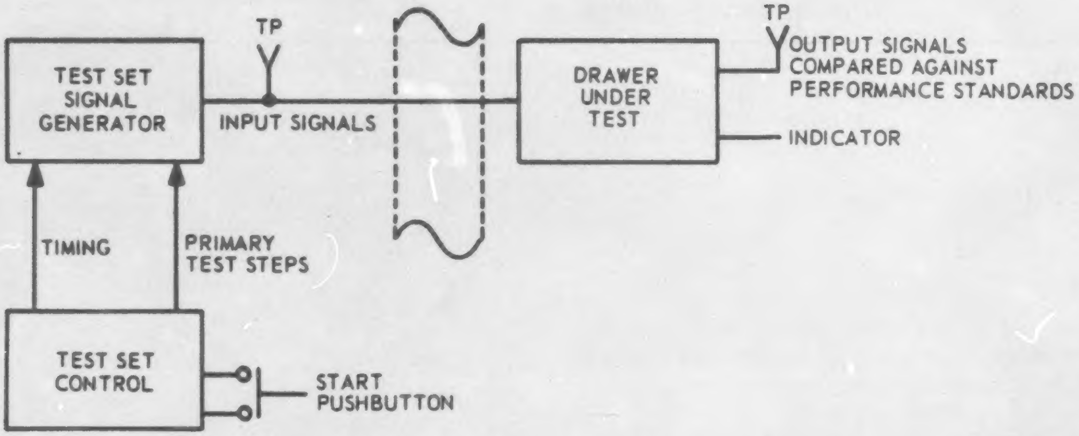

TP
TEST SET SIGNAL GENERATOR
INPUT SIGNALS
DRAWER UNDER TEST
TP
OUTPUT SIGNALS COMPARED AGAINST PERFORMANCE STANDARDS
INDICATOR
TIMING
PRIMARY TEST STEPS
TEST SET CONTROL
START PUSHBUTTON

Figure 94. Manual test, block diagram.

selected and mounted on the programmer panel (cabinet A2). One or more pluggable programmers are available for each of the drawers the test set will test. One of these programmer patchboards is shown installed in the top panel of the right-hand cabinet in figure 90.

9-5. The drawer test set checks each drawer by automatically exercising each circuit in the drawer in a preprogrammed sequence. The input and output signals of the drawer are evaluated at each programmed step by comparator circuits. Each satisfactory response initiates a GO (sequence advance) signal which causes the drawer test set to advance one step and automatically evaluates the next programmed function. In some instances, circuit complexity makes it impractical to perform the entire test procedure automatically. Auxiliary test equipment is connected to the tester in order to make the necessary additional checks manually. During these manual operations, the automatic sequencing of the test steps is interrupted and resumed thereafter. You may also select the manual mode of operation so that you can examine waveforms at any particular test step.

9-6. *Automatic test.* Figure 92 shows a block diagram of the automatic test setup. Signals produced by the test set signal generator for each test step are applied, through the patchboard, to appropriate inputs of the drawer under test. The output signals produced by the drawer are then coupled through the patchboard to the test set comparator. The test set comparator samples the drawer outputs at each test step to determine whether they are of proper quality and in proper time relationship with the signals from test set control. If the comparator accepts the signals, the test set will automatically advance to the next step. If the incoming signal is rejected, the test set will stop and the test fail lamp will go on. The *primary test step* lamp matrix (see fig. 93 in the workbook) indicates the step at which the fail condition occurred,

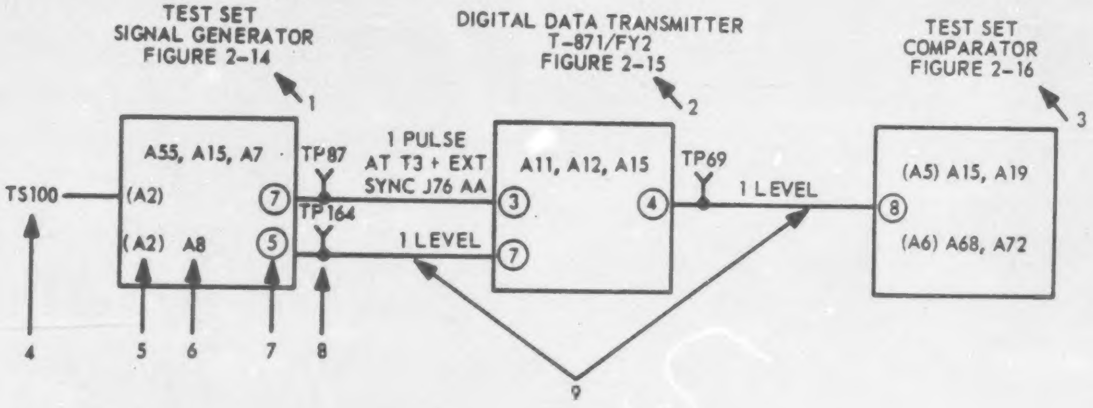

TEST SET SIGNAL GENERATOR FIGURE 2-14
1
DIGITAL DATA TRANSMITTER T-871/FY2 FIGURE 2-15
2
TEST SET COMPARATOR FIGURE 2-16
3
A55, A15, A7
(A2)
(A2) A8
⑦
⑤
TS100
TP87
TP164
1 PULSE AT T3 + EXT SYNC J76 AA
1 LEVEL
A11, A12, A15
③
⑦
④
TP69
1 LEVEL
⑧
(A5) A15, A19
(A6) A68, A72
4
5
6
7
8
9

Figure 95. Test block diagram.

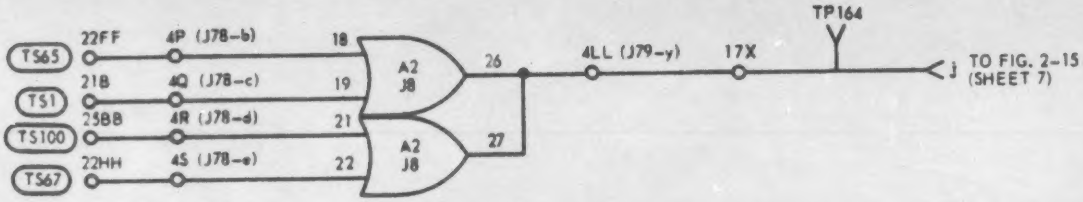


Figure 96. Test 1 level at TP164.

and the test fail lamp lights. Inputs and outputs are then checked to determine the cause of the failure. We will discuss the control panel (fig. 93) in greater detail after first analyzing the manual test mode of operation.

9-7. *Manual test.* Figure 94 illustrates the use of visual comparison of signals instead of the test set comparator. The test set control circuits provide the required control and timing signals that cause the signal generator to activate the drawer under test. The drawer outputs are then checked at the test point with auxiliary test equipment and compared with prescribed performance standards. If the indications are correct, the START pushbutton is depressed to advance to the next test set. If the indications are incorrect, the trouble is then isolated to the defective printed circuit board.

9-8. When a malfunction occurs during the performance of a test procedure, it is necessary to determine the location of the trouble by using the following support material:

- Test block diagrams.
- Test set signal generator test logic diagrams.
- Drawer under test logic diagrams.
- Test set comparator test logic diagrams.

9-9. **Test Block Diagram.** Figure 95 is a typical test block diagram for one test step. A complete set of block diagrams is provided for each drawer assembly test. The test block diagram provides the initial data needed for troubleshooting. Refer to the callouts in figure 95 and we will discuss the block diagram in detail.

CALLOUT:

1 - Indicates the figure number of the test logic diagrams for the test set signal generator.

2 - Indicates the figure number of the test logic diagrams for the drawer under test.

3 - Indicates the figure number of the test logic diagrams for the test set comparator. All of these logic diagrams are conveniently placed in the technical order with each drawer test procedure.

4 - Indicates the particular test step which is visually indicated on the display panel in figure 93 (control panel).

5 - Indentifies the particular test set drawer or drawers containing the PCBs or components being tested during this test step.

6 - Identifies the particular PCB or component within the test set drawer or the drawer under test that is being tested at this test step.

7 - Indicates the sheet number of the logic diagram in the figure designated above the block that corresponds to the indicated test point. For example, callout 7 in figure 95 indicates that sheet 5 of figure 2-14 contains the logic for card A8 (J8 on logic diagram) which produces the 1 level at TP164. Figure 96 shows the logic diagram that is tested to generate the 1 level at TP164. Sheet 7 of figure 2-14 contains the logic tested to generate the signal at TP87. This portion of the logic is shown in figure 97. Notice that TS100 is gated through all the cards indicated on the test block diagram.

8 - Indicates the test points on the test panel shown in figure 91 (programmer and storage console, assembly A2).

9 - Indicates the performance standard to be observed.

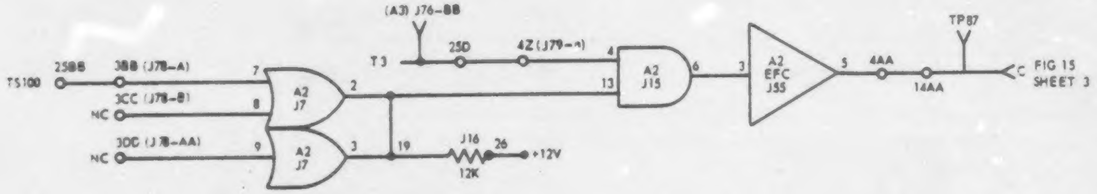


Figure 97. Test, TP87.

9-10. If you know how to read the test logic diagrams, it is easy to troubleshoot both the drawer under test and the drawer tester. Refer to figure 95. If the tester fails on TS100, a check at the three test points would isolate the trouble to the group of cards listed for either the drawer under test or the test set signal generator. If these signals are correct, then the trouble would be in the test set comparator. When the trouble has been localized to one of these sections, the PCBs indicated in this section should be replaced. If this doesn't correct the trouble, you should then refer to the appropriate logic diagram and make further checks with an oscilloscope. Figure 98 (in the workbook) illustrates the typical logic diagram and the general symbology and coding used in the drawer test set.

9-11. **Test Procedures.** Before you attempt to test a drawer you must refer to the appropriate technical order which describes the operations of the tester and provides a guide for correct interpretation of performance standards. General information for operating the tester and the individual drawer test procedures for the AN/FYM-2 are covered in TO 31S5-2FYQ-47. This TO includes the test procedures, test block diagrams, and logic diagrams used in testing and troubleshooting both the drawer under test and drawer test logic that is being checked.

9-12. Self-Check. Refer to figure 93 (in the workbook). As with any other piece of test equipment, the first step is to determine the operational status of the test set. Performing a self-check of the drawer checker assures that the functional circuits of the test set are operational. The test is comprised of 100 test steps with groups of these steps being used to test operation of specific test set circuits. The logic circuits used during a self-check are made up of elements located in the various drawers of the test set. If a failure occurs during the self-check routine, you should refer to TO 33D7-49-14-2. This TO covers the principles of operation and the diagrams of the logic exercised during each test step. Performance test data tables which indicate the test points, performance standards, and drawer and card under test at each test step are also provided.

9-13. The drawer tester enables you to

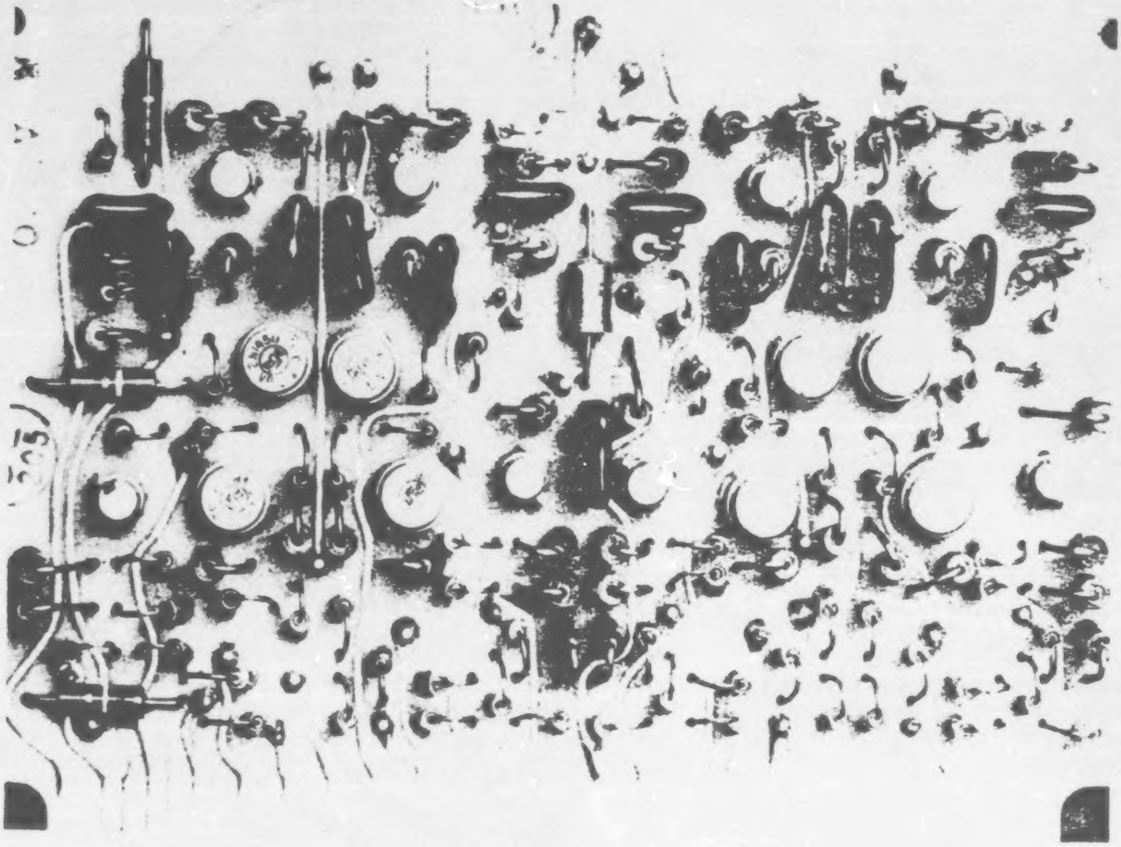


Figure 99. Printed circuit card.

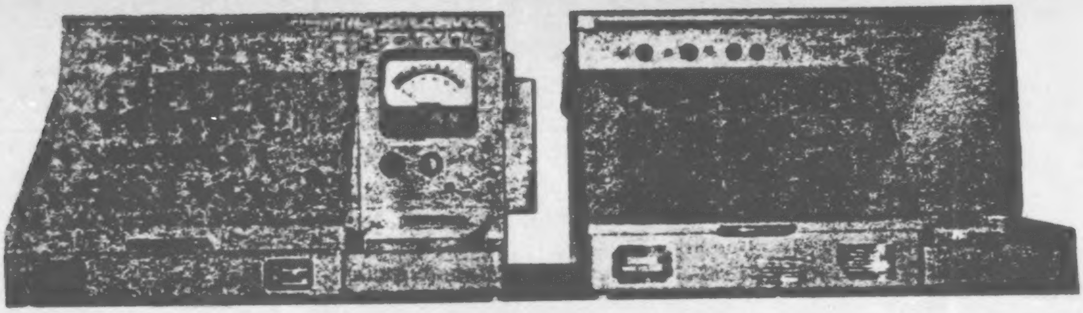


Figure 100. Card testers, 416L.

isolate the trouble to a card or group card level. If you know data flow well, it is quite possible that you will be able to further isolate the malfunction to a single card component. In most cases, however, you will need to subject the suspected cards to further tests. Card testers are supplied for this purpose.

9-14. Again referring to figure 93 (in the workbook) notice the group of lights and controls. We have not explained all of them because of their varied complexity and special-purpose uses; however, the test status lamps indicate the overall testing capability of the set. The primary test step and secondary test step light in sequence, and if a test fails, the total of their numbers equals the test step where the failure occurred. The rest of the lamps and switches are used for power control and special test features.

9-15. **Card Testers.** Each different type of card requires specific input and output conditions for accurate testing. Since the using system often requires thousands of cards, you could conclude that the problem of designing a card tester would be insurmountable if each type of card had a different requirement for testing. This is not true, however, because designers of modern-day equipment have developed a system for the standardization of cards.

9-16. In any system there are requirements for basic circuits such as AND gates, OR gates, and diode matrices. The number of combinations of these basic circuits is almost unlimited; however, the number of different types of individual circuits is limited to a relatively small number. Cards are assembled using capacitors, resistors, diodes, and other components necessary for the formation of one or more basic circuits. All components and circuits on the card are connected to a connector strip at one edge of the card (see fig. 99). This makes it possible to use variations in external wiring to connect various components on the card to form the required circuits. One card, for example, may be connected to form four flip-flops with their associated input and output components. When four of these cards are used, a 16-stage shift register, storage register, or counter can be constructed simply by variations in external wiring. A small number of different kinds of cards can be used to form the many circuits required by the data processor. Some processors use as few as five different kinds of cards. This standardization of cards also makes card testers practical in that they need be programmed to check only a limited number of standard cards.

9-17. The test sets covered here generate test signals and provide test loads and voltages which simulate actual input and output operating conditions for the plug-in cards or modules under test. Setups and programs for card testers vary; however, all of them simulate operating conditions when testing cards. All testers have test jacks at which circuit functions are available for application to external test equipment such as the oscilloscope. Now let's look at some of these testers and see how they work.

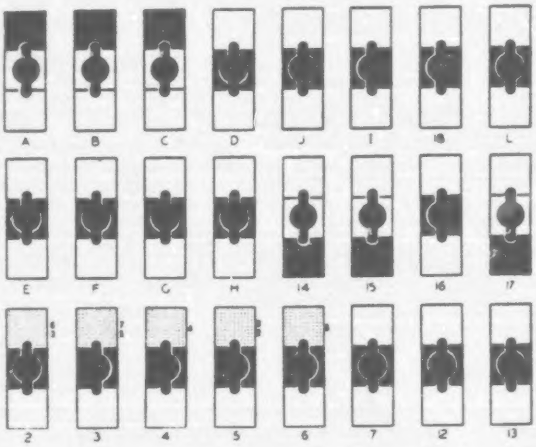


Figure 101. Card tester overlay program.

9-18. *Card tester, 416L.* The card tester used with the 416L system is relatively when compared with others. This simplicity is due in part to the fact that all cards used by the 416L data processor are not tested on the same card tester. There are at least three different card testers. Each one is able to supply only the functions necessary for testing one group of cards. Another reason for the simplicity is that test programs are set up by means of switches. Two of these testers are shown in figure 100. Note the switch panel of the tester on the left. The tests which it performs on a card under test are programmed by various combinations of these switch settings. The card tester comes supplied with a set of plastic overlay cards for this switch panel. To operate this tester, you simply select the overlay for the card you wish to test, place the overlay on the switch panel, and set the switches as indicated by the overlay. The overlay, shown in figure 101, has the test position for each switch indicated by a blackened area or a dotted area. In the initial tests, the switches are moved toward the blackened areas. If the center of the rectangle is blackened, the switch remains in its center position. Additional tests are made by individually moving each switch toward a dotted area, reading an associated meter, and then returning the switch to the position indicated by the blackened area.

9-19. *Card tester, AN/GPM-50.* Probably the most elaborate card tester you may come in contact with is the AN/GPM-50, shown in figure 102, which is in the workbook. This tester is used to test cards of the data processing and display subsystems of the 412L Aircraft Warning and Control System. This test set can completely test all of the components on 95 percent of the system's cards semiautomatically. It will check part of the components on the remaining 5 percent semiautomatically. The remaining components must be checked manually. The cards are subjected to one or more of the following tests:

- Resistance.
- Impedance.
- Static.
- Dynamic.

9-20. Look closely at figure 102 and you will note from the callouts that the tester is composed of four cabinet units bolted together. From left to right, the units are:

- Program and decoding.
- Viewing and switching.
- Simulator and display.
- Manual test and power.

Semiautomatic operation of this set is accomplished through use of predetermined test programs stored in binary-coded form on punched tape.

9-21. The program stored on the tape is decoded by the program and decoding unit which, in turn, automates all programmed test functions to allow a complete analysis of the card under test.

9-22. Values measured by the tester are compared with high and low limits programmed on the test tape. The test sequence automatically stops if a given test result is not within the prescribed tolerance or if a manual reading or control manipulation is required. Note the two rows of small windows just below the tape deck on the program and decoding unit. The upper row displays the test number, and the lower row displays the out-of-tolerance measurement. The test number refers the operator to the applicable TO instructions about the test being performed. Waveforms requiring detailed analysis are automatically displayed on the oscilloscope of the simulator and display unit.

9-23. For rapid reference to applicable TO instructions, the viewing and switching unit provides a microfilm view screen. Complete TO reference data is contained on microfilm and is displayed on the view screen through the use of a front panel film slew control.

9-24. Test signals (pulses, feedback nets, bias voltages, etc.) are supplied by the simulator and display section. The manual test and power portion of the set is used to test cards that cannot be completely checked in the semiautomatic mode.

9-25. *Card tester, TS1996/FYQ.* Another example of a card tester (see fig. 103 in the workbook) is the electronic circuit plug-in unit used with the 465L data processing subsystem. The principles of this tester are no different from those of the card testers just discussed. This tester supplies the supply voltages and signals that the card would receive under normal operating conditions and then checks to determine whether the card circuits perform their proper functions.

9-26. Standard and special test equipment is used in conjunction with the card test set for various performance tests. Figure 104 shows a bench test setup. The drawer tester covered earlier supplies the signals which are necessary for the operation of the card tester during routines in which two signals are applied simultaneously to the circuit under test. In addition to the drawer tester, two standard test sets, an oscilloscope (not shown), and a signal generator are used. The signal generator must be of the type that can produce square waves and rectangular pulses

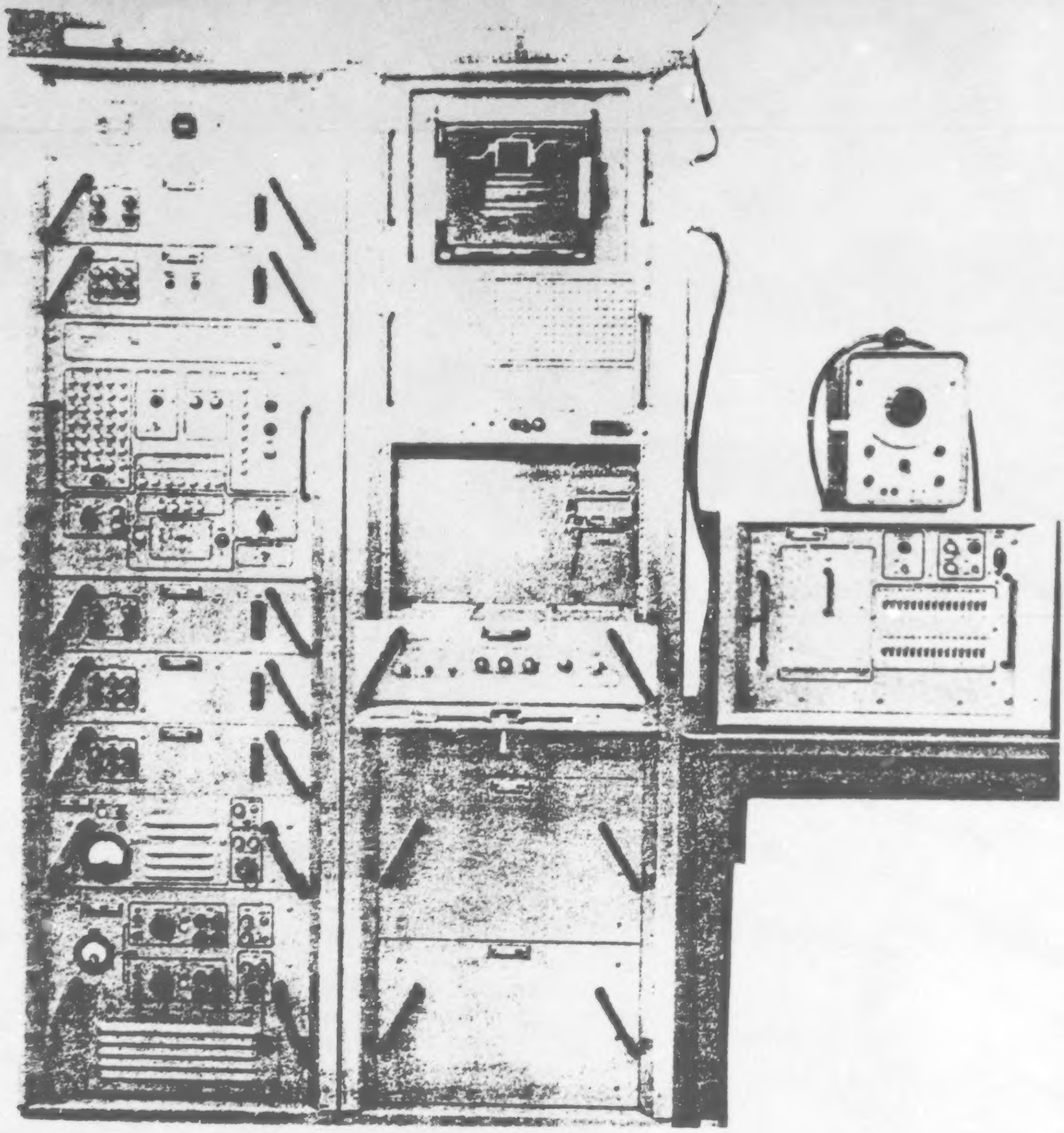


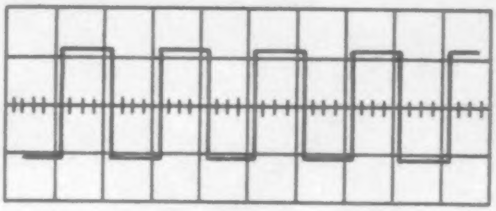
Figure 104. Card tester bench setup, 465L.

of a frequency and pulse width that is compatible with the equipment being tested.

9-27. Refer to figure 103, the card test set, and you can see that the test set contains 30 *test circuit selector* switches. These control input voltages and signals, provide resistive loads to the assembly under test, and supply outputs to an externally connected oscilloscope or multimeter. At the beginning of a performance test, the hinged card receptacle subchassis (callout A) is pulled out from the front panel of the set. There are five connectors or jacks on the receptacle which accommodate the various printed circuit assembly types (callout B). The 36 test jacks (callout C) enable you to monitor all of the assembly outputs. The printed circuit board is inserted into the receptacle with the component side forward, as shown in figure 103. There is a lamp located behind the assembly which provides a shadow of the etched printed wiring on the reverse side. This feature enables you to locate wiring junctions and defects or breaks in the etching (run).

9-28. The test procedures for this test set, TS1996/FYQ, are covered in TO 31S5-

TABLE 6
TEST PROCEDURE

Step	Operation of Test Equipment	Point of Test	Performance Standard
5	Set POWER INPUT ON-OFF switch to OFF. Set TEST CIRCUIT SELECTOR switches to the following: 1-C, 2-D, 4-I, 5-J, 7-D, 15-B, 18-B, 24-F, 25-F, 26-I, 28-D, 29-C, and 30-I. Set all others to A.		
6	Set POWER INPUT ON-OFF switch to ON. Adjust oscilloscope horizontal display for 50 usec/CM.	2, 24	Waveform 5  V_o = 0 ± 1V V_1 = -11 ± 1V T_d = 50 usec T_r = 1.5 usec T_f = 1.5 usec

2FYQ-7. Each test procedure includes the circuit description, the schematic diagram, and the waveforms for the circuit under test. For example, the assembly shown plugged in the tester in figure 103 is described in the TO as assembly 4581219-G1, consisting of two flip-flops, two AND gates, an OR gate, and a differentiator. The flip-flops are used in applications requiring negative setting, resetting, and triggering. Complementary transistor output circuits provide pulses with fast rise and fall time. The card tester is then set up to measure the performance of these circuits. Table 6 shows typical steps involved in the test procedure. If the output is below the performance standard, you can then go to the schematic diagram and make further checks toward isolating the malfunction component.

9-29. **Power Supply Test Set, TS1846/FYQ.** TS1846/FYQ. One of the most important pieces of equipment in any data processing system is the power supply. Without the power supply, the system is of no use. Therefore, it is very important that you be able to maintain the power supplies in your system to keep the downtime to a minimum. To repair the power supplies, you must be able to use the test set that is provided with your system.

9-30. The test set shown in figure 105 (in the workbook) is a typical set which is used to maintain four types of power supplies in the 465L system. This test set is used to analyze power supply operation, to set overload calibration, and to isolate malfunctions.

9-31. **Functional Elements.** The functional elements of the test set include the variable power transformer circuit, the resistive load circuits, and the monitor meter circuit, as shown in figure 106. The elements that operate to perform a specific function or a group of related functions are described below.

9-32. *Variable power transformer circuit.* This circuit is used to control the input voltage to the power supply under test. In this way, the regulation of a power supply under varying input voltage conditions may be determined.

9-33. *Resistive load circuits.* The +12-volt or - 12-volt output of the power supply under test is applied to various configurations of fixed and variable load resistors which comprise the resistive load circuits of the test set. The resistive load circuits are used in the performance of static load tests, transient load tests, and overload calibration tests.

9-34. *Monitor meter circuit.* This circuit is connected in series with the output of the power supply under test and the selected resistive load circuits. An ammeter in the monitor circuit indicates the amount of current drain required to actuate the overload protective circuit of the power supply under test. The ammeter is also used to set current drains on a power supply when testing the power supply voltage regulation.

9-35. Operation. Let's now discuss the elements of the test set in terms of their function in relation to the operation of the controls and switches while testing a power supply. (Refer again to fig. 105)

9-36. *AC input.* The AC input function provides a variable AC voltage for the power supply under test. This voltage is available by turning front panel 120-VAC Input On/Off switch to ON and adjusting front panel AC input to power supply control T1 to the required voltage.

9-37. *Voltage polarity.* The front panel Voltage Polarity switch permits a positive or negative voltage from a power supply under test to be appropriately applied to the test set circuitry without changing inter-equipment cabling connections. Also, this switch insures that the correct voltage polarity is applied at all times to the load current monitor meter.

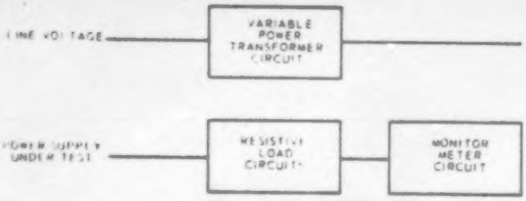


Figure 106. Functional elements, power supply test set.

9-38. *Static load.* The static load function provides a variable load for a power supply under test. Placing the front panel Static Load On/Off switch to the ON position and varying the Static Load control causes a resistive load to be presented to the power supply under test. This variable resistive load presents static loads in a range of 50 to 100 percent of the power supply rated output. The power supply DC output and ripple voltages are checked under maximum load conditions using an external meter or scope.

9-39. *Transient load.* The front panel transient load function provides a load step exercise to the power supply under test in order to observe its recovery time. When the Transient Load On/Off switch is placed in the ON position, the Transient Load control is adjusted to provide a load of 20 to 80 percent of the rated output. Once the control is adjusted to a desired load, the Transient On/Off switch is repeatedly cycled between ON and OFF positions to provide a transient load. During this time, an oscilloscope is used to observe the recovery time of the power supply.

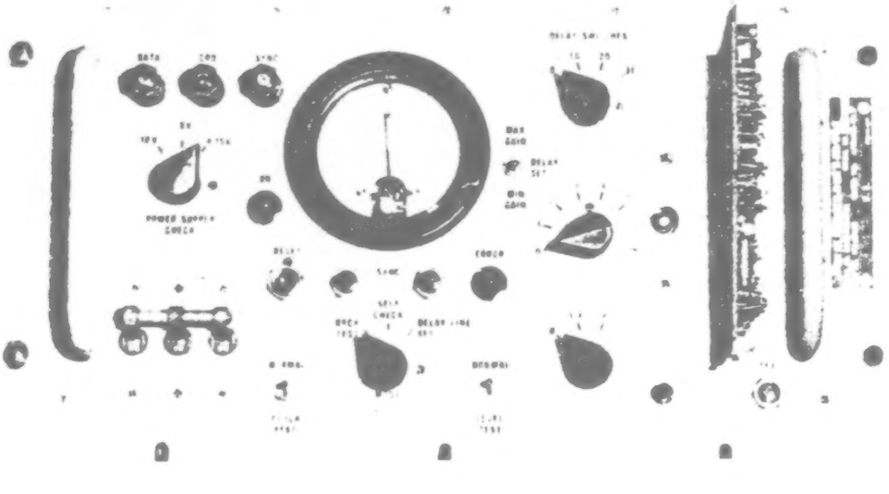


Figure 107. Trouble analyzer, AN/GPM-47.

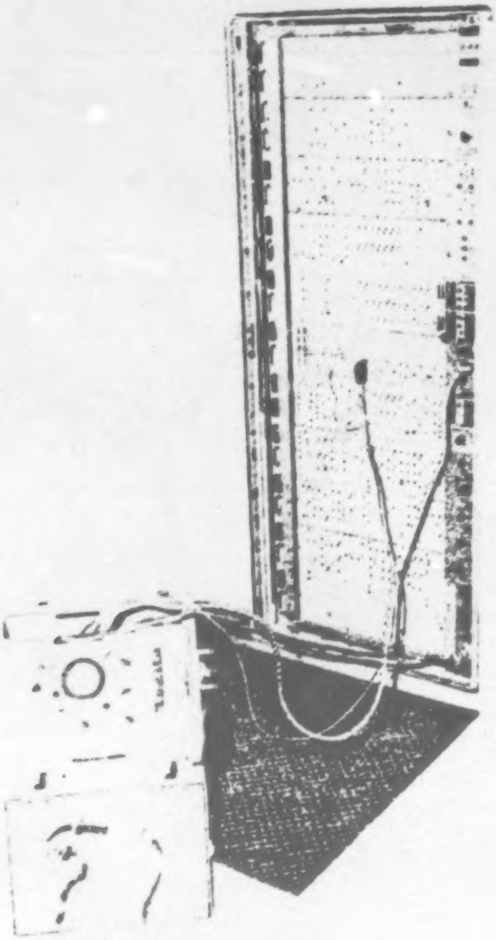


Figure 108. Trouble analyzer interconnected.

9-40. *Calibrate load.* The front panel Calibrate Load On/Off switch, in conjunction with the static load circuitry, provides for overload testing. While adjusting the static load control for a decreasing resistance, the meter is observed for the maximum current indication before a sudden reduction in power supply output occurs due to the overload protection circuits of the power supply under test. An oscilloscope is also used during this test to observe the sudden reduction in the power supply output.

9-41. The test set has a bank of front panel test jacks divided into two groups: power supply and test set. There are 50 test jacks, A through HH, associated with the power supply under test. Some or all of these test points are made available by using various types of inter-equipment cables connected between the test set and power supply. There are six test jacks, 3 through 8, associated with the test set group which permit access to test points within the test set. Both groups of test jacks are used with auxiliary test equipment to monitor voltage levels and waveforms.

9-42. Trouble Analyzer. The trouble analyzer used with the 412L system (see fig. 107) tests suspected assemblies without their being removed from the equipment cabinet. The analyzer is a small, portable digital device composed of a number of plug-in cards which are identical in most instances to the cards it tests. The meter and indicators on the analyzer work in conjunction with a test probe and probe indicator to provide the operator with simple GO or NO-GO results. This set isolates trouble to a faulty card, monitors assembly supply voltages, and aids in the adjustment of delay component cards. You may wish to use an oscilloscope in conjunction with the analyzer while troubleshooting or checking an assembly. If so, the analyzer has sync, data, and ground terminals available for this purpose. Data processors usually process data in both serial and parallel form, and the circuits that process that data must be checked. The trouble analyzer, for example, can compare two serial words bit for bit. One word is produced by the analyzer and is used as a standard. This standard word is processed by the circuits to be tested and then fed back to the analyzer for comparison with the original word. Other tests performed by this tester are:

- Logic level.
- Pulse presence.
- Clock test.

The particular test that you program the analyzer to perform is obviously determined by the circuit under test. The 412L equipment cabinets are composed of a number of racks. Test function switches that select programs for the analyzer are located on these racks.

9-43. Figure 108 shows the same trouble analyzer interconnected to an equipment rack. Notice that there is a multilead cable connected from the analyzer to a plug midway up to the right-hand side of the rack. The test function switches are adjacent to this plug. The black plug in the center of the rack is inserted in one of the many possible signal test jacks. You can see from figure 107 that the analyzer is relatively small and can be easily moved to whatever rack needs testing.

10. Category I and II Test Equipment Calibration Program

10-1. As a data processing repairman, you not only must use test equipment but also must determine that it is in proper working condition and that it is properly calibrated. Because of the many different types of test sets and the necessity for accurate standards with which to check these sets, test equipment has been divided into categories; the responsibility for the calibration of equipment within these categories is assigned to various organizations.

10-2. For maintenance purposes, test equipment is divided into four categories, but only the first two apply to you as a maintenance man.

- Category I — Category I includes all operational test equipment installed in a system as an integral part of the system. Examples of this are ammeters, voltmeters, and oscilloscopes that are built into the system.
- Category II — Category II includes all equipment that is used to check Category I test equipment. This group may include devices such as multimeters, counters, and frequency meters.

10-3. All equipment that you are responsible for falls into Categories I and II. However, this doesn't mean that you are responsible for all Category I and II test equipment. There are two organizations that have the primary responsibilities for maintaining all equipment in Categories I and II. These are (1) the using organization of which you are a part and (2) the base Precision Measurement Equipment Laboratory (PMEL). As part of the using organization, you have the responsibility for the calibration of all Category I and II equipment with the following exceptions:

- Base PMEL calibrates all general-purpose and commercial Category II test equipment that can be removed to the PMEL. This does not include test equipment that must be calibrated while it is an integral part of data processing equipment.
- Maintenance of test equipment that requires special skills or special equipment (whether it be Category I or II) that is available only at the PMEL is the responsibility of the base PMEL. However, you do have responsibilities for maintenance of test equipment, and these are outlined in the technical orders.

10-4. Technical Orders. The TOs listed below are those most used in identification of procedures for calibration of Category I and II test equipment.

10-5. *TO 00-20-10-6*. This TO, *PME Scheduling and Maintenance Data Collection Procedures*, establishes procedures for the implementation and operation of an automated system for scheduling and inventory control of precision measurement equipment.

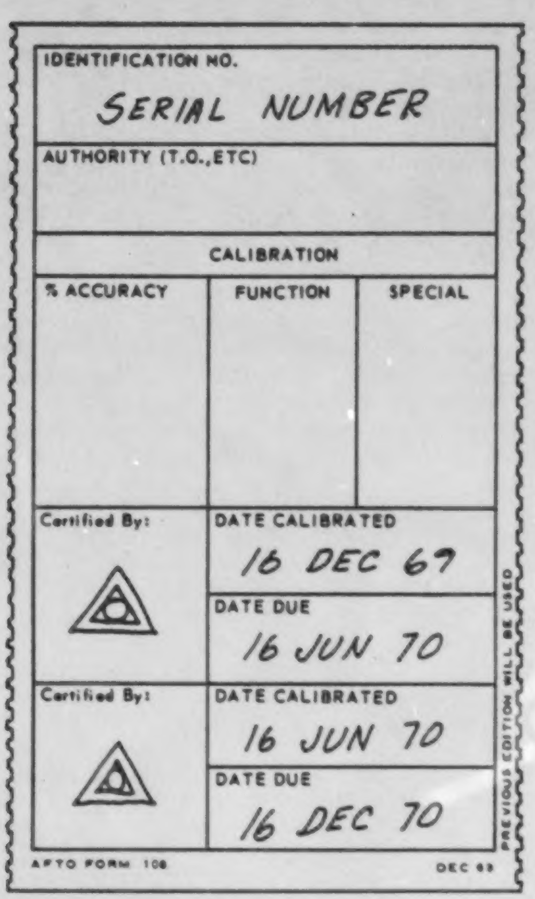
10-6. *TO 33-1-14*. Titled *Calibration and Certification of PME*, this TO provides information such as calibration responsibilities, PME quality control, PME scheduling and data collection, and preparation and use of calibration forms and labels.

10-7. *TO 33K-1-100*. This TO, *Calibration Technical Orders—Responsibilities and Calibration Measurement Areas*, designates the organization responsible for calibrating specific items of PME, items not requiring calibration, and the publication pertinent to the equipment when either the type number or manufacturer's part number is known. For example, the AN/FYM-2 covered earlier is classified as Category II and the maintenance technical order is 33D7-49-14. However, the calibration instructions, such as calibration intervals, performance standards, etc., are covered in TO 33K-1-61.

10-8. Scheduling of Calibration. The PMEL should automatically schedule your test equipment and call for it when calibration is required. Normally, the materiel control office in the maintenance organization has the responsibility of seeing that the equipment is delivered to PMEL on the date scheduled and then returned to the maintenance work center when calibration is completed. Materiel Control also normally handles unscheduled maintenance requests on equipment that the PMEL is responsible for. However, test equipment that is an integral part of your data processing system and cannot be removed, but which requires special skills and equipment for calibration, may be calibrated by the using organization with the assistance of PMEL personnel.

10-9. Standards of Calibration. Each piece of test equipment must be calibrated against a standard. The standard used must be designated, and when all like items and items can be checked and aligned with this standard, they are called lower echelon items. The piece of test equipment used as a standard must in itself be calibrated before it can be used as a standard; therefore, various levels of certification are established. The ultimate or highest echelon used for certification of all standards in the United States is the National Bureau of Standards for Electrical and Electronic Equipment, Boulder, Colorado.

10-10. You may have standards in your shop; if so, these standards are called *shop standards*. A shop standard is defined as a precision measurement equipment known to have been officially calibrated and certified for use as a comparison in checking other items in the maintenance shop. These standards are



IDENTIFICATION NO. SERIAL NUMBER		
AUTHORITY (T.O.,ETC)		
CALIBRATION		
% ACCURACY	FUNCTION	SPECIAL
Certified By:	DATE CALIBRATED 16 DEC 69 DATE DUE 16 JUN 70	
Certified By:	DATE CALIBRATED 16 JUN 70 DATE DUE 16 DEC 70	

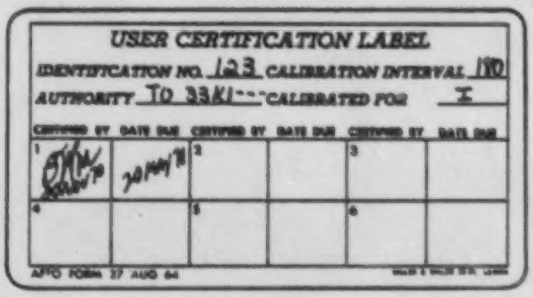
AFTO FORM 108 DEC 63

PREVIOUS EDITION WILL BE USED

Figure 109. AFTO Form 108, certification label.

not used for routine maintenance functions unless an emergency exists or all like items are inoperative.

10-11. An example of a shop standard is the model 269 multimeter discussed earlier. Shop standards are classified as Category III test equipment. The same meter may also be used as a standard by PMEL. However, when used by PMEL the standard is classified as Category IV equipment. From this you can see that the same meter or other test set may fall into any of three categories, depending on its use. If used in regular maintenance, it is Category II; as a shop standard, it is Category III; and as a PMEL standard, it is Category IV.



USER CERTIFICATION LABEL

IDENTIFICATION NO. 123 CALIBRATION INTERVAL 180

AUTHORITY TO 33K1--- CALIBRATED FOR I

CERTIFIED BY	DATE DUE	CERTIFIED BY	DATE DUE	CERTIFIED BY	DATE DUE
1	20 May 70	2		3	
4		5		6	

AFTO FORM 27 AUG 64

Figure 110. AFTO Form 27, User Certification Label.

10-12. As another example of how a test set could fall into more than one category, consider the oscilloscope. Some data processing systems have an oscilloscope, modified and installed, as an integral part of the system. Notice the oscilloscope in figure 102 (in the workbook). This oscilloscope is part of the AN/GPM-50 and, as a result, falls into the Category I test equipment area.

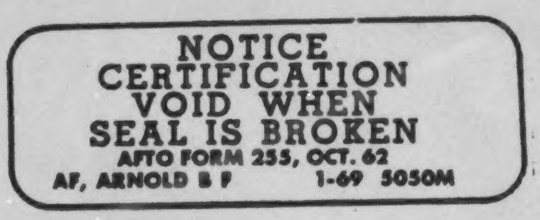
10-13. It is extremely important that you be thoroughly familiar with your test equipment. Knowing how to use it effectively and care for it properly cannot be overemphasized. Properly used, it will provide you with years of dependable service. Know its capabilities and it will aid you immeasurably in the performance of your job.

10-14. **Responsibility of Calibration.** Delineation of responsibilities for calibration/certification of PME, definition of the categories of PME, assignment of calibration intervals, and procedures and specifications for accomplishing calibration, repair, and modification of all categories of PME are contained in TOs 33-1-14, 33K-1-100, or Weapon/Equipment System Series Calibration Measurement Summaries, Maintenance TOs, and TCTOs. TO 33-1-14 prescribes procedures for clarification of conflicting instructions, correcting errors, and recommending changes to calibration intervals.

10-15. **Forms and Labels for Calibration.** This section covers the forms and labels that you will encounter most frequently when using precision measuring equipment.

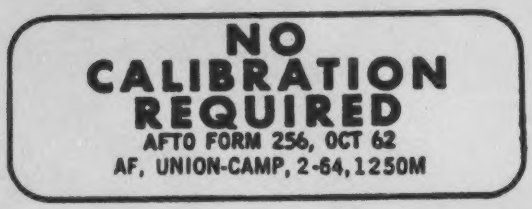
10-16. *Certification label (AFTO Form 108).* This label, shown in figure 109, is completed and affixed to standards and PME certified by all Air Force calibration laboratories. This label is filled out and affixed by authorized PMEL personnel.

10-17. As indicated in figure 109, when the piece of equipment is calibrated, the technician puts a certification stamp in the Certified By block. The next due date is then entered in the adjacent Date Due block. After the second inspection and all blocks are filled, the label is removed and a new one is affixed by authorized PMEL personnel at the next inspection. The only time you, as a data processing repairman, will make entries on this form is when you are authorized by special order to certify calibration.



NOTICE
CERTIFICATION
VOID WHEN
SEAL IS BROKEN
AFTO FORM 255, OCT. 62
AF, ARNOLD B F 1-69 5050M

Figure 111. AFTO Form 255, certification void seal.



NO
CALIBRATION
REQUIRED
AFTO FORM 256, OCT 62
AF, UNION-CAMP, 2-64, 1250M

Figure 112. AFTO Form 256, No Calibration Required.

10-18. *Certification label (AFTO Form 27).* This label, shown in figure 110, is completed and affixed to equipment designated for calibration by the using organization. The label is prepared as follows:

- Identification No. Enter the equipment serial number or appropriate base inventory number of the equipment receiving calibration.
- Calibration Interval. Enter the calibration interval for the equipment in days. For example, 3 months is 090 days; 6 months is 180 days.
- Authority. Enter the technical order number or special instruction source which contains the calibration procedure of the specific equipment.
- Calibrated For. Insert specific type of calibration conducted on the equipment. If equipment has been calibrated on all ranges, enter the word "All."
- Certified By. The organization's quality stamp or the initials of the maintenance inspector are entered in this block. The date calibration was performed is entered along the left outer margin, in the same block with the initials or stamp certification.
- Date Due. The date the equipment is due for recalibration is entered in the next Date Due block by the technician who calibrated the equipment.

10-19. The certification label is affixed to a clean surface in a conspicuous, clear area on the equipment. On small items, the label may be affixed to a plain manila tag and tied to the equipment. Items which, by their nature, will not allow affixing of the label may have the label affixed to their container.

10-20. On complex PME, such as test stands or checkout consoles, one certification label for the stand or console will suffice for all items that are an integral part of the stand or console. Items are considered an integral part if they are hooked up in the total complex in such a way that they must be calibrated in, and as a part of, the stand or console to assure the integrity of the complex.

10-21. *Certification void seal (AFTO Form 255).* Refer to figure 111. This is a seal which PMEL attaches to all standards and to items of PME which have adjustments that affect calibration. This seal is not required on mechanical zero adjustment screws located on electrical indicating meters. This seal is applied in such a manner that any attempt to repair or adjust the equipment will result in breaking the seal. When the seal is broken, certification of calibration accuracies is no longer valid. Recertification must be accomplished by PMEL in the event calibration accuracy is in question.

10-22. *No Calibration Required label (AFTO Form 256).* TO 33K-1-100 is used to determine which items are to be labeled with AFTO Form 256 (refer to fig. 112). The forms are obtained from the local PMEL. Usually, PMEL will furnish a stamped or initialed form to the user for application. However, the form can be certified by the user simply by initialing it.

10-23. There are other forms and labels used in conjunction with PME; however, the ones covered here are the most important.

MODIFICATIONS

Chapter 5 of this publication has (have) been deleted in adapting this material for inclusion in the "Trial Implementation of a Model System to Provide Military Curriculum Materials for Use in Vocational and Technical Education." Deleted material involves extensive use of military forms, procedures, systems, etc. and was not considered appropriate for use in vocational and technical education.

54. All operational test equipment installed in a system as an integral part of the system.

55. Test equipment used to check Category I test equipment.

56. Precision Measurement Equipment Laboratory (PMEL).

57. 1. *e.*
    2. *c.*
    3. *b.*
    4. *a.*

58. United States National Bureau of Standards for Electrical and Electronic Equipment.

59. A piece of PME known to have been officially calibrated and certified for use as a comparison in checking other items in a maintenance shop.

60. 1. *c.*
    2. *d.*
    3. *a.*
    4. *b.*

MODIFICATIONS

Page 28 of this publication has (have) been deleted in adapting this material for inclusion in the "Trial Implementation of a Model System to Provide Military Curriculum Materials for Use in Vocational and Technical Education." Deleted material involves extensive use of military forms, procedures, systems, etc. and was not considered appropriate for use in vocational and technical education.

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Index

A

AF Form 623, Training Record (2-10-12; Figs. 2-5)*
AFM 39-1, *Airman Classification Manual* (2-13)
AFM 66-1, *Maintenance Management* (11-2)
AFM 100-12, *Communications-Electronics* (11-3)
AFR 66-8, *Maintenance Evaluation Program* (5-29)
AFR 400-44, *Corrosion Prevention and Control Program* (5-29)
AFTO Form 349/350 (12-4; 14-18, 25)
Air Materiel Areas (13-5, 6; 14-26)
Analysis, definition of (3-4-6)
Assignment and Supervision of Work (1-11)
Assignment Rules (1-12)
ATC Course Numbers, definition of (2-6, 7)

C

Calibration, certification label, AFTO Form 27 (10-18)
  certification label, AFTO Form 108 (10-16)
  certification void seal, AFTO Form 255 (10-21)
  forms and labels (10-15-23)
  National Bureau of (10-9)
  No Calibration Required label, AFTO Form 256 (10-22)
  responsibility (10-14)
  shop standard (10-10)
Career Development (2-8)
Card Tester (9-15-17)
  AN/GPM50 (9-19-24)
  TS 1996/FYQ (9-25-28)
  416L (9-18)
Chief of Maintenance (12-2)
Components, replacement techniques (4-2)
Connector, nomenclature (3-64, 5)
  remove, replace procedure (3-66)
  types (3-59)
Corrosion, causes (5-11-13)
  cleaning (5-19-28)
  definition (5-1-3)
  electrochemical (5-6)
  prevention (5-14-18)
  requirements for (5-5)
  terms (5-4)

D

Desoldering (4-26)
Demonstration, the (2-21)
Differential Voltmeter (8-62-70)
  controls (8-66-70)
  DC measurement (8-71)
  high resistances measurement (8-77-79)
  voltage excursions measurement (8-76)
  output voltage set (8-75)
  used as a VTVM (8-72, 74)
Discussion, the (2-21)
Drawer Tester (9-2-14)
Dual-Channel OJT, definition of (2-8)

E

Emergency Unsatisfactory Materiel Report (11-6)
Engineering Change Proposals (ECP) (13-1, 3)
Equipment, automated recording system (15-9-13)
  history of (15-2)
Equipment Identification (see Technical Orders)
  coordinate coding (6-17)
  coordinate numbering (6-14)
  location coding method (6-15)
  location numbering method (6-12)
  sequential coding (6-16)
  sequential numbering (6-13)
  unit numbering method (6-3)
  manual recording system (15-5-8)
  recording of (15-4)
Evaluate Performance of Personnel (1-29-35)

F

Flux (3-18)
  defined (4-24)
Fuses and Fuse Holders (3-36)
  damage signs (3-42)
  melting point (3-38)
  numbering (3-37)
  remove and replace procedures (3-43, 44)
  size and use (3-41; Table 2)

G

Galvanic Cell (5-6-9)
General Plan for AF Training (2-2)
Graduate Evaluation Programs (2-28-33)

H

HOW MAL Codes (12-5, 6, 7; 15-10)

---

*Indicates para number, unless otherwise stated.

I

- Indicator controls, 545A oscilloscope (8-61)
- Inspect and Service Electrical and Mechanical Connectors (3-58-67)
- Inspect and Service Read/Write Heads (3-17)
- Inspection Checklist (1-26)
- Inspection, connectors (3-63)
  - elements of (1-26)
  - responsibilities of (1-25)
- Instruction, techniques of (2-20)
- Interim Engineering Change Authorization (13-2, 3)
- Inventory Manager (13-1)

J

- Jacks (7-11)
- Job Proficiency Development (2-8,*b*)

L

- Lamp and Lamp Sockets (3-24; Table 1)
  - neon indicator 93-29-32)
  - offset prong (3-27)
  - remove and replace procedure (3-25)
  - screwbase (3-24, 5)
  - subminature (3-33, 34)
- Lateral OJT (2-4)
- Lecture, the (2-21)
- Lights (3-21-36)

M

- Maintenance Control (12-2)
- Materiel Control (12-6)
- Maintenance Data Collection MDC (13-1, 4; 14-3, 6)
  - analysis (1-27)
- Measurement of DC Voltages (8-71)
- MIL-STD-1250, *Corrosion Prevention and Deterioration Control* (5-29)
- Multimeters, applications (8-97-102)
  - description (8-80, 81)
  - uses (8-86-96)

O

- OJT, Dual-Channel (2-8)
  - general plan for (2-2)
  - lateral training (2-4)
  - records, AF Form 623 (2-10-12)
  - maintenance (2-9)
  - used as a tool (2-18, 19)
- Origin of TCTO (Sec 13)
- Oscilloscope, purpose (8-2)
  - 545A (8-3)
  - controls (8-4-8)
  - indicator controls (8-61)
  - use of controls (8-9-40)
  - use of external sweep (8-42)
  - use of single sweep (8-41)
  - use of square-wave calibrator (8-58-60)
- Oxide Deposits (3-18)

P

- Personnel, evaluation of (1-29-35)
- Performance, the (2-21)
  - routines (3-2)
  - standard, definition of (1-21-24)
- Power Supply Test Set, TS 1846/FYQ (9-29-41)
- Priorities, definition of (1-20)
- Production Controls (1-19)

Q

- Quality Control (12-3; 14-17, 34, 35)
- Quality Unsatisfactory Materiel Report (11-6)

R

- Rating Forms, completion of (1-29-31)
- Records (12-4; 14-25)
- Record Jacket File (15-14, 15)
- Repair/Replace Defective Components (4-1-58)
- Repair, Replacement, General Tasks (4-45)
  - removal of component task list (4-46, 47)
  - special areas (4-49-58)
- Routine Unsatisfactory Materiel Report (11-6)

S

- Sniffing (4-31-33)
- Solder, joints (4-25)
  - nature of (4-11-23)
  - application of solder (4-41-43)
  - desoldering (4-8)
  - forming (4-38-40)
  - preparation for (4-34-37)
  - terms (4-9)
  - tools (4-10)
- Specialty Training Standard (2-14, 15, 16)
- Standard Configuration Management System (15-9-13)
  - action code (15-10)
- Supervision, adjusting to the new job (1-9, 10)
  - categories of (Ch 1, Intro-3)
  - definition (1-1)
  - determining lines of authority (1-8)
  - job assignment (1-5)
  - orientation (1-2)
  - responsibilities (1-4)
  - specific work areas (1-7)
- Switch (3-45-57)
  - micro (3-54)
  - pushbutton with lamp indicator (3-51)
  - repair or replace procedures (3-56, 57)
  - spring-loaded pushbutton micro (3-50)
  - toggle, (3-49)
- System Support Manager (13-1)

T
TCTO, applicability (14-13)
  event type (15-10)
  format (14-12)
  installation (14-29-36)
  immediate action (14-2, 3, 17; 15-10)
  record action (14-2, 11; 15-10)
  routine action (14-2, 6, 7, 9, 10; 15-10)
  routine, category I (14-2, 9)
  routine, category II (14-2, 10)
  routine, class IVA (14-2, 6, 17)
  routine, class IVB (14-2, 7)
  safety (14-6)
  urgent action (14-2, 4, 17; 15-10)
Technical Orders (3-7-9)
  remove, replace (4-4-7)
  series -2, series -3, series -6WC, (6-8, 9, 10, 11; 7-3)
  use to validate repaired equipment (1-28)
  0-1-31-X, *Numerical Index and Requirement Table* (11-10)
  0-0-5-1, *AFTO System* (11-4)
  00-20-1, *Preventive Maintenance Program* (11-5)
  00-20-2-1, *MDC, AFTO Forms, and General Documentation Procedures* (11-5)
  00-20-4, *Historical Records and Configuration Management* (11-5; 12-5)
  00-20-2-8, *ON EQUIPMENT Maintenance Documentation for C-E-M Equipment* (11-5)
  00-20-2-10, *OFF EQUIPMENT Maintenance Documentation* (11-5)
  00-20-8, *Ground C-E-M Records* (11-5)
  00-20-10-4, *Base Level Mechanized TCTO Reporting System* (11-5; 12-5; 15-10)
  00-20-10-6, *PME Scheduling and MDC Procedures* (10-5)
  33-1-14, *Calibration and Certification of PME* 10-6)
  33K-1-100, *Calibration TO—Responsibilities and Calibration Measurement Areas* (10-7)
  00-35D-54, *USAF Materiel Deficiency Reporting System* (11-6)
Test Equipment, category II (10-2)
  category I (10-2)
Test Set, trouble analyzer (9-42, 3)
Time Compliance Technical Order, definition of (Ch 5, Intro-2)
Training (Sec 2)
Training Methods (2-21)
  techniques (2-22, 23)

U
Unit Manning Listing (2-17)

V
Vertical Controls, 545A oscilloscope (8-43-57)

W
Wicking (4-27-30)
Wiring Diagrams, alphanumeric codes (7-6, 9)
  elements (7-2)
  horizontal connector listing (7-7)
  identification of connecting points (7-6-9)
  interpretation of (7-1-9)
  jacks (7-11)
  multi-routed signal tracing (7-7)
  vertical connector point listing (7-6)
  table (7-9)
Work, assignment and supervision of (1-11)
Work Center (12-9)
Work Load Control (12-8)
Work Methods (1-15, 16, 18)

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TABLE OF CONTENTS

Study Reference Guide

Chapter Review Exercises

Answers For Chapter Review Exercises

Volume Review Exercise

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STUDY REFERENCE GUIDE

1. *Use this Guide as a Study Aid.* It emphasizes all important study areas of this volume.

2. *Use the Guide as you complete the Volume Review Exercise and for Review after Feedback on the Results.* After each item number on your VRE is a three digit number in parenthesis. That number corresponds to the Guide Number in this Study Reference Guide which shows you where the answer to that VRE item can be found in the text. When answering the items in your VRE, refer to the areas in the text indicated by these Guide Numbers. The VRE results will be sent to you on a postcard which will list the *actual VRE items you missed.* Go to your VRE booklet and locate the Guide Number for each item missed. List these Guide Numbers. Then go back to your textbook and carefully review the areas covered by these Guide Numbers. Review the entire VRE again before you take the closed-book Course Examination.

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Guide
Number

Guide Numbers 100 through 120

100 Supervision and Training; Supervision; pages i–6

101 Training; pages 6–13

102 General Maintenance; Performance Routines, Repairs, and Operational Checks: Analysis–Switches; pages 14–21

103 Performance Routines, Repairs, and Operational Checks: Types of Switches and Their Related Applications–Typical Removal and Replacement of Multiple Connectors; pages 21–27

104 Repairing or Replacing Defective Components: Replacement Techniques–The Nature of Solder; pages 27–35

105 Repairing or Replacing Defective Components: Flux–Conclusions; pages 35–43

106 Controlling Corrosion; pages 43–50

107 Equipment Identification; Using Alphanumeric Equipment Numbering Systems; pages 51–55

108 Interpreting Wiring Diagrams and Correlating the Diagrams with Connectors, Interconnecting Cables, Cabinets, and Remote Equipment; pages 55–61

Guide
Number

109 Test Equipment; Operating Standard Test Equipment: Oscilloscopes–"B" Intensified By "A"; pages 62–69

110 Operating Standard Test Equipment: Delay-Time Frequency Measurement–Gain Adjust; pages 69–75

111 Operating Standard Test Equipment: Use of Square-Wave Calibrator–Measurement of Voltage Excursions About a Nominal Value; pages 75–81

112 Operating Standard Test Equipment: Measuring High Resistances–Checking Transistors; pages 81–85

113 Special Test Equipment; pages 85–94

114 Category I and II Test Equipment Calibration Program; pages 94–97

115 Equipment Modification; Technical References; pages 98–100

116 Responsibilities of the Maintenance Organization; pages 100–101

117 Organization of a TCTO; pages 101–102

118 Installation of a TCTO; pages 102–107

119 Recording a TCTO; pages 107–110

120 The Program in Perspective; pages 110–111

CHAPTER REVIEW EXERCISES

The following exercises are study aids. Write your answers in pencil in the space provided after each exercise. Immediately after completing each set of exercises, check your responses against the answers for that set. Do not submit your answers to ECI for grading.

MODIFICATIONS

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CHAPTER 2

Objective: To determine requirements and skills which are necessary so that you can perform routines, repair actions, and control corrosion.

1. Name five tasks which fall in the category of preventive maintenance routines and repairing or replacing of electronic components. (3-1)

2. What would be the result of a poor general maintenance program? (3-2, 3)

3. List the TO series which will provide step-by-step instructions of PMIs. (3-7)

4. If airflow is decreased within an equipment cabinet because of faulty maintenance, what may result? (3-12)

5. What are the two most dangerous enemies of magnetic tape and drum systems? (3-17)

6. Why is it important to remove power before installing a new lamp socket? (3-25)

7. What are the two uses of the NE68 lamp? (3-32)

8. Where are fuses normally found in a circuit? (3-37)

9. What is the approximate melting temperature of the current-carrying element of a fuse? (3-38)

10. What effect will a large decrease in resistance have on a circuit fuse? (3-39, 40)

11. What are most common causes of fuse holder damage? (3-42)

12. The method used in replacing a fuse holder is much the same as replacing ____________________. (3-43, 45)

13. What are two broad uses of switches in computer systems? (3-46)

14. What are the four most common switches in use today? (3-49–54)

15. When replacing a switch, you see the letters NO, NC, and C on the switch. What are the meanings of the letters? (3-57)

16. What three letters are not used to label pin connections of a connector? (3-59, 60)

17. What would be the most probable causes of a recessed pin in an electrical connector? (3-63)

18. How are the connectors labeled for a printed circuit board? (3-64, 65)

19. What is the primary purpose of the –4 TO, illustrated parts breakdown? (4-6)

20. What are the usual causes of cold solder joints? (4-9)

21. Define flow point. (4-9)

22. The point at which an alloy starts to melt is called ______________________. (4-9)

23. What is tinning? (4-9)

24. What is the primary purpose for using a thermal shunt? (4-10)

25. What is the most likely way to ruin a transistor or diode when soldering? (4-10)

26. Is soldering a metallurgical process or a physical adhesion? (4-13)

27. Explain why a soldered connection is better than one that is bolted or wired. (4-14, 15)

28. What is the purpose of using flux in the soldering process? (4-24)

29. What type of flux is required for electronics soldering? (4-24)

30. List two methods used in desoldering. (4-29–31)

31. In cleaning a circuit board for soldering, what would be the proper cleaning tool to use? (4-37)

32. What is the purpose of the stress relief? (4-39)

33. Who is most responsible for corrosion control? (5-2, 3)

34. Name the three types of electrochemical cells. (5-6)

35. What causes the dew point to vary in equipment? (5-11)

36. What causes uniform etching corrosion? (5-11)

37. Why does corrosion usually occur in and around spot welds? (5-12)

38. What is the physical appearance of corroded aluminum? (5-12)

39. What two preventive maintenance actions are used to control corrosion? (5-14)

40. What are two effective corrosion-preventive coatings? (5-15–18)

41. What type cleaner would be used on oily or fatty soils? (5-19–22)

42. When would you use mechanical cleaning techniques rather than chemical? (5-28)

43. What AFR contains the corrosion prevention and control program? (5-29)

44. Does corrosion control play an important part in the reliability of the system? (5-30)

14. Which units of an equipment set are likely to have interconnecting cables? (7-1)

15. What three parts of electronic equipment serve the same general purpose of linking elements of a system together? (7-1)

16. What are two methods of making a wiring list? (7-1)

17. What distinctive advantage does a bay or rack have over a chassis? (7-2)

18. Which unit in a set is similar in purpose to a chassis? (7-2)

19. Why is the service manual useful for identification of equipment wiring? (7-3)

20. Refer to figure 52. Before its full location is known, what other information does jack A1J17–6 need? (7-6; Fig. 52)

21. The RM3 pulse is not being received at the SIF unit J503103—4. List the possible test points between its origin and J503103—4. (7-7; Fig. 53)

22. Refer to figure 53. Where is the output from assembly 616, J616, routed to? (7-7; Fig. 53)

23. Refer to figure 56. Do callouts 1 through 5 on a table listing refer to data location of the input or output of a signal? (7-9; Fig. 56)

24. The locations listed in the From and To (Fig. 56) columns under MDF title, identify locations physically located in which unit? (7-9; Fig. 56)

25. Cable 59 (Fig. 57) will route the DO pulses from where? (7-9; Fig. 57)

26. Refer to figure 58, situation B, and identify the following elements: HH 16 W64 A J6. (7-9; Fig. 58)

CHAPTER 4

Objective: To show an understanding of the uses of AGE equipment and apply this understanding to problems defined in the text.

1. Which oscilloscope is used as the example in Chapter 4? (8-3)

2. The front panel controls on the oscilloscope can be divided into three main areas of control. List them. (8-4)

3. The ______________________________ are included in the Horizontal Display control. (8-5)

4. Explain the purpose of the time base A group of controls. (8-6)

5. What portion of a display is presented when the 5X magnifier switch is on? (8-6; Fig. 61)

6. From the function in the right column, select the control setting in the left column which most closely identifies the control's use. (8-6)

Setting

_____ 1. AC and DC
_____ 2. AC LF REJECT
_____ 3. AUTOMATIC
_____ 4. HY SYNC

Function

a. Use of an RC filter is to reject 60-hertz or lower frequencies to prevent triggering the scope when both high and low signals enter the scope.
b. Internal circuits connect the triggering source directly to the sweep-gating MV to synchronize with the triggering waveform.
c. Provides the input with a low-frequency MV which can lock in with input signals from 50 hertz to 2 megahertz.
d. Controls the display positioning of a waveform by locking to the DC level or eliminating the DC level of the input signal.

7. What is the function of the Trigger Slope selection switch? (8-6)

8. Which control selects the position on the triggering waveform, the point where triggering occurs? (8-6)

9. When used, preset on the Trigger Level control provides a _______________ at a predetermined level to cause triggering. (8-6)

10. What are the maximum and minimum DC levels of voltage which can be preset? (8-6; Fig. 64)

11. Solve the following problems using the formula $f = \frac{1}{T}$.

a. A sine wave requires 2 centimeters for one complete cycle. The Time Per Centimeter control is set to 1 microsecond. What is the frequency?
b. A 100-kHz signal is being displayed and one cycle occupies 4 centimeters on the display. What is the setting of the Time Per Centimeter control? (8-10–14)

12. Explain the label "B" INTENSIFIED BY "A." (8-18–20)

13. List the control conditions which must be set for a "B" INTENSIFIED BY "A" trace. (8-21–8-23)

14. Explain how the intensity modulation of the "A" trace results in greater intensity of a portion of the display. (8-22, 23)

15. Using figure 66,B, of the text as an example, and the Delay-Time Multiplier, what reading would you expect to read on the multiplier scale at the end of *one* cycle if the scale read zero at the beginning of the graticule? (8-29–33; Fig. 66,B)

16. If the Delay-Time Multiplier control is used to measure a square wave or rectangular waveform, what two types of information can it provide? (8-33, 34)

17. For an "A" DELAYED BY "B" presentation, what controls must be used? (8-36, 37)

18. For "A" DELAYED BY "B" presentation, what unblanking pulse is inhibited? (8-36, 37)

19. What occurs when the Horizontal selector control is turned to "A" DELAYED BY "B"? (8-36, 37)

20. What useful purpose does the single sweep serve? (8-40, 41)

21. The vertical input unit, type CA, can process in various ways. List the different ways. (8-43–45)

22. Calculate the amplitude of the signal shown in figure 76 of the text if the Volts/CM switch is in the .2 position. (8-47)

23. To obtain the DC reference of an AC signal, what conditions must be established on the input unit? (8-48, 49; Fig. 60)

24. What is the primary oscilloscope operation difference when using ALTERNATE mode or CHOPPED mode selections on a CA preamp? (8-51, 52)

25. One of the most valued uses of the square-wave calibrator on an oscilloscope is for ______________ ______________________________. (8-58, 59)

26. List the four indicator controls on the front of the 545A oscilloscope. (8-61; Fig. 60)

27. Can a differential voltmeter measure AC voltages? (8-62)

28. Name the three uses of a differential voltmeter. (8-62)

29. What position must the Range selection switch be in when an unknown voltage is being measured? (8-67)

30. List the four major control switches on the 801B meter. (8-65–70)

31. If you try to calibrate the meter and an external voltage source is connected to the positive binding post, what condition results? (8-70)

32. What two ways can the meter be used when measuring DC voltages? (8-71)

33. If a circuit is designed to have a 4-volt output, how would the meter be set before an accurate VTVM measurement is made? (8-74; Fig. 82)

34. What is the maximum accuracy of the differential voltmeter? (8-73–75; Fig. 82)

35. To set a circuit to a specific output with an accuracy of ±.01 VDC, what must the meter controls be set to? (8-75)

36. The differential voltmeter may be used to measure resistances between ____________________ megohm and ______________ megohms. (8-77, 78)

37. List the uses of the multimeter shown in figure 89 of the text. (8-81; Fig. 89)

38. What precaution should be taken when measuring high voltage with the multimeter? (8-90)

39. The multimeter may be connected in various ways. Match the type of measurement in Column A with the type of connection in Column B. (8-81–96)

COLUMN A

1. _____ DC voltage
2. _____ AC voltage
3. _____ Direct current
4. _____ Decibel measurements
5. _____ Ohms

COLUMN B

a. Connected in series with the source.
b. Connected in parallel with the source.
c. Either series or parallel connected.

40. Explain the method used for checking a capacitor. (8-98)

41. List the steps used to check a diode. (8-101)

42. Which junction of a transistor amplifier will measure close to a 1:1 front-to-back ratio? (8-102)

43. Can a valid test with a multimeter usually be made of a transistor with two of the leads disconnected from the circuit? (8-102, 103)

44. Define the primary use for a special piece of test equipment. (9-1)

45. Explain the basic principle involved in the use of drawer and card checkers. (9-1–5)

46. The drawer tester shown in figure 90 can be operated in what two modes? (9-5–7)

47. List the support material that is needed to locate a trouble detected by the drawer checker. (9-8)

48. Is it necessary to self-check the drawer checker prior to actual use? (9-12)

49. What feature of modern EDPs makes the development and use of card checkers possible? (9-16)

50. Drawer checkers and card checkers have one *major* common element. Identify the element. (9-3, 17, 18)

51. List the four types of checks a tester may be designed to check. (9-19)

52. A power supply test set compares closely with what other type of test set? (9-29, 30)

53. What does the static load provide when a power supply is under test? (9-38)

54. Define Category I test equipment. (10-2)

55. Define Category II test equipment. (10-2)

56. What agency on base has prime responsibility for calibrating most standard test equipment used in work centers? (10-3)

57. Select the correct description of a technical order in Column B that matches the technical order number in Column A. (10-5-7)

COLUMN A

1. _____ TO 00-20-10-6
2. _____ TO 33-1-14
3. _____ TO 33K-1-100
4. _____ TO 33K-1-61

COLUMN B

a. Contains instructions for performance standards to calibrate the AN/FYM-2.
b. Contains data which specifies responsibility for calibration.
c. Contains information about the use of calibration forms and labels.
d. Identifies Category II maintenance as applicable to the AN/FYM-2.
e. Establishes procedures for inventory control and scheduling of PME.

58. What agency contains the highest standards of certification of standards? (10-9)

59. Define a "shop standard." (10-10)

60. Select the description in column B that identifies the form label in column A. (10-16-22)

COLUMN A

1. _____ Certification label (AFTO Form 108)
2. _____ Certification label (AFTO Form 27)
3. _____ Certification void seal (AFTO Form 255)
4. _____ No Calibration Required label (AFTO Form 256)

COLUMN B

a. A seal placed upon PME in such a manner that prevents the user from making internal adjustments.
b. A label used on equipment often signed by the user and authorized under provisions of TO 33K-1-100.
c. A label completed and signed by PME personnel specifying that all standards have been met.
d. A label completed by the user when calibration is completed.

MODIFICATIONS

Pages 17- 19 of this publication has (have) been deleted in adapting this material for inclusion in the "Trial Implementation of a Model System to Provide Military Curriculum Materials for Use in Vocational and Technical Education." Deleted material involves extensive use of military forms, procedures, systems, etc. and was not considered appropriate for use in vocational and technical education.

ANSWERS FOR CHAPTER REVIEW EXERCISES

CHAPTER 2

1. Servicing, inspecting, repairing, replacing, and validating.
2. System deterioration.
3. Series –6WC.
4. Cabinet temperature will rise and the risk of equipment malfunction will increase.
5. Residue deposits and magnetizing of the heads.
6. To prevent loss of power to the equipment or injury to the personnel.
7. (1) Display and (2) voltage regulator.
8. Usually in an input power line.
9. 170°.
10. The fuse for the circuit will blow.
11. (1) Heat and (2) mechanical abuse.

12. The lamp socket.

13. Digital input and command input devices.

14. (1) Toggle.
    (2) Pushbutton microswitch.
    (3) Pushbutton with indicator.
    (4) Microswitch.

15. (1) NC = normally closed.
    (2) NO = normally open.
    (3) C = common.

16. i, o, q.

17. Broken clip, lack of spring tension on the clip, or a broken plastic recess catch.

18. Printed circuit board is labeled A3, A4, and the receptacle XA3, XA4, etc.

19. Identification of parts.

20. Surfaces which are not clean or insufficient heat.

21. That point at which an alloy is completely liquid.

22. The melting point.

23. Coating metal with a very thin layer of molten filler metal.

24. To protect components.

25. Allowing excess heat to enter the component.

26. Metallurgical.

27. A soldered connection is continuous in metal continuity, while a bolted or wired connection is only physical. The latter connection becomes loose during small temperature variations.

28. To prevent combining of oxygen with the metals.

29. Noncorrosive.

30. Wicking, sniffing.

31. A white typewriter eraser.

32. The stress relief will allow movement of the wire without placing stress on the solder connection.

33. You are.

34. Galvanic cell, concentrated cell, and electrolyte cell.

35. The amount of moisture taken into the air-conditioning system.

36. Chemical attack over the entire surface of a material.

37. Because corrosive agents are trapped between the layers of metal.

38. It is dull with a whitish powderey residue.

39. Protective coating and cleaning.

40. (1) Acrylics and (2) epoxies.

41. Alkaline cleaners.

42. When heavy corrosion exists.

43. AFR 400–44.

44. Yes.

CHAPTER 3

1. Alphanumeric coding systems.

2. Smallest component.

3. Fault location guide, troubleshooting, and system validation.

4. R.

5. 5, 6, 7; –5; 5A1.

6. Descending order, largest to smallest.

7. Circuit diagrams, –3.

8. Use of the letter "N" to identify areas which are not assemblies.

9. Cabinet 1 because of its prefix N1.

10. 0001.

11. Even.

12. 12H.

13. A - assembly.
    C - capacitor.
    CR - crystal, diode.
    F - fuse.
    L - coil.
    P - plug.
    Q - transistor.
    X - socket.
    J - jack.

14. Unit, 0A group, assemblies, and subassemblies.

15. Main distribution frame, filter panel, junction box.

16. Vertical listing and horizontal listing.

17. Bays or racks usually reach from the floor to the ceiling within a cabinet and contain chassis. They generally provide a major function or purpose, whereas chassis are part of a rack and provide only a portion of the major function.

18. Drawer.

19. It identifies installation layout, cable identification, routing data, termination, jack and plug pin lettering and wire color coding, and component part number.

20. Cabinet 45A1.

21. J611–5, J613–4, J614(DL1)10, J622–13, J/P602–01, J/P403703, J/P503405001, J50332053/50, and J503103–4.

22. J/P602119, J/P980112, J/P4860, J/P4682117, to J4693018 in SM–137.

23. Input on left; output on the right.

24. Main distribution frame.

25. Console connector J6 to MDF location A2–A3–J1–15.

26. J5, pin HH.
    Size 16 wire.
    W64, cable 64.
    A - pin A, J6.
    J6 - connector.

CHAPTER 4

1. 545A Tektronix oscilloscope.

2. (1) Horizontal display controls, (2) vertical position and deflection, (3) indicator controls.

3. Time Base A, Time Base B, and Delay-Time Multiplier.

4. The time base A group provides control of horizontal deflection circuits within the scope, can handle signals from DC to 2 megahertz, allows for the selection of various trigger synchronizations, and provides magnification of the display.

5. The fifth and sixth centimeters.

6. 1. *d.*
   2. *a.*
   3. *c.*
   4. *b.*

7. It causes triggering to occur during the rising or falling portion of the triggering waveform, depending upon the selection of positive or negative slope.

8. Triggering Level control.

9. DC voltage.

10. -150V to 0 VDC.

11. *a.* $f = \frac{1}{T}$

    $f = \frac{1}{2 \times 10^{-6}}$

    $f = 500$ kHz.

    b. $t = \frac{1}{f}$

    $t = \frac{1}{100 \times 10^{3}}$

    $t = 1 \times 10^{-5}$

    $t = 10\ \mu\text{sec}$ per cycle

    Time Per Centimeter control setting is 2.5 microseconds per centimeter.

12. Two sweep generators are used within the scope to trigger sweep and unblanking voltages. "A" when used with "B" intensifies a portion of "B's" trace. Therefore, "A" sweep time must be faster. "A" sweep intensity-modulates a portion of "B's" trace.

13. Time Base B controls are set as follows:

    - Triggering Source to INT.
    - Triggering Level to 0.
    - Triggering Slope to either negative or positive.
    - "B" Time Per Centimeter control to desired setting.
    - "A" Time Per Centimeter control to setting shorter than "B's."
    - Delay-Time Multiplier to a setting which causes "A" intensity modulation to begin.

14. The "A" unblanking pulse is gated along with the "B" unblanking pulse. This causes an increase in emission through the CRT during the time that both unblanking levels are present.

15. 4.

16. (1) pulse width and (2) time between pulses (pulse repetition time).

17. Both A and B sweep controls (Time Per Centimeter).
Trigger Slope.
Trigger INT.
Delay-Time Multiplier.

18. "B's" unblanking pulse. Only "A" unblanking intensifies the display.

19. The intensified portion of "B" INTENSIFIED BY "A" is expanded to 10 centimeters wide when "A" DELAYED BY "B" is selected.

20. For taking photographs of the single sweep display.

21.
- Either A or B input separately.
- A and B input alternately.
- Chopped display of two input signals.
- Algebraic sum of two vertical input signals.

22. .02 X 3.5 = .07V peak to peak.

23.
- The DC-AC switch must be in the DC position.
- A zero VDC reference line must be established by use of the Vertical position controls.
- The Volts Per Centimeter control must be set high enough to keep deflection on the screen.
- Set the Polarity switch to the proper polarity.

24. The MV in the scope operates at a different rate.

25. Use in calibrating the attenuator probe.

26. Scale (Illum) (illumination), Focus, Astigmatism, and Intensity.

27. No.

28. It may be used as a (1) vacuum-tube voltmeter, (2) differential DC voltmeter, and (3) megohmmeter.

29. The highest range.

30. (1) Range selection switch, (2) Null switch, (3) Voltage dial switches, and (4) Calibration knob switch.

31. Two capacitors charge to full potential inside the meter. Their charges disable the meter if no circuit damage results.

32. As a VTVM and as a differential meter.

33. Range control to 5V, Null control to VTVM, positive source to + post, return to GND post.

34. Plus or minus .01 VDC.

35. (1) Range control to the lowest voltage range which includes the voltage being set.
    (2) Null control to .01 scale.
    (3) Dials to desired output voltages.
    (4) Polarity control which shows any deflection of the null meter needle to the right.

36. One (and) 500,000.

37. The 269 multimeter measures DC and AC voltages, direct current, and resistance.

38. Remove power, connect probes to test points (using high-voltage probe), then restore power.

39. 1. *b.*
    2. *b.*
    3. *a.*
    4. *b.*
    5. *b.*

40. Isolate the capacitor from the circuit. Select the highest Rx range and apply the leads to the ends of the capacitor. The supply voltage will charge the capacitor (if good) to a given polarity. Observe the meter for a deflection of the needle and a return to infinity for detection of a good capacitor.

41. (1) Isolate the diode.
    (2) Obtain an ohms reading with diode forward bias and reverse bias.
    (3) Calculate the difference and determine a front-to-back ratio if 10:1 or greater is present.

42. Emitter to collector.

43. Yes.

44. Special test sets are built to insure that circuit components meet the design specification.

45. A drawer or card is inserted into a specially designed test set which simulates actual operating characteristics of the unit. The operator simply follows a set of written instructions to locate the trouble.

46. MANUAL, AUTOMATIC.

47. Test block diagrams, test signal generator logic diagrams, drawer under test logic diagrams, and test set comparator test logic diagrams.

48. Yes.

49. The limited number of *different* cards.

50. Each has a control panel for programming a variety of signals to check different types of assemblies.

51. Resistance, impedance, static, dynamic.

52. Drawer test set.

53. It provides the necessary resistive load which simulates the maximum operating parameter in load of the supply under test.

STOP– **1. MATCH ANSWER SHEET TO THIS EXERCISE NUMBER.** **2. USE NUMBER 1 PENCIL.**

30554 01 21

VOLUME REVIEW EXERCISE

Carefully read the following:

DO'S:

1. Check the "course," "volume," and "form" numbers from the answer sheet address tab against the "VRE answer sheet identification number" in the righthand column of the shipping list. If numbers do not match, take action to return the answer sheet and the shipping list to ECI immediately with a note of explanation.
2. Note that numerical sequence on answer sheet alternates across from column to column.
3. Use only medium sharp #1 black lead pencil for marking answer sheet.
4. Circle the correct answer in this test booklet. After you are sure of your answers, transfer them to the answer sheet. If you *have* to change an answer on the answer sheet, be sure that the erasure is complete. Use a clean eraser. But try to avoid any erasure on the answer sheet if at all possible.
5. Take action to return entire answer sheet to ECI.
6. Keep Volume Review Exercise booklet for review and reference.
7. If *mandatorily* enrolled student, process questions or comments through your unit trainer or OJT supervisor.
   If *voluntarily* enrolled student, send questions or comments to ECI on ECI Form 17.

DON'TS:

1. Don't use answer sheets other than one furnished specifically for each review exercise.
2. Don't mark on the answer sheet except to fill in marking blocks. Double marks or excessive markings which overflow marking blocks will register as errors.
3. Don't fold, spindle, staple, tape, or mutilate the answer sheet.
4. Don't use ink or any marking other than with a #1 black lead pencil.

NOTE: TEXT PAGE REFERENCES ARE USED ON THE VOLUME REVIEW EXERCISE. In parenthesis after each item number on the VRE is the *Text Page Number* where the answer to that item can be located. When answering the items on the VRE, refer to the *Text Pages* indicated by these *Numbers*. The VRE results will be sent to you on a postcard which will list the *actual VRE items you missed*. Go to the VRE booklet and locate the *Text Page Numbers* for the items missed. Go to the text and carefully review the areas covered by these references. Review the entire VRE again before you take the closed-book Course Examination.

Multiple Choice

Note: The first three items in this exercise are based on instructions that were included with your course materials. The correctness or incorrectness of your answers to these items will be reflected in your total score. There are no Text Page Numbers for these first three items.

1. The form number of this VRE must match

   a. the form number on the answer sheet.
   b. my course number.
   c. the number of the Shipping List.
   d. my course volume number.

2. So that the electronic scanner can properly score my answer sheet, I must mark my answers with a

   a. pen with blue ink.
   b. number 1 black lead pencil.
   c. ball point or liquid-lead pen.
   d. pen with black ink.

3. If I tape, staple or mutilate my answer sheet; or if I do not cleanly erase when I make changes on the sheet; or if I write over the numbers and symbols along the top margin of the sheet,

   a. I will receive a new answer sheet.
   b. my answer sheet will be hand-graded.
   c. I will be required to retake the VRE.
   d. my answer sheet will be unscored or scored incorrectly.

Chapter 2

14. (015) Preventive maintenance routines are found in which of the following technical order series?

a. –2.
b. –4.
c. –6.
d. –8.

15. (016) If the air flow within an electronic unit is impeded extensively, what causes the intermittent failure rate to increase?

a. Dirt in the blower fan.
b. An increase in ambient temperature.
c. Deficient electronic components.
d. Decrease in air flow.

16. (018) In a typical removal and replacement of a component just prior to restoring power, you should

a. label wires to be removed from and replaced on the new component.
b. unsolder the old leads and resolder the leads to the new component.
c. secure the component to its chassis.
d. make a continunity check with a VOM.

17. (020) The current-carrying element in a fuse melts when

a. an increase in line voltage causes an increase in current.
b. an increase in line voltage causes a decrease in line current.
c. an increase in line current causes an increase in fuse element resistance.
d. a decrease in fuse element resistance results because of a decrease in circuit resistance.

18. (019) AC neon lamps usually require how much voltage for ignition?

a. 120 VAC.
b. 60–65 VAC.
c. 10 VAC.
d. 5 VAC.

19. (014) Analysis, as defined in this chapter, means all of the following *except* determining

a. the objective.
b. the steps involved in accomplishment of the task.
c. what principles or characteristics or specific requirements must be considered while the task is being performed.
d. why a task has been assigned and why you must do it.

20. (021) Which of the following is a command input?

a. Repeat cycle.
b. Static level logic 1.
c. Dynamic level 1.
d. Pulse train.

21. (016–017) Other than oxide on the magnetic head surface, what phenomenon distorts and/or inhibits transfer of data onto or from the tape?

a. Improper hysteresis looping.
b. Static deposits on tape.
c. Magnetized head frame.
d. Lubricated tapes.

22. (019) Which type lamp is usually installed in power supply regulation circuitry?

a. Neon with screw-in.
b. Neon with pigtails.
c. Incandescent screw-in.
d. Incandescent plug-in.

23. (020) At approximately what temperature does a fuse wire melt?

a. 210°.
b. 190°.
c. 170°.
d. 150°.

24. (022) Refer to figure 18 of the text. If switch S1 is on,

a. DS1 and DS2 are on.
b. DS3 and DS4 are on.
c. video amplitude control is not in the circuit.
d. the holding coil is not energized.

25. (023) Which type of switch defect would most likely require repair or replacement?

a. Defective springs.
b. No continuity.
c. Loose toggle.
d. Improper placement of switch unit.

26. (024) When working with multiple pin connectors, identification of wires by alphabetic characters is common; all characters of the alphabet are used *except*

a. i.
b. o and p.
c. i and o.
d. i, o, and q.

27. (026) A connector labeled "P" is the

a. stationary connector of a mating pair.
b. movable connector of a mating pair.
c. connector always connected to a jack.
d. connector on a flexible cable matched with a connector designated "X" rather than "J."

28. (026) A printed circuit card might have a location designation

a. A3.
b. JA3.
c. XA3.
d. PA3.

29. (023) Which of the following switches is energized by electromechanical devices?

a. Toggle switch.
b. Circular microswitches.
c. Pushbutton switch with lamp indicators.
d. Microswitch with level contactor.

30. (026) Inspection of solderless connectors should reveal loose fitting pins, cracked or broken connectors, bare wire in contact with metal casings, and

a. recessed pins.
b. bad solder joints.
c. improper lacing.
d. jack or plug designations.

31. (029) The term used for nonwetting of one or both surfaces to be joined by solder is

a. ADHESION.
b. BLIND JOINT.
c. COLD JOINT.
d. INTERGRANULAR PENETRATION.

32. (032) The four main characteristics of soldering irons are

a. tip size, tip shape, voltage rating, and wattage rating.
b. tip angle, tip size, current rating, and voltage rating.
c. handle shape, tip shape, wattage rating, and current rating.
d. handle size, tip size, voltage rating, and wattage rating.

33. (033) Which is true of the technique of soldering?

a. It is the bonding of two metals into one metal alloy.
b. It is a metal solvent action between solder and the metal being joined.
c. It involves fusion of the two metals being joined rather than solution action.
d. It is another form of electroplating.

34. (029) A device used to absorb or transfer high temperature elements away from delicate parts is called a

a. water cooler.
b. heat extractor.
c. heat sink.
d. refrigerant or fan.

35. (034) Concerning solder alloy within a joint, which of the follwing statements is *incorrect*?

a. It is capable of withstanding stresses and strains.
b. It resists rupture due to temperature changes.
c. It contains rosins for more secure bonding of metal surfaces.
d. It allows for accumulation of nonconductive oxide film between conducting surfaces.

36. (035) Of the four types of flux material listed below, which one is specified in MIL Specification MIL–F–14256, Type A, for use with electronic components?

a. Hydrochloric acid.
b. Rosin.
c. Sal amoniac.
d. Zinc chloride.

37. (038–039) If a component lead is to be cut off after installation of a PCB and no bending is to be performed, the

a. solder is applied before cutting the excess lead.
b. excursion onto the solder surface of the lead must be cut as close to the solder as possible.
c. lead must be cut to a height equal to a #20 wire before soldering.
d. lead may be cut flush with the PCB, since solder will flow into the hole around the lead.

38. (036–037) The principal difference in the desoldering techniques called sniffing and wicking is that

a. sniffing uses a system of air suction.
b. sniffing uses a system of osmosis.
c. wicking uses a system of air suction.
d. wicking uses a system of rosin saturated core material.

39. (040) The task of removal of a component includes the subtasks of removing sealer, cleaning the joint with alcohol, wicking solder from the joint, removal of the defective part, and

a. labeling of part.
b. removing power.
c. locating replacement procedures in TOs.
d. cleaning the joint.

40. (035) The purpose of using a flux when soldering is to

a. mix with oxygen from the air to make solder melt faster.
b. mix with solder for better bonding of the joint.
c. prevent oxygen in the joint from combining with the metals.
d. reduce the melting temperature of solder.

41. (039–040) A term used to mean soldering of IC parts where the IC does not protrude through the PCB is

a. bridging.
b. plating.
c. iron soldering.
d. potting.

42. (043) Alkali is

a. the positive electrode.
b. a chemical that gives a base reaction.
c. the formation by electrochemical means of a thin oxide film on a metal surface.
d. a compound which restricts chemical reaction, especially corrosion.

43. (044) The four basic elements needed to have electrochemical corrosion are anodic and cathodic areas, an electrolyte, and

a. a conductor.
b. an encapsulate.
c. ferrous materials.
d. scaling.

44. (047) Corrosion of metals is distinguishable by discoloration. Three of the four situations below correctly associates a metal with the color of its corrosion. Select the one which is *incorrect.*

a. Aluminum–dull white powdery residue.
b. Carbon and alloy steel–dull gray coating.
c. Copper alloys–dark, greenish-white or grayish-white.
d. Tin-plated copper–white-yellow.

130

45. (048) Of the four areas pertaining to electronic equipment listed below, which would probably require the most frequent inspections for fungus growth?

a. Air-conditioning systems.	c. Painted surfaces.
b. Battery areas.	d. Black boxes.

46. (048) Protective coatings used on electronic gear are placed in classes. Three of the four items below are correct classifications, select the *incorrect* one.

a. Lacquers.	c. Binders.
b. Varnishes.	d. Paints.

47. (050) Which military standard is designed to establish minimum standards for control of corrosion?

a. MIL-STD-1250.	c. MIL-STD-15.
b. MIL-STD-1050.	d. MIL-STD-15-1.

48. (050) Which AFR explains the program of controlling corrosion and assigns responsibilities?

a. 66-1.	c. 100-8.
b. 66-8.	d. 400-44.

Chapter 3

49. (051) The number AR102, using the unit numbering methods, means the

a. 102nd resistor in the circuit.
b. 102nd resistor in the assembly.
c. assembly has 102 resistors.
d. assembly 102, resistor 1.

50. (052) Given a unit alphanumeric of 2A1V2, the part would be located where and in what?

a. Unit 2, assembly 2A, transistor 2.
b. Assembly 2A, tube 1V2.
c. Unit 2, assembly A1, tube V2.
d. Assembly 2A, subassembly 1, transistor V2.

51. (053-054) Coordinate numbering, whether using the location numbering method or location coding method, requires assignment of alphanumerics

a. right to left, bottom to top, back to front.
b. left to right, bottom to top, front to back.
c. right to left, top to bottom, back to front.
d. left to right, top to bottom, front to back.

138

52. (055) The class letter *A* may be assigned to

a. an assembly, computer, set, or teleprinter.
b. only an assembly.
c. only a subassembly.
d. an assembly, a set, a teleprinter, or a motor.

53. (054–055) The alphanumeric 12B6A5/Q1 is a number assigned to which element?

a. Unit 12.
b. Subassembly 6, subassembly A5.
c. Unit 12, subassembly B6, subassembly A5.
d. Transistor Q1.

54. (052) Which system of numbering of electronic equipment uses the letter "N" for areas which are not assemblies?

a. Unit numbering.
b. Location numbering.
c. Location coding.
d. Coordinate coding.

55. (056) Information on cable identification, routing, termination, lettering, and coding can best be located in which technical order?

a. Service manual.
b. Circuits and diagrams manual.
c. Illustrated parts breakdown manual.
d. Preventive maintenance manual.

56. (056) The connector alphanumeric A1P2/A2J2 indicates

a. plug A1P3 is a cabinet plug and jack A1J2 is a chassis or drawer jack.
b. plug A1P3 is a cabinet plug and jack J2 is a cabinet plug.
c. jack J2 mates with interconnecting wire A1P2.
d. plug P3 mates with jack J2.

57. (057) The part identified in figure 53 of the text as alphanumeric J/P503405001 is

a. an interconnector from assembly 503 to connector panel 405, pin 001.
b. jack/plug 503 to connector 405001.
c. an interconnector from connector panel J/P503 to SIF connector 405001.
d. an interconnector from assembly 503 to SIF connector 403, panel 703, pin 007.

58. (058–059) In order for a table used with a main distribution frame (MDF) to be complete, it must have a listing of incoming and outgoing connectors, pin numbers, wire color and size, and

a. MDF location.
b. function.
c. cable number.
d. color of MDF wiring.

59. (056; 058–059) The main distribution frame provides what type of function?

a. Stores the memory.
b. Holds up the cabling.
c. Links up cables to cables.
d. Routes inputs to outputs.

60. (061) In assigning numbers to a jack, to a socket, or to plug pins,

a. all numbers and letters may be used.
b. any number and all letters except i, o, and q may be used.
c. only lower-case letters and any numbers may be used.
d. only letters may be used.

Chapter 4

61. (063) The 545A oscilloscope has two time base generators which control the

a. horizontal sweep.
b. vertical sweep.
c. horizontal magnitude.
d. vertical amplitude.

62. (064) If the Stability control on the 545A oscilloscope is set all the way to the left, the MV is

a. sweep gating.
b. inoperative.
c. triggered.
d. free-running.

63. (067) What source is used to intensify part of the sweep in the "B" INTENSIFIED BY "A" mode of operation?

a. B sweep unblanking.
b. B intensity pulse.
c. A sweep unblanking.
d. A sweep trigger.

64. (064) If the Stability control on the 545A oscilloscope is set 5° to 10° left of a point where the MV runs free, the bias level will cause

a. no effect on the operation.
b. the free-run of the MV to stop.
c. the MV to become inoperative.
d. answers b and c both to be correct.

65. (068) The pickoff point used in the "B" INTENSIFIED BY "A" mode of operation is controlled by the

a. Stability control.
b. Triggering Level control.
c. Horizontal Display control.
d. Delay-Time Multiplier control.

66. (063) The 5X magnifier expands which segment or segments of the graticule display?

a. First.
b. Fourth and fifth.
c. Fifth and sixth.
d. Last.

67. (067) In the "B" INTENSIFIED BY "A" mode of operation, the

    a. B sweep functions normally.
    b. sweep generator develops a sawtooth and negative unblanking signal.
    c. developed voltages are coupled to the indicator but not sent to the trigger circuit.
    d. bias on the pickoff circuit is limited so that pickoff can only occur at specified amplitudes.

68. (069) If a display results in no cycle ending at a centimeter dividing line, what control can be used to measure accurately the time of a cycle?

    a. Horizontal Display selection switch.
    b. Vertical Amplitude control.
    c. Variable Time/CM control.
    d. Delay-Time Multiplier control.

69. (070) The primary difference between "A" DELAYED BY "B" and "B" INTENSIFIED BY "A" is that the

    a. B sweep outputs are not used by the indicator.
    b. indicator receives only B sweep unblanking signals.
    c. A sweep sawtooth is not coupled to the indicator.
    d. intensity-modulated portion of the display is limited to 2 centimeters.

70. (072--073) Vertical input units have provisions for control of all *except* which one of the items listed below?

    a. Acceptance of two input signals.
    b. Display of two signals separately.
    c. Trigger input jack.
    d. Varying the amplitude of the display.

71. (076) The differential voltmeter may be used as all of the following *except* as

    a. an AC voltmeter.
    b. a DC voltmeter.
    c. a vacuum-tube voltmeter.
    d. a megohmmeter.

72. (076–077) The model 801B differential voltmeter has an accuracy of

    a. .5V.
    b. .1V.
    c. .01V.
    d. .001V.

73. (076) The differential voltmeter is a high accuracy meter designed to measure

    a. AC voltages.
    b. DC voltages.
    c. current.
    d. RMS voltages.

74. (077) The range switch on the differential voltmeter must be on which range?

    a. Any range.
    b. Highest range.
    c. Highest range above the source voltage.
    d. Lowest range which will give an on-scale reading.

75. (077–079) An adjustable circuit output is known to require a 10-VDC output level. Prior to calibrating the voltage to exactly 10 VDC, in what conditions should the control switches be?

a. Dials set to 10V, Range set to 50, Null set to VTVM.
b. Dials set to ZERO, Range set to 500, Null set to 10.
c. Dials set to 10V, Range set to 50, Null set to 1V.
d. Operate/Calibrate to CALIBRATE, Range to 500, Null to VTVM.

76. (076) Which is an *incorrect* statement concerning oscilloscope indicator controls?

a. The Focus and Astigmatism controls are used to obtain a clear defined horizontal trace.
b. The Intensity control sets the trace brightness by varying cathode emission.
c. The Intensity control may show the rise time of a pulse more clearly by decreasing the cathode emission.
d. The scale illumination intensifies the graticule.

77. (078–079) If, while using the 801B as a differential meter, the needle deflects to the left, the voltage being measured is

a. below the programmed voltage.
b. equal to the programmed voltage.
c. above the programmed voltage.
d. cannot be determined to be above, even, or below the programmed voltage.

78. (081) When the 801B meter is used as a megohmmeter, the minimum resistance that can be measured is

a. 50 megohms.
b. 1 megohm.
c. 50K.
d. 10K.

79. (083) On the model 269 multimeter, which of the four AC ranges listed below requires a computation factor?

a. 8.
b. 40.
c. 160.
d. 800.

80. (082) Seven ranges of DC voltage measuring selections are built into the model 269 multimeter. The lowest range is

a. 0 - 1.2 volts.
b. 0 - 1.4 volts.
c. 0 - 1.6 volts.
d. 0 - 1.8 volts.

81. (081) When used as a megohmmeter, the model 801B meter ohms readings are taken from what element of the meter for group I, II, and III measurements?

a. Range control.
b. Null meter reading.
c. Null control.
d. Dial readouts.

82. (082) The sensitivity of model 269 multimeter is how many ohms per volt when using the AC selection?

a. 2000.
b. 5000.
c. 20,000.
d. 100, 000.

83. (083) If a multimeter connected to a circuit results in the needle being deflected off scale to the left, the probable cause is

a. improper mechanical positioning.
b. incorrect ohms adjustment.
c. incorrect polarity.
d. incorrect range selected.

84. (084–085) Why is a diode check made with an ohmmeter have limited validity?

a. It can determine the front-to-back ratio of all diodes accurately.
b. It does not account for conduction at other voltage values.
c. All diodes have at least a 10:1 back-to-front ratio.
d. Zener diodes as well as rectifiers have the same ratios and conduct the same.

85. (084) When checking capacitors, the meter has to be used in which mode of operation?

a. Ohms.
b. DC.
c. AC.
d. Current.

86. (085) Drawer testers usually are useful in

a. making alignments.
b. troubleshooting.
c. performance checks.
d. understanding technical orders.

87. (088) If, the drawer under test fails at test step 100, for example, the test points will identify all of the following *except*

a. the drawer failure point.
b. the test set failure point.
c. a group of cards suspect.
d. the logic associated with the equipment.

88. (090) An element common to the card testers discussed in Volume 1, Chapter 4, is that each

a. is programmed the same way.
b. uses switches for programming.
c. has a video output.
d. can generate all signals necessary for checking cards.

89. (089) The card test sets described in Volume 1 generate all of the following *except*

a. test signals.
b. test loads.
c. various voltages.
d. various socket arrangements.

90. (093) The purpose for a *static* load function on a power supply checker is to be able to

a. monitor its load during recovery time after subjecting the unit under test to loads.
b. provide a resistive load for the unit under test.
c. establish a capacitive loading of the test set during operation.
d. calibrate the test set prior to its use as a power supply tester.

91. (095) Which technical order establishes procedures for inventory control and scheduling of PME?

a. 00–20–10–6.
b. 33–1–14.
c. 33K–1–100.
d. 00–35D–54.

92. (095) Examples of Category I test equipment include all of the following *except*

a. ammeters.
b. voltmeters.
c. oscilloscopes.
d. multimeters.

MODIFICATIONS

Pages 43-44 of this publication has (have) been deleted in adapting this material for inclusion in the "Trial Implementation of a Model System to Provide Military Curriculum Materials for Use in Vocational and Technical Education." Deleted material involves extensive use of military forms, procedures, systems, etc. and was not considered appropriate for use in vocational and technical education.

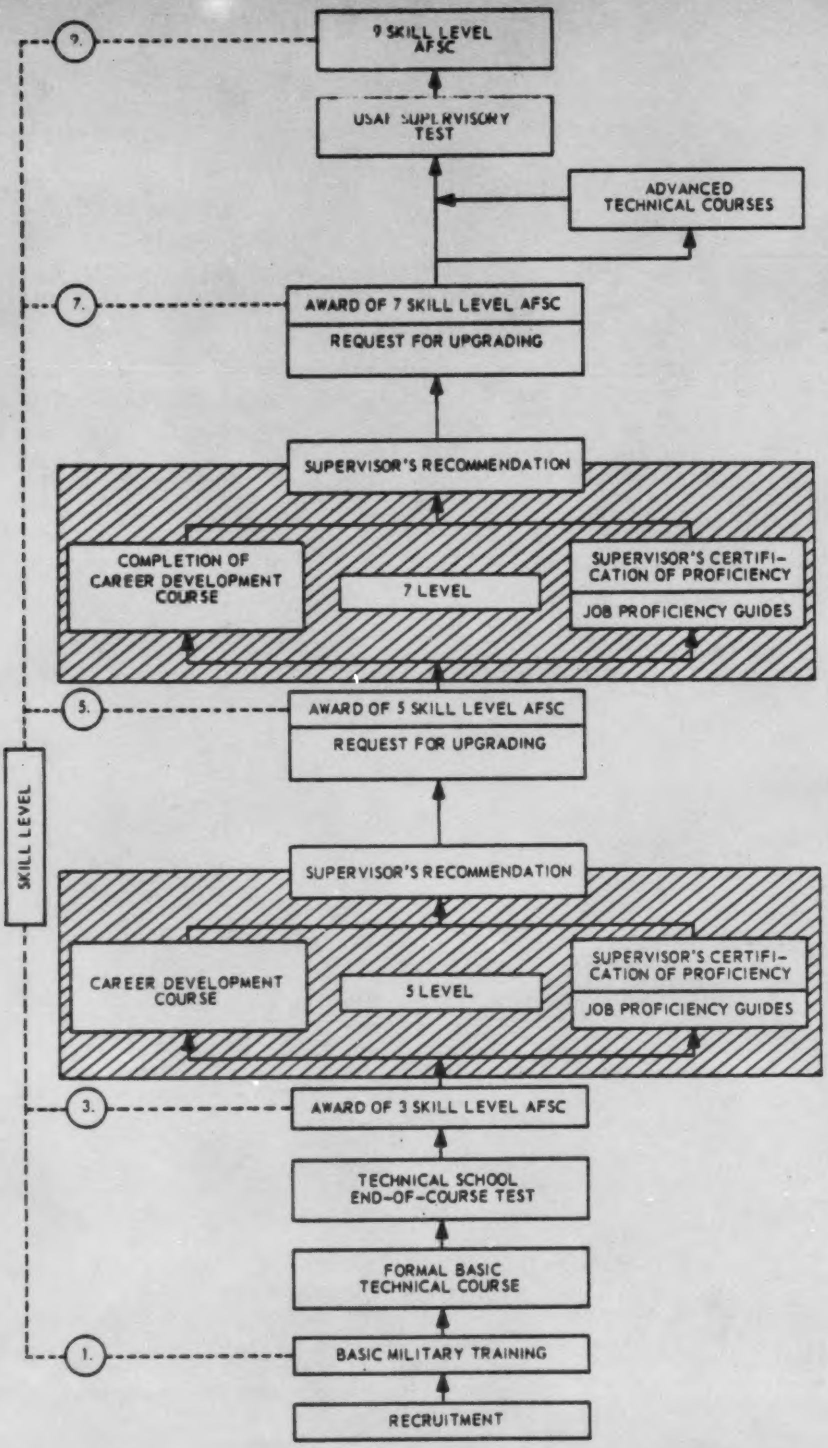
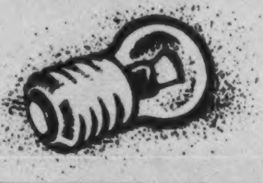
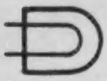
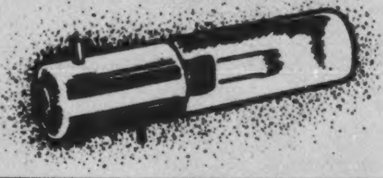
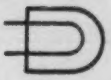
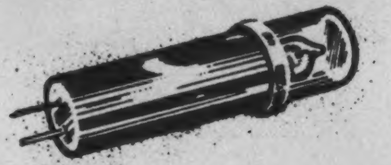
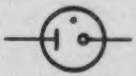
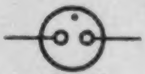
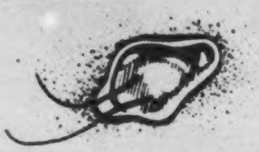
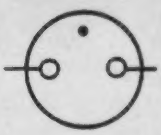
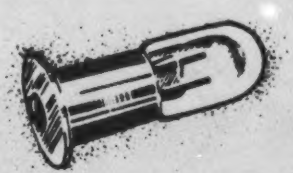
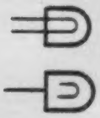

9 SKILL LEVEL AFSC
USAF SUPERVISORY TEST
ADVANCED TECHNICAL COURSES
9.
7.
AWARD OF 7 SKILL LEVEL AFSC
REQUEST FOR UPGRADING
SUPERVISOR'S RECOMMENDATION
COMPLETION OF CAREER DEVELOPMENT COURSE
7 LEVEL
SUPERVISOR'S CERTIFICATION OF PROFICIENCY
JOB PROFICIENCY GUIDES
5.
AWARD OF 5 SKILL LEVEL AFSC
REQUEST FOR UPGRADING
SKILL LEVEL
SUPERVISOR'S RECOMMENDATION
CAREER DEVELOPMENT COURSE
5 LEVEL
SUPERVISOR'S CERTIFICATION OF PROFICIENCY
JOB PROFICIENCY GUIDES
3.
AWARD OF 3 SKILL LEVEL AFSC
TECHNICAL SCHOOL END-OF-COURSE TEST
FORMAL BASIC TECHNICAL COURSE
1.
BASIC MILITARY TRAINING
RECRUITMENT

Figure 1. Skill progression ladder.

TABLE 1
LAMPS

	DESCRIPTION	NUMBERS	SYMBOL	SCHEMATIC REF
1		GE 46 6-8V GE 112 1.2V		DS1
2		GE 47 6-8V GE 57 12-16V GE 313 28V GE 1819 28V GE 1820 28V GE 1929 28V GE 1847 6.3V		DS1
3		NE 2 65V START NE 51 65V START NE 2H 65V START	 DC LAMP  AC LAMP	NE DS1, 2
4		NE 2 65V START NE 2E 65V START NE 68 60V START NE 83 60V START		NE
5		GE 327 28V GE 328 6V GE 330 14V GE 381 6.3V GE 387 28V		DS1, 2

140

TABLE 2
FUSES AND FUSE HOLDERS

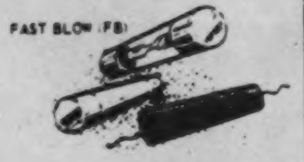
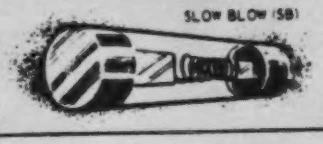
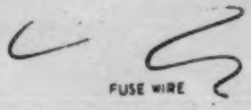
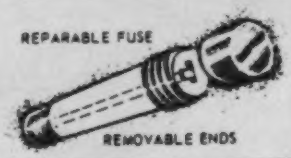
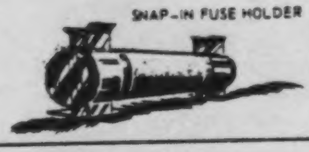
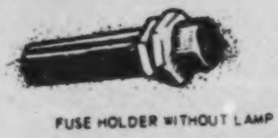
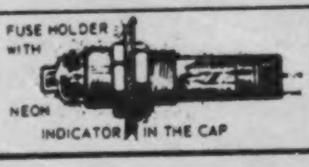
NO.	TYPE PICTORIAL	SIZE VOLT AMP RATING	DESCRIPTION USES APPLICATION
1.		125V/250V .01/10A 1-1/4" L X 1/4" Dia. 1" L X 1/4" Dia. 5/8 X 5/64	Metal ends with a glass or ceramic cylinder between the ends. Blows instantly with input surges or shorts.
2.		125V/250V .01/30A 1-1/4" X 1/4" Dia.	Similar to Fastblow in size, except this fuse is designed to withstand heavy surges for a short time period but will blow instantly on shorts.
3.		125/250V Variable amps depending upon the diameter of the wire.	A strand of malleable wire designed to melt as any other fuse. However, this fuse is usually connected between terminals and not put in a fuse holder. This wire may also be used to repair reparable fuses.
4		125/440V Variable to 100 amps, sizes vary with amperage and voltage requirements.	This fuse has screw-type end connectors which, when removed from the center cylinder, allow for replacement of the fuse wire.
5.		Size and weight is determined by the size of fuse to be held.	Built to accommodate short and long FB and SB fuses as well as reparable fuses.
6		1-11/32" X 5/8" overall. Voltage ranges to 250V @ 15 amps. 1-5/8" X 5/8"	Fuse holder with a twist top. Top is removed by slight inward pressure and twisting the release. Internal contact is backed by a spring to allow for removal and installation of a fuse.
7	 FUSE HOLDER WITH NEON INDICATOR IN THE CAP	Approximately 2-3/8" L X 5/8" Dia. Voltage ranges 2.5V to 250V @ 20 amps.	Fuse holder with a neon indicator in the cap. This neon lights when the fuse blows (refer to text for description.)

TABLE 3
SWITCHES

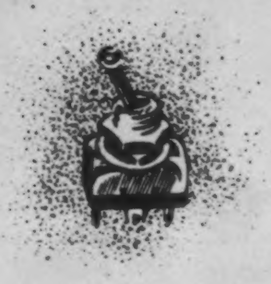
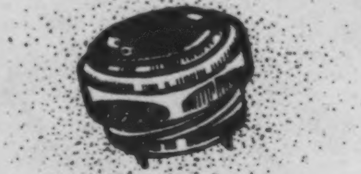
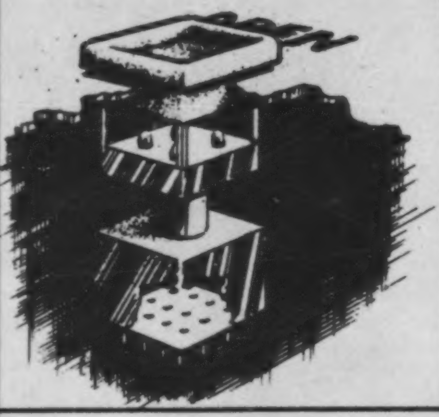
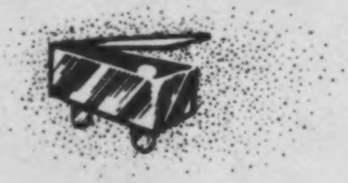
NO.	TYPE AND ILLUSTRATION	DESCRIPTION/USE
1.	Toggle 	a. Two position OFF, ON, Normally Open (NO), Normally Closed (NC). b. Two position NO, NC c. SPST, Single Pole Single Throw. d. DPDT, Double Pole Double Throw. (not shown) multiple connectors in series. e. Spring loaded in one direction. f. Primary uses. (1) Control of voltage and current--ON-OFF. (2) Reset, Preset, Command Control of digital circuits.
2.	Microswitch, circular 	a. Two position ON-OFF, spring loaded contactor. b. Command uses, Reset, Preset control of digit circuits.
3.	Pushbutton Switch w/Lamp Indicators 	a. Pushbutton switch with: (1) Lamp indicator for either OFF, or ON or both. (2) Contact connectors NO, NC, C. (3) Holding coil for locking in either NO or NC. b. Holding coil may not be used as lock, requiring independent release. c. Lamps may be OFF or ON or may contain dual lamp circuit where one or more lamps will always be on. d. Primary uses: (1) Digital input device, entering codes, bits, presetting wired configurations, advancing. (2) Command uses, transfer, clear, erase, reset.
4.	Microswitch, rectangular cased with Level Contactor 	a. A rectangular encased switch with 2 external connectors. b. Connector ball is usually depressed by a spring tension arm assembly. c. Uses--controlling operations of electromechanical devices.

TABLE 4
STANDARDS FOR SOLDERING

STANDARD	TITLE
MIL-S-45743A (M1)	Soldering High Reliability Electrical Connections
O-E-760b	Alcohol Spec
MIL-F-14256C	Flux Spec
QPL-14256C	Flux Supply List
QPL-QQ-S-571d	Solder Spec
QQ-S-571d	Solder Supply List
MIL-STD-252A	Wired Equipment Classification of Mechanical and Visual Defects
MIL-STD-275B	Printed Wiring for Electrical Equipment
MIL-STD-454A	Standard General Requirements for Electrical Equipment
QQ-R-571b	Rods, Welding, Copper and Nickel Alloys Spec
MIL-S-006872A	Soldering Process, General Specifications for

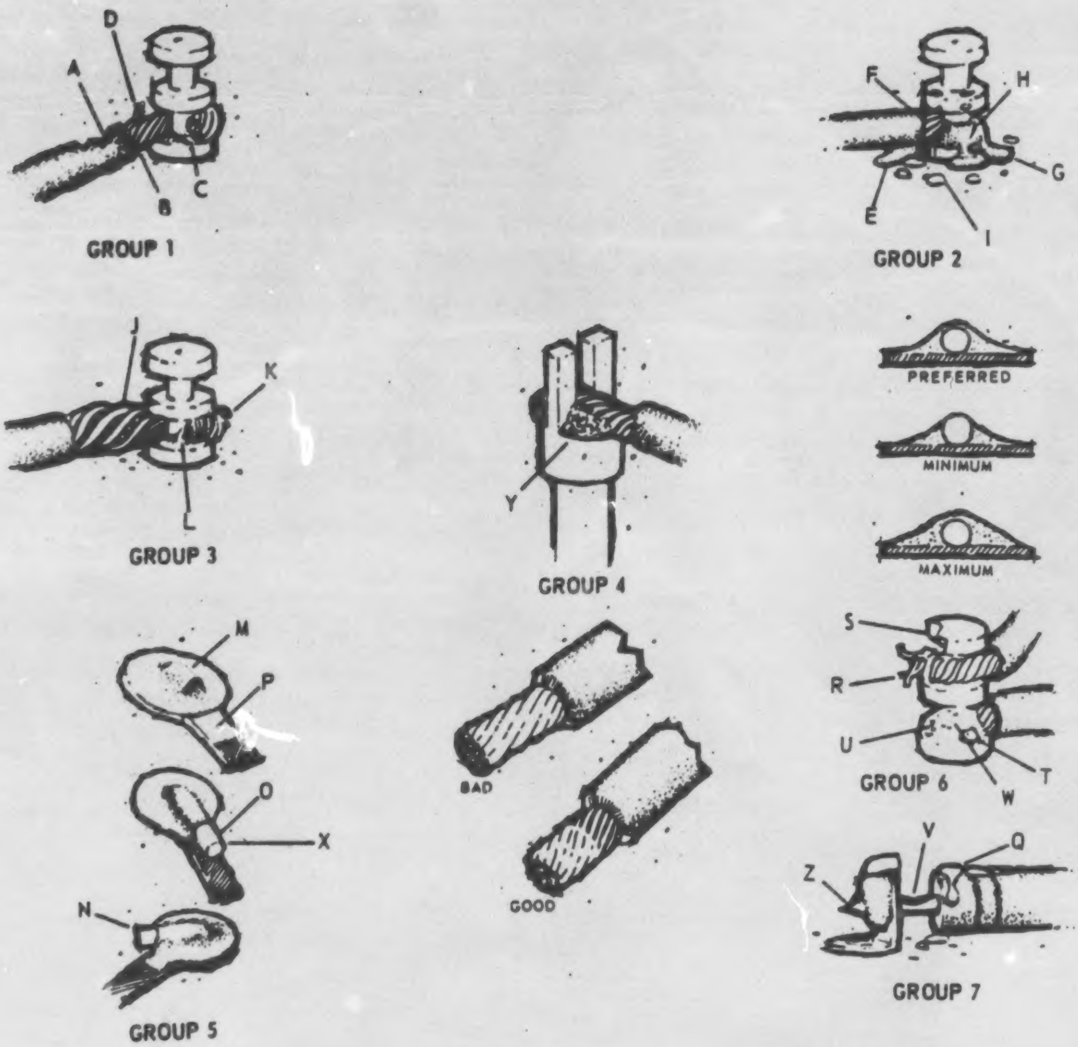

D
A
B
C
GROUP 1
F
H
G
E
I
GROUP 2
J
K
L
GROUP 3
Y
GROUP 4
PREFERRED
MINIMUM
MAXIMUM
M
P
O
X
N
GROUP 5
BAD
GOOD
S
R
U
T
W
GROUP 6
V
Q
Z
GROUP 7

Figure 32. Good and bad solder joints.

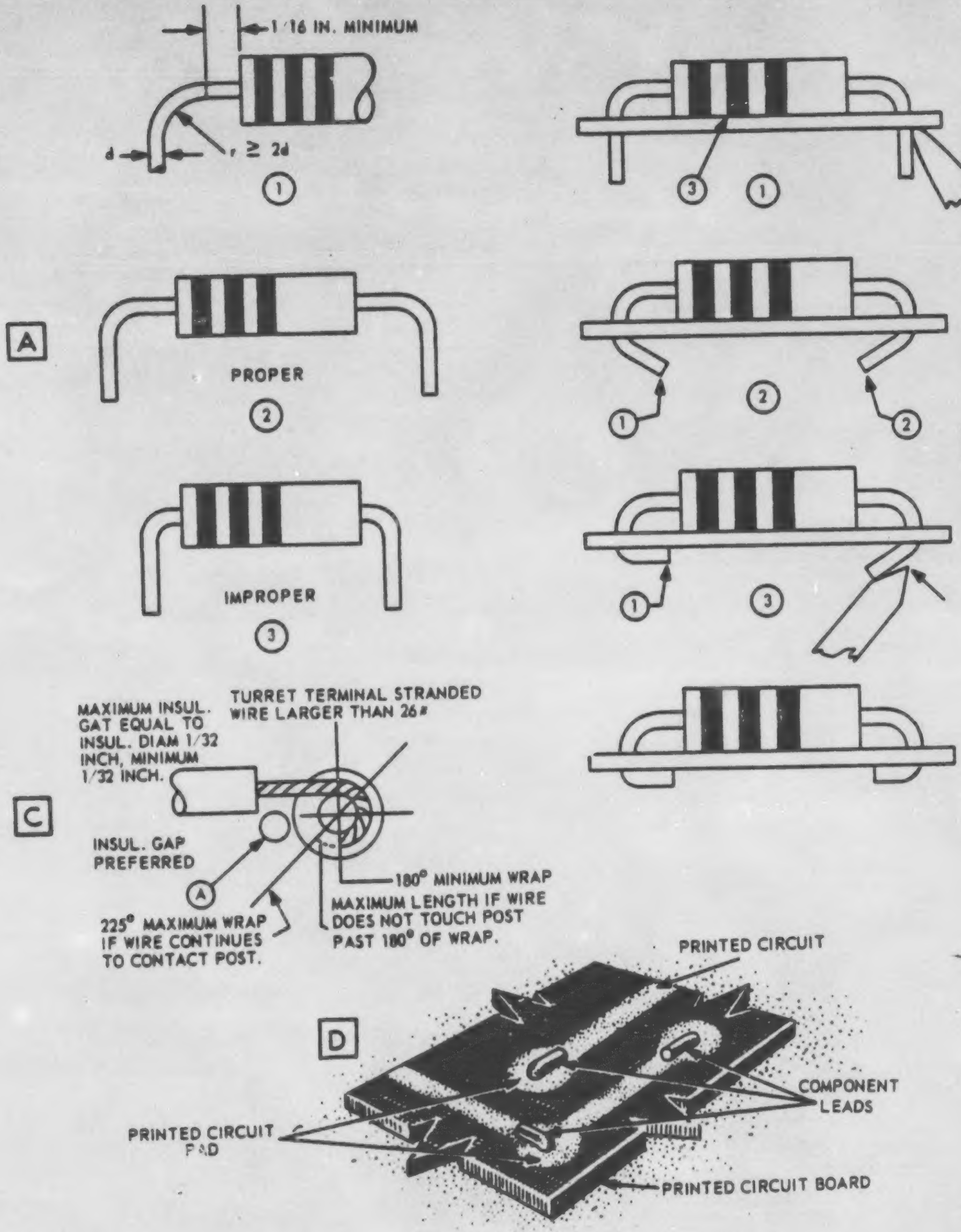

1/16 IN. MINIMUM
d
r ≥ 2d
①
③
①
A
PROPER
②
①
②
②
B
IMPROPER
③
①
③
MAXIMUM INSUL. GAT EQUAL TO INSUL. DIAM 1/32 INCH, MINIMUM 1/32 INCH.
TURRET TERMINAL STRANDED WIRE LARGER THAN 26#
C
INSUL. GAP PREFERRED
Ⓐ
180° MINIMUM WRAP
225° MAXIMUM WRAP IF WIRE CONTINUES TO CONTACT POST.
MAXIMUM LENGTH IF WIRE DOES NOT TOUCH POST PAST 180° OF WRAP.
PRINTED CIRCUIT
D
COMPONENT LEADS
PRINTED CIRCUIT PAD
PRINTED CIRCUIT BOARD

Figure 36. Forming component leads.

TABLE 5
GALVANIC COUPLES

GALVANIC COUPLES			
GROUP	METALLURGICAL CATEGORY	EMF (VOLT)	PERMISSIBLE COUPLES*
1	GOLD, SOLID AND PLATED, GOLD - PLATINUM ALLOYS, WROUGHT PLATINUM	+0.15	○
2	RHODIUM, GRAPHITE	+0.05	● ○
3	SILVER, SOLID OR PLATED, HIGH SILVER ALLOYS	0	● ○
4	NICKEL, SOLID OR PLATED, MONEL, HIGH NICKEL - COPPER ALLOYS, TITANIUM	-0.15	● ● ○
5	COPPER, SOLID OR PLATED, LOW BRASSES OR BRONZES, SILVER SOLDER, GERMAN SILVER, HIGH COPPER-NICKEL ALLOYS, NICKEL-CHROME ALLOYS, AUSTENITIC STAINLESS STEELS (301, 302, 304, 309, 316, 321, 347)	-0.20	● ○
6	COMMERCIAL YELLOW BRASSES AND BRONZES	-0.25	● ● ○
7	HIGH BRASSES AND BRONZES, NAVAL BRASS, MUNTZ METAL	-0.30	● ○
8	18% CHROMIUM TYPE CORROSION-RESISTANT STEELS 440-430, 431, 446, 17-7PH, 17-4PH	-0.35	● ● ○
9	CHROMIUM, PLATED, TIN, PLATED, 12% CHROMIUM TYPE CORROSION-RESISTANT STEEL, 410, 416, 420	-0.45	○ ●
10	TIN-PLATE, TERNEPLATE; TIN-LEAD SOLDERS	-0.50	● ○
11	LEAD, SOLID OR PLATED; HIGH LEAD ALLOYS	-0.55	● ● ○
12	ALUMINUM, WROUGHT ALLOYS OF THE DURALUMIN TYPE, 2014, 2024, 2017	-0.60	● ● ○
13	IRON, WROUGHT, GRAY, OR MALLEABLE, PLAIN CARBON AND LOW ALLOY STEELS, ARMCO IRON	-0.70	● ○
14	ALUMINUM, WROUGHT ALLOYS OTHER THAN DURALUMIN, TYPE 6061, 7075, 5052, 5056, 1100, 3003. CAST ALLOYS OF THE SILICON TYPE 355, 356	-0.75	● ○
15	ALUMINUM, CAST ALLOYS OTHER THAN SILICON TYPE, CADMIUM, PLATED AND CHROMATED	-0.80	● ● ○
16	HOT-DIP-ZINC PLATE; GALVANIZED STEEL	-1.05	● ○
17	ZINC WROUGHT, ZINC-BASE DIE CAST ALLOYS, ZINC, PLATED	-1.10	●
18	MAGNESIUM AND MAGNESIUM-BASE ALLOYS CAST OR WROUGHT	-1.60	●

*MEMBERS OF GROUPS CONNECTED BY LINES ARE CONSIDERED AS PERMISSIBLE COUPLES. HOWEVER, THIS SHOULD NOT BE CONSTRUED AS BEING DEVOID OF GALVANIC ACTION. PERMISSIBLE COUPLES REPRESENT A LOW GALVANIC EFFECT.

○ INDICATES THE MOST CATHODIC MEMBER OF THE SERIES, ● AN ANODIC MEMBER, AND THE ARROWS INDICATE THE ANODIC DIRECTION.

REFER TO TABLE II, MIL-STD-186, FOR GROUP AMPLIFICATION OF GALVANIC COUPLES.

NOTE: EXTRACTED FROM MIL-STD-1250(MI) 31 MAR 67

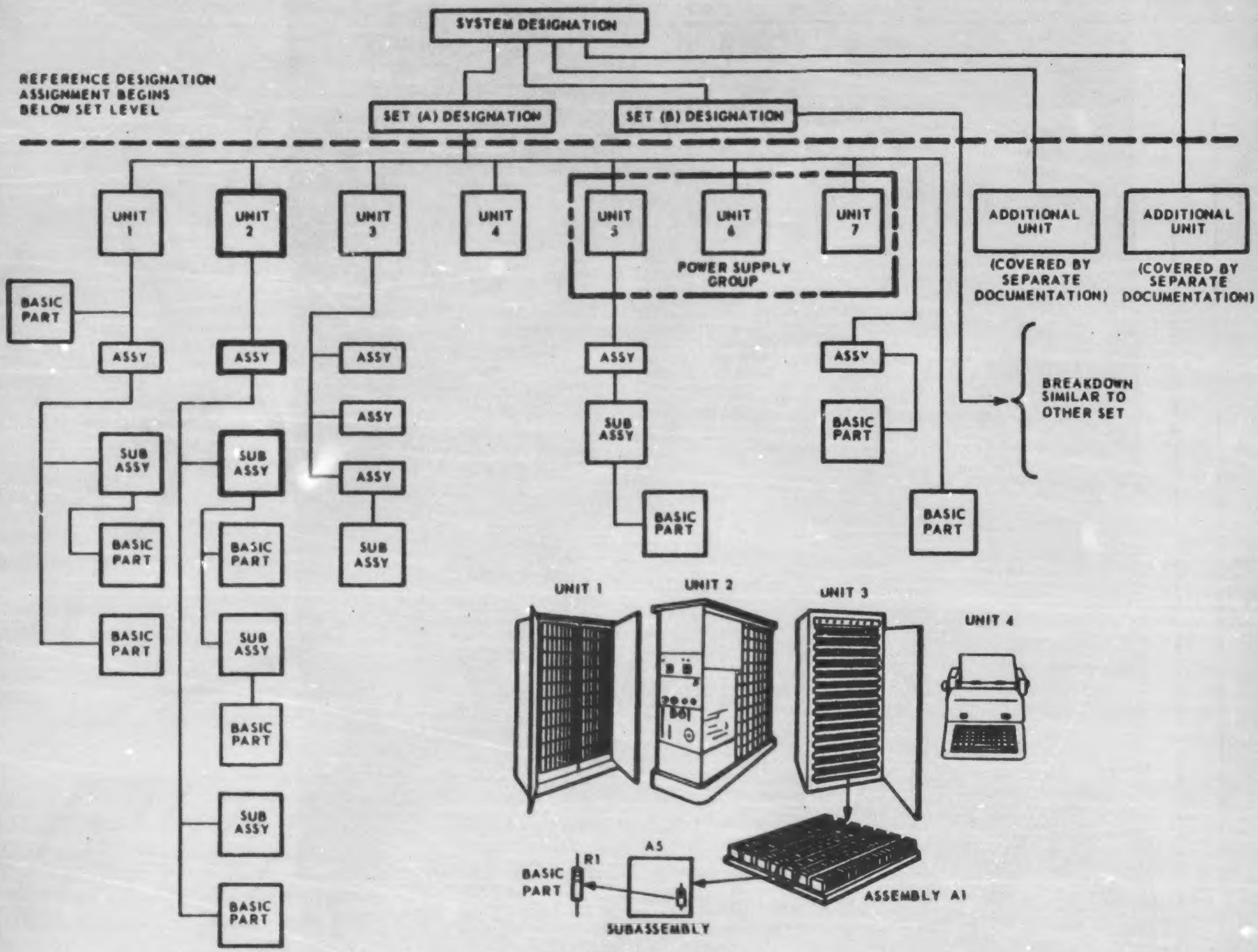

SYSTEM DESIGNATION
REFERENCE DESIGNATION ASSIGNMENT BEGINS BELOW SET LEVEL
SET (A) DESIGNATION
SET (B) DESIGNATION
UNIT 1
UNIT 2
UNIT 3
UNIT 4
UNIT 5
UNIT 6
UNIT 7
POWER SUPPLY GROUP
ADDITIONAL UNIT
(COVERED BY SEPARATE DOCUMENTATION)
ADDITIONAL UNIT
(COVERED BY SEPARATE DOCUMENTATION)
BASIC PART
ASSY
SUB ASSY
BREAKDOWN SIMILAR TO OTHER SET
UNIT 1
UNIT 2
UNIT 3
UNIT 4
A5
R1
BASIC PART
SUBASSEMBLY
ASSEMBLY A1

Figure 46. System Subdivision.

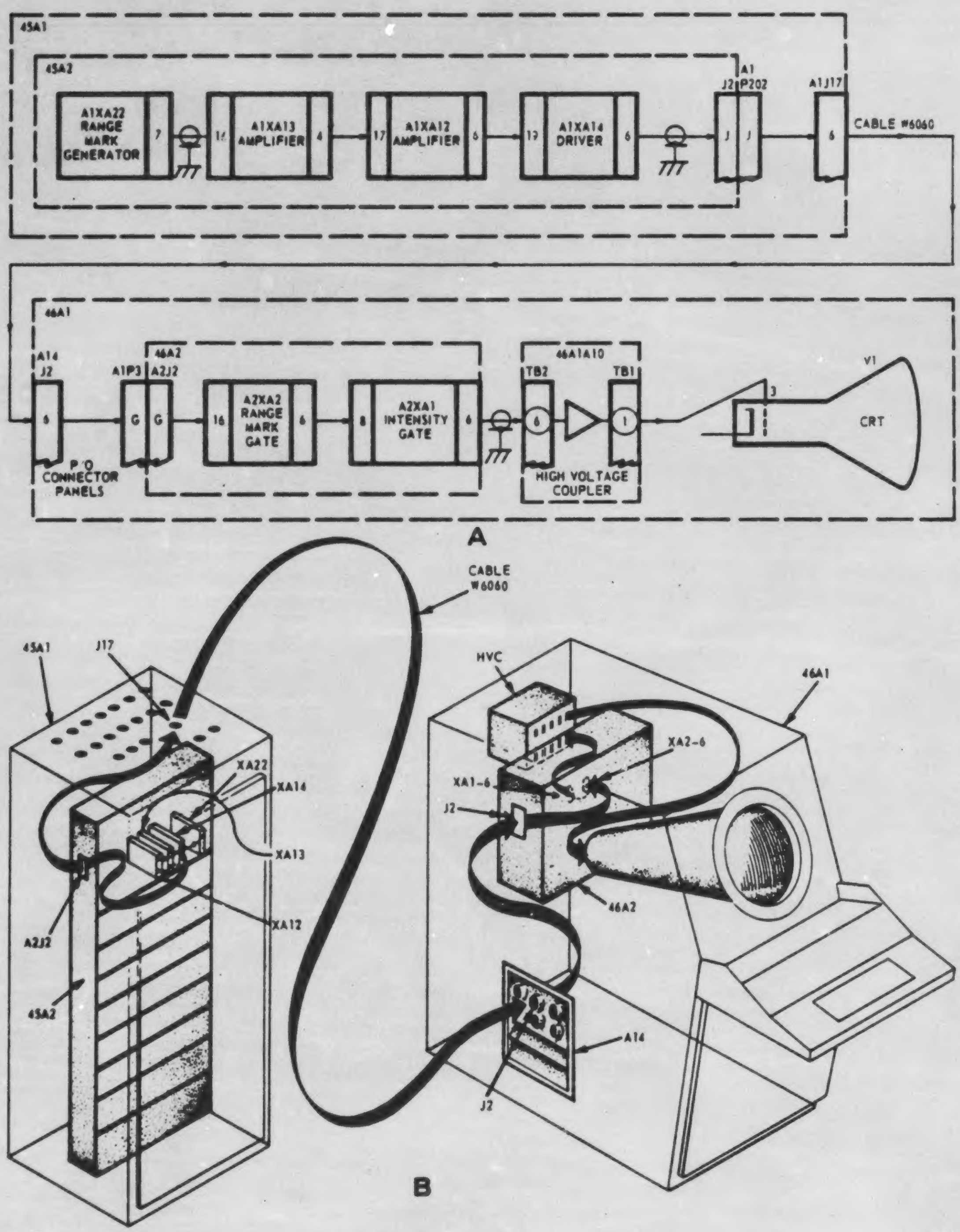

45A1
45A2
A1XA22 RANGE MARK GENERATOR
7
14
A1XA13 AMPLIFIER
4
17
A1XA12 AMPLIFIER
6
17
A1XA14 DRIVER
6
A1
J2
P202
J
J
A1J17
6
CABLE #6060
46A1
A14 J2
6
A1P3
A2J2
G
G
46A2
16
A2XA2 RANGE MARK GATE
6
8
A2XA1 INTENSITY GATE
6
46A1A10
TB2
6
TB1
1
HIGH VOLTAGE COUPLER
P/O CONNECTOR PANELS
V1
3
CRT
A
CABLE W6060
45A1
J17
XA22
XA14
XA13
XA12
A2J2
45A2
HVC
46A1
XA2-6
XA1-6
J2
46A2
A14
J2
B

Figure 52. Range mark routing.

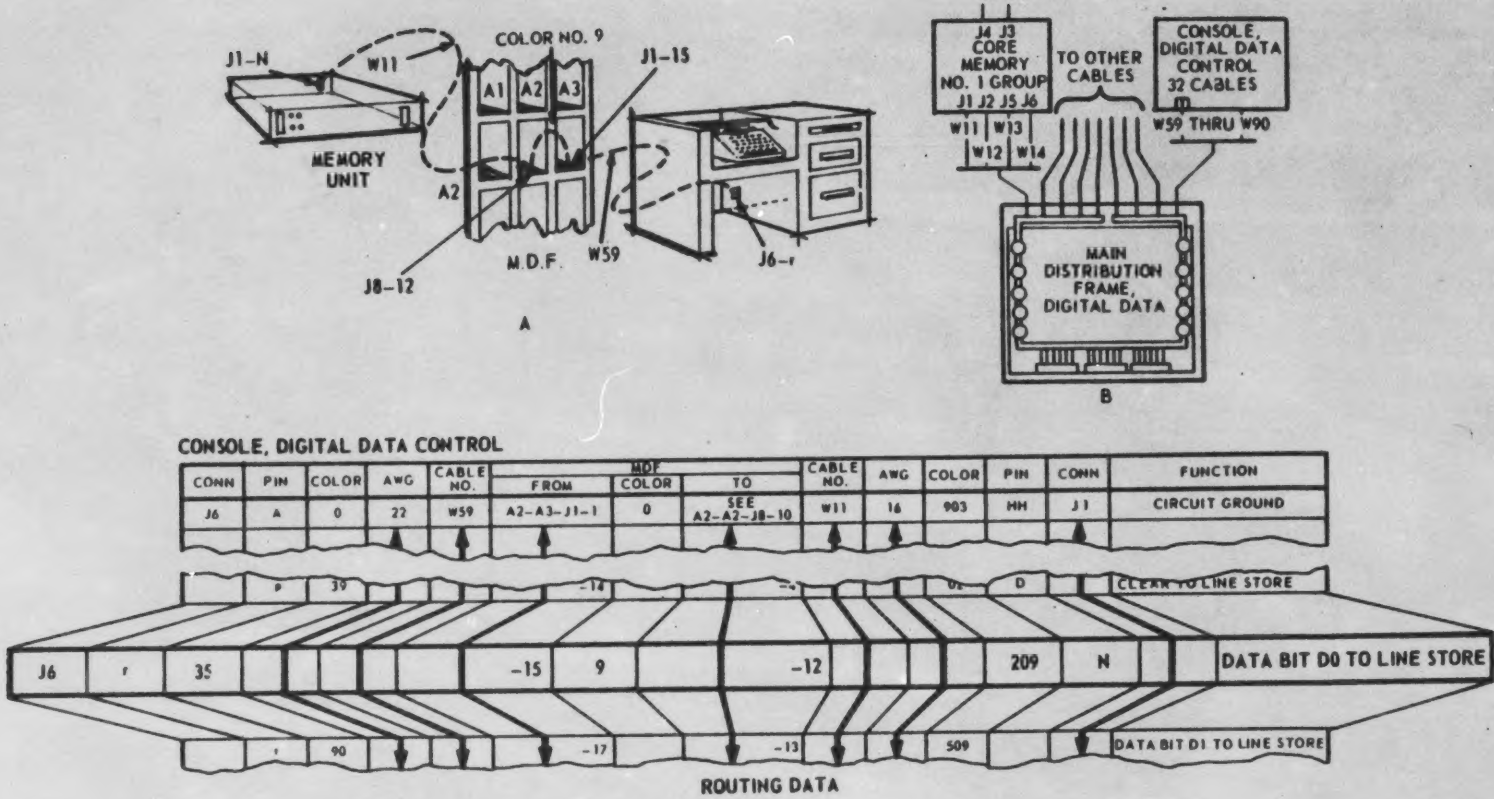

J1–N
W11
COLOR NO. 9
A1
A2
A3
J1–15
MEMORY UNIT
A2
J8–12
M.D.F.
W59
J6–r
A
J4 J3
CORE MEMORY NO. 1 GROUP
J1 J2 J5 J6
W11
W13
W12
W14
TO OTHER CABLES
CONSOLE, DIGITAL DATA CONTROL 32 CABLES
W59 THRU W90
MAIN DISTRIBUTION FRAME, DIGITAL DATA
B
CONSOLE, DIGITAL DATA CONTROL
CONN
PIN
COLOR
AWG
CABLE NO.
MDF
FROM
COLOR
TO
CABLE NO.
AWG
COLOR
PIN
CONN
FUNCTION
J6
A
0
22
W59
A2–A3–J1–1
0
SEE A2–A2–J8–10
W11
16
903
HH
J1
CIRCUIT GROUND
p
39
–14
D
CLEAR TO LINE STORE
J6
r
35
–15
9
–12
209
N
DATA BIT D0 TO LINE STORE
r
90
–17
–13
509
DATA BIT D1 TO LINE STORE
ROUTING DATA

Figure 57. Signal routing through MDF.

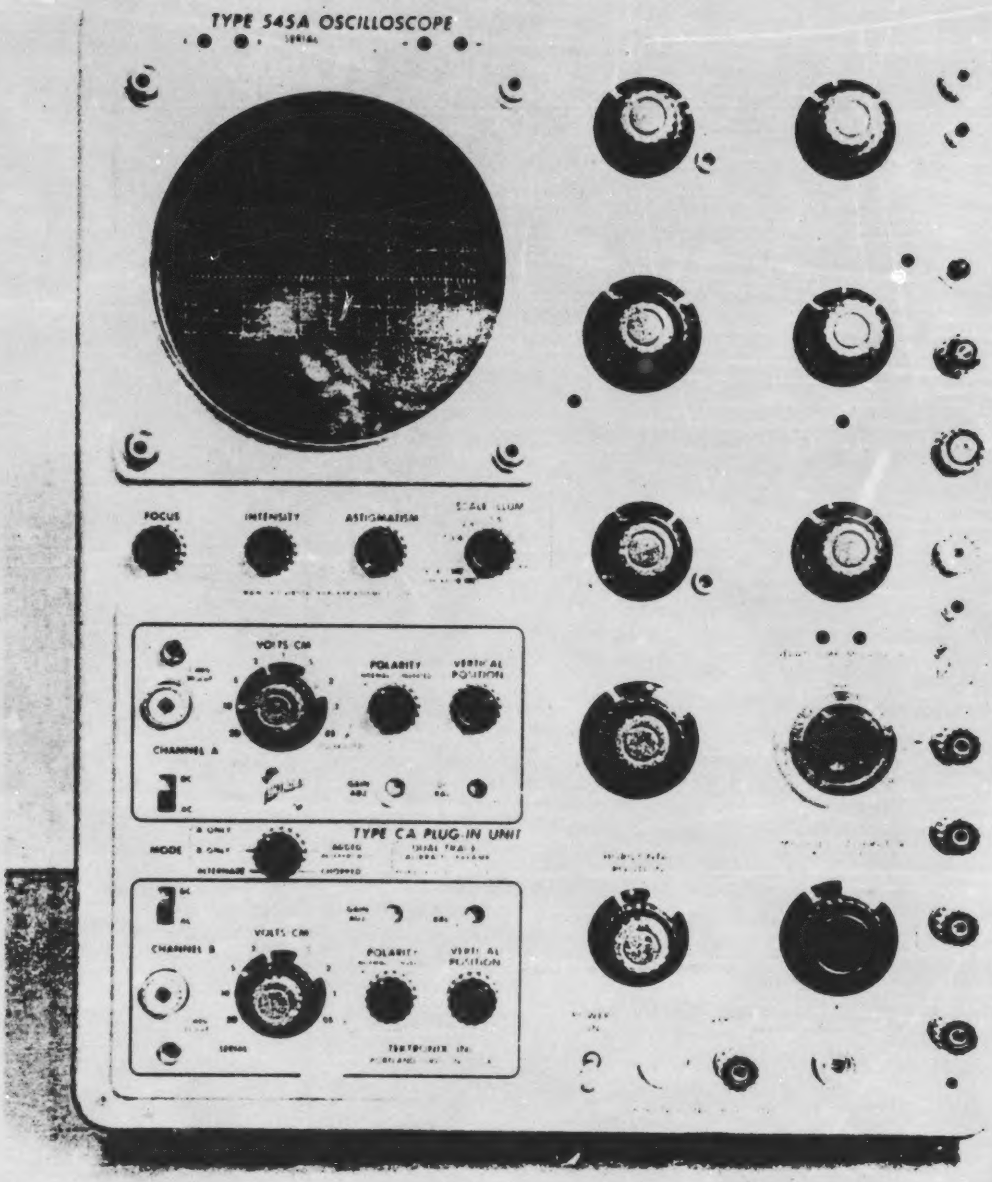

TYPE 545A OSCILLOSCOPE
SERIAL
FOCUS
INTENSITY
ASTIGMATISM
SCALE ILLUM
VOLTS CM
POLARITY
VERTICAL POSITION
CHANNEL A
DC
AC
GAIN ADJ
TYPE CA PLUG-IN UNIT
MODE
A ONLY
B ONLY
ALTERNATE
CHOPPED
DUAL TRACE
CHANNEL B
VOLTS CM
POLARITY
VERTICAL POSITION
TEKTRONIX INC
POWER

Figure 60. 545 oscilloscope.

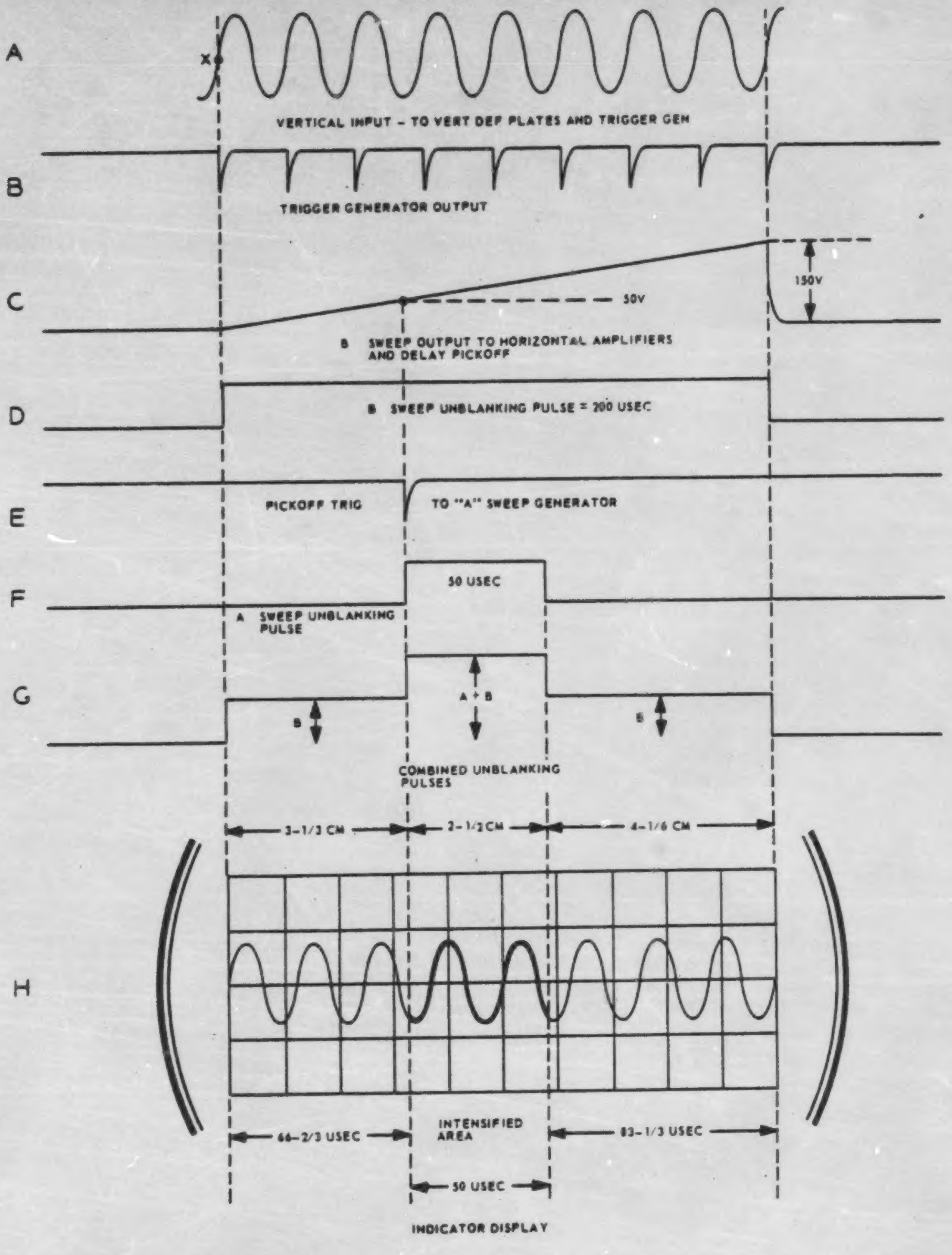

A
X
VERTICAL INPUT – TO VERT DEF PLATES AND TRIGGER GEN
B
TRIGGER GENERATOR OUTPUT
C
150V
50V
B SWEEP OUTPUT TO HORIZONTAL AMPLIFIERS AND DELAY PICKOFF
D
B SWEEP UNBLANKING PULSE = 200 USEC
E
PICKOFF TRIG
TO "A" SWEEP GENERATOR
F
50 USEC
A SWEEP UNBLANKING PULSE
G
B
A + B
B
COMBINED UNBLANKING PULSES
3-1/3 CM
2-1/2 CM
4-1/6 CM
H
66-2/3 USEC
INTENSIFIED AREA
83-1/3 USEC
50 USEC
INDICATOR DISPLAY

Figure 67. Intensified sweep.

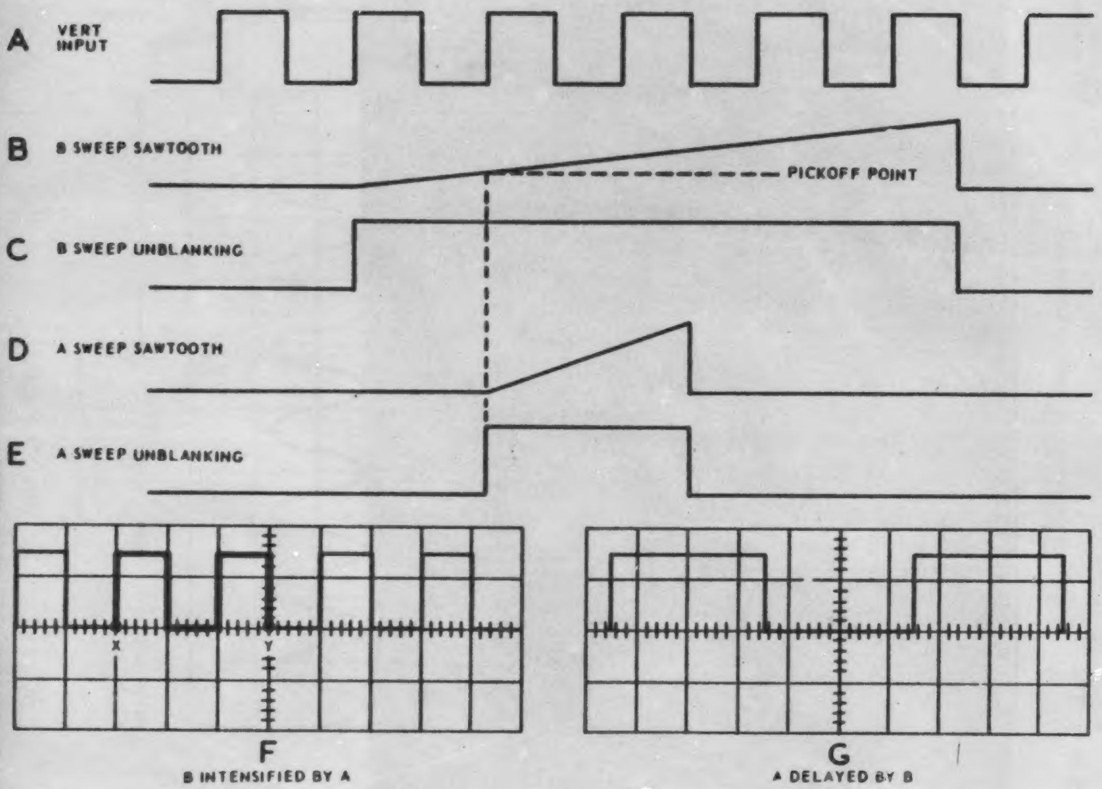

A
VERT INPUT
B
B SWEEP SAWTOOTH
PICKOFF POINT
C
B SWEEP UNBLANKING
D
A SWEEP SAWTOOTH
E
A SWEEP UNBLANKING
X
Y
F
B INTENSIFIED BY A
G
A DELAYED BY B

Figure 73. "A" delayed by "B" - display expansion.

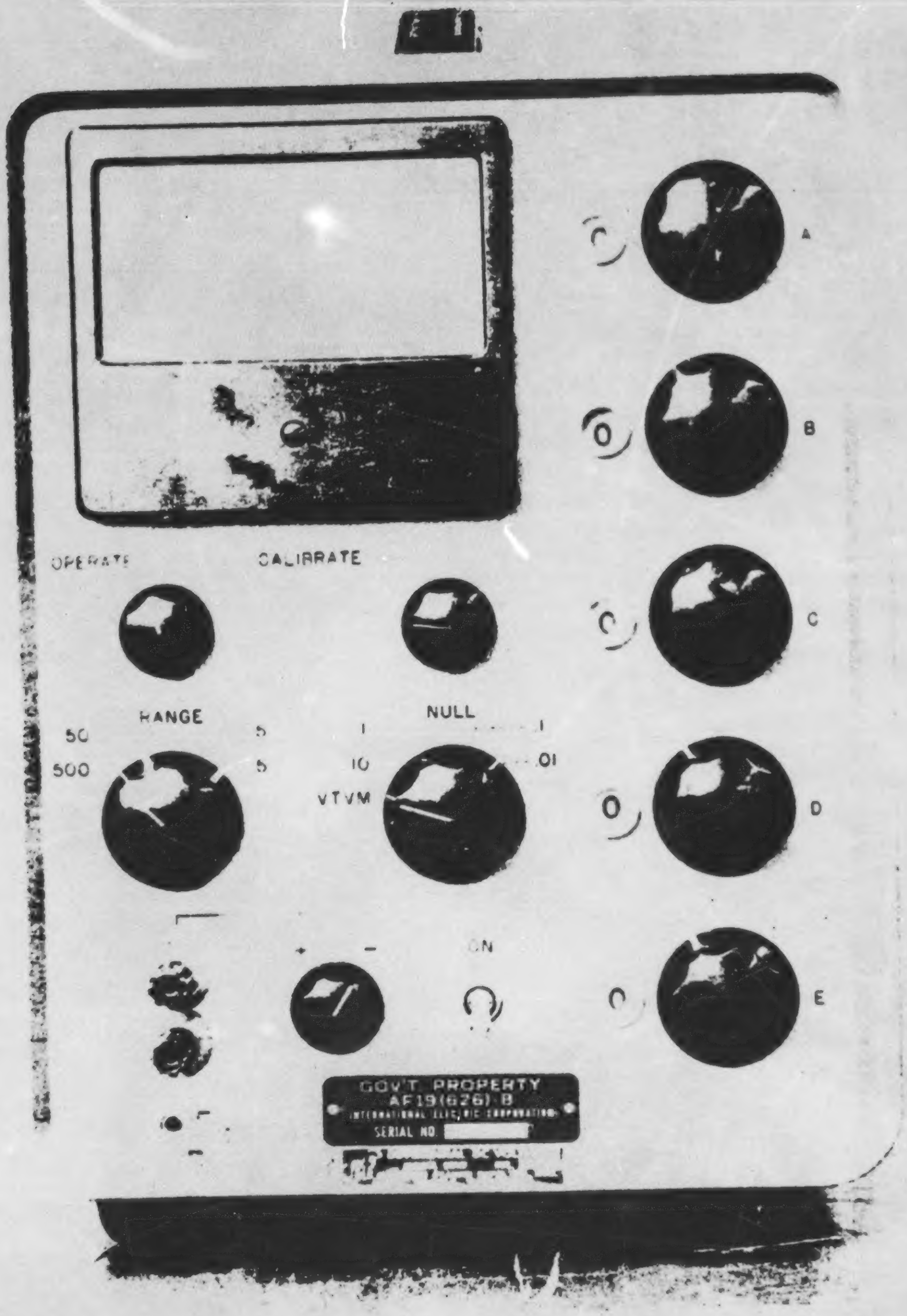

OPERATE
CALIBRATE
A
B
C
D
E
RANGE
50
500
5
5
NULL
1
10
VTVM
.1
.01
+
−
ON
GOV'T PROPERTY
AF19(626)-B
INTERNATIONAL ELECTRIC CORPORATION
SERIAL NO.

Figure 82. Differential voltmeter.

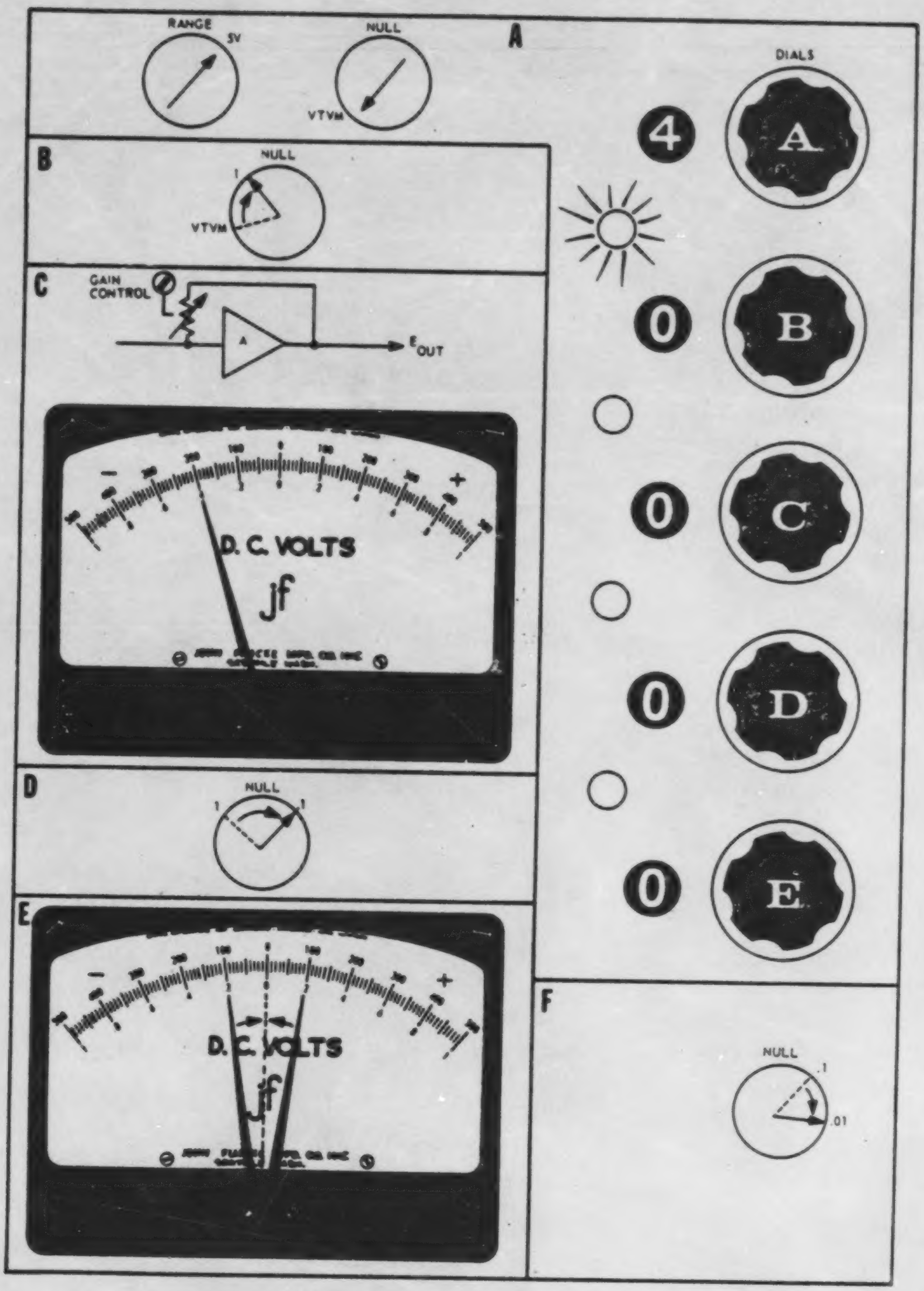

A
RANGE
5V
NULL
VTVM
DIALS
4
A
B
NULL
1
VTVM
C
GAIN CONTROL
A
E_{OUT}
D. C. VOLTS
jf
0
B
0
C
0
D
0
E
D
NULL
1
1
E
D. C. VOLTS
jf
F
NULL
.1
.01

Figure 87. Circuit calibration.

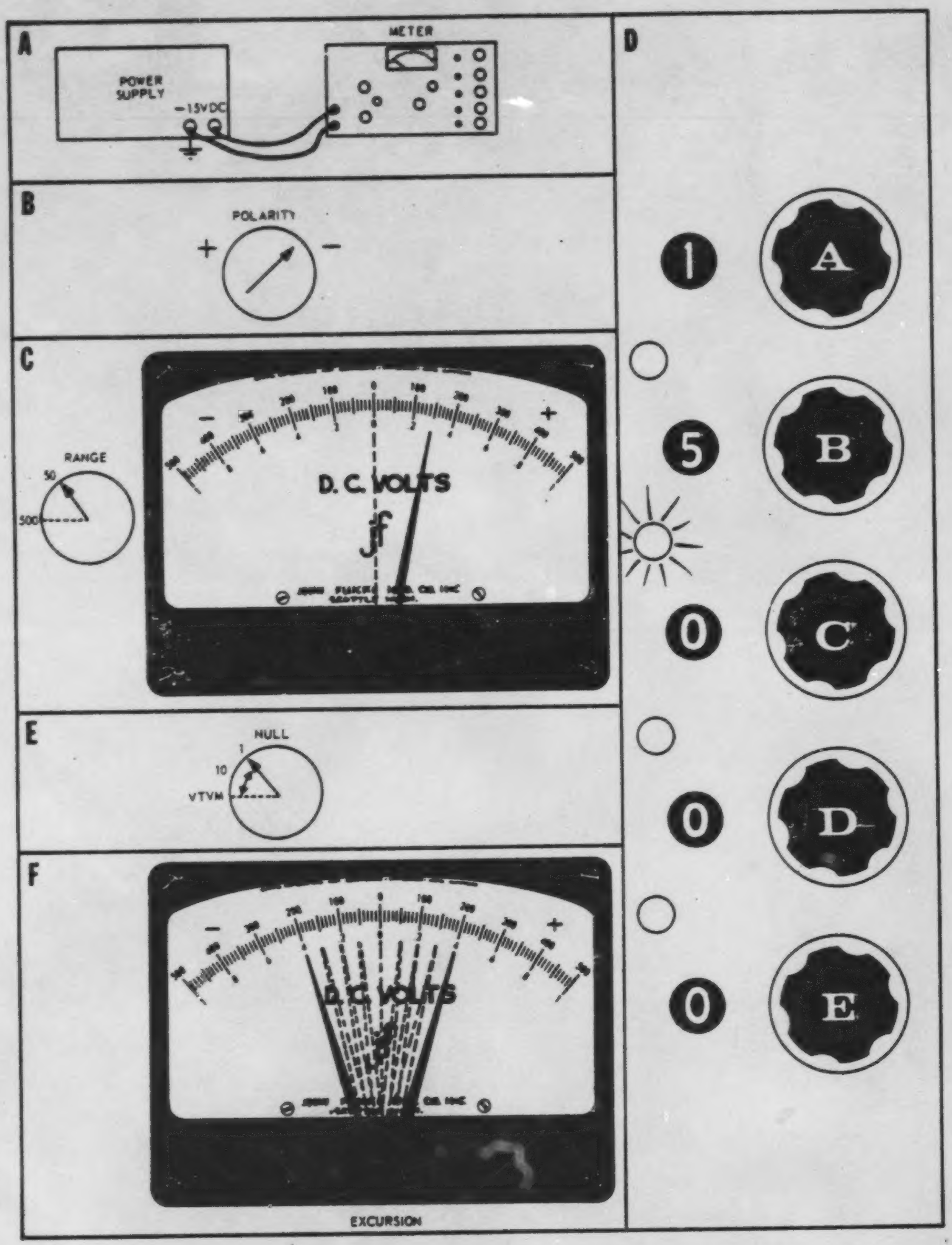

A
METER
POWER SUPPLY
−15VDC
B
POLARITY
+
−
C
RANGE
50
500
D.C. VOLTS
D
1
5
0
0
0
A
B
C
D
E
E
NULL
1
10
VTVM
F
D.C. VOLTS
EXCURSION

Figure 88. Voltage excursions.

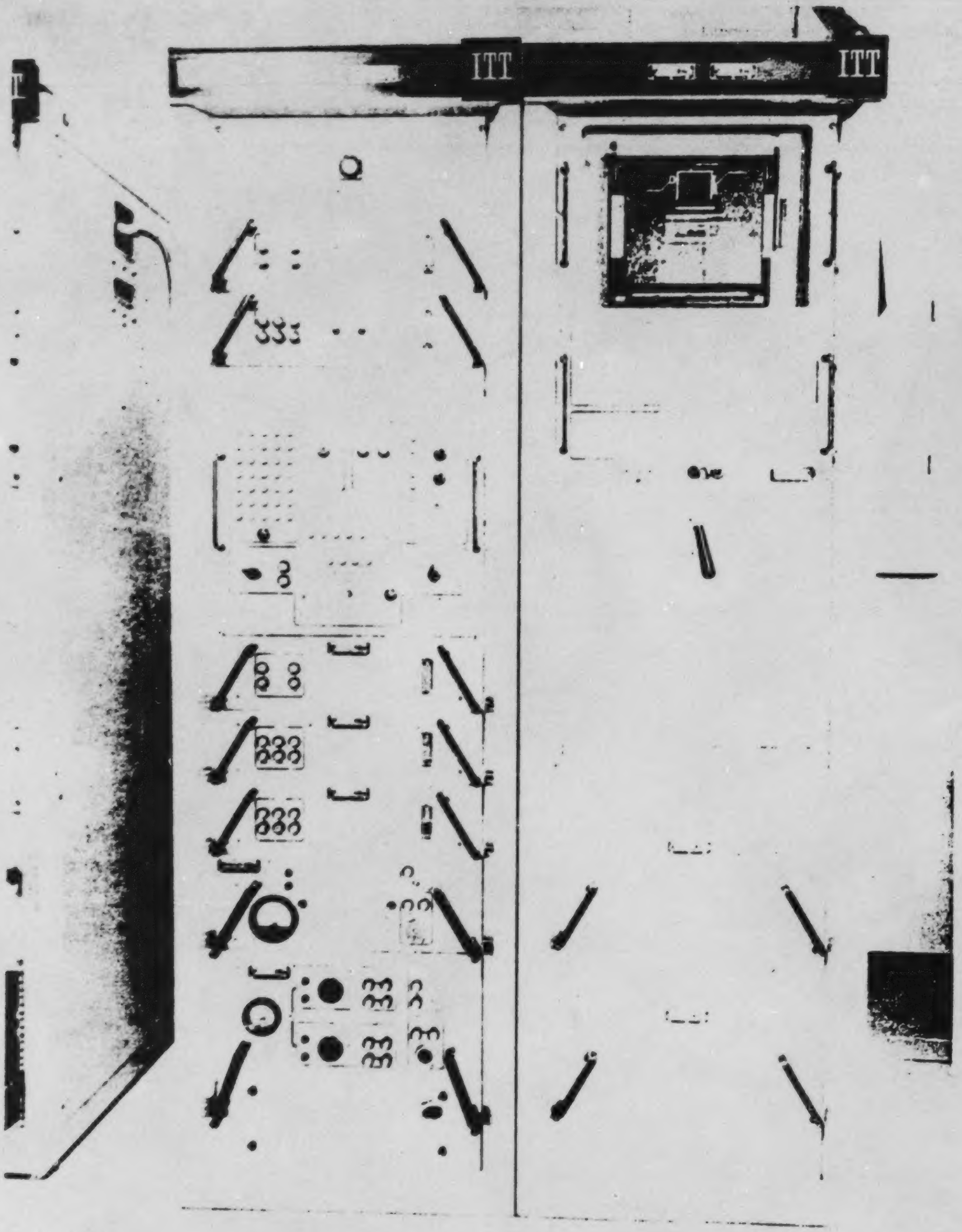


Figure 90. Drawer tester.

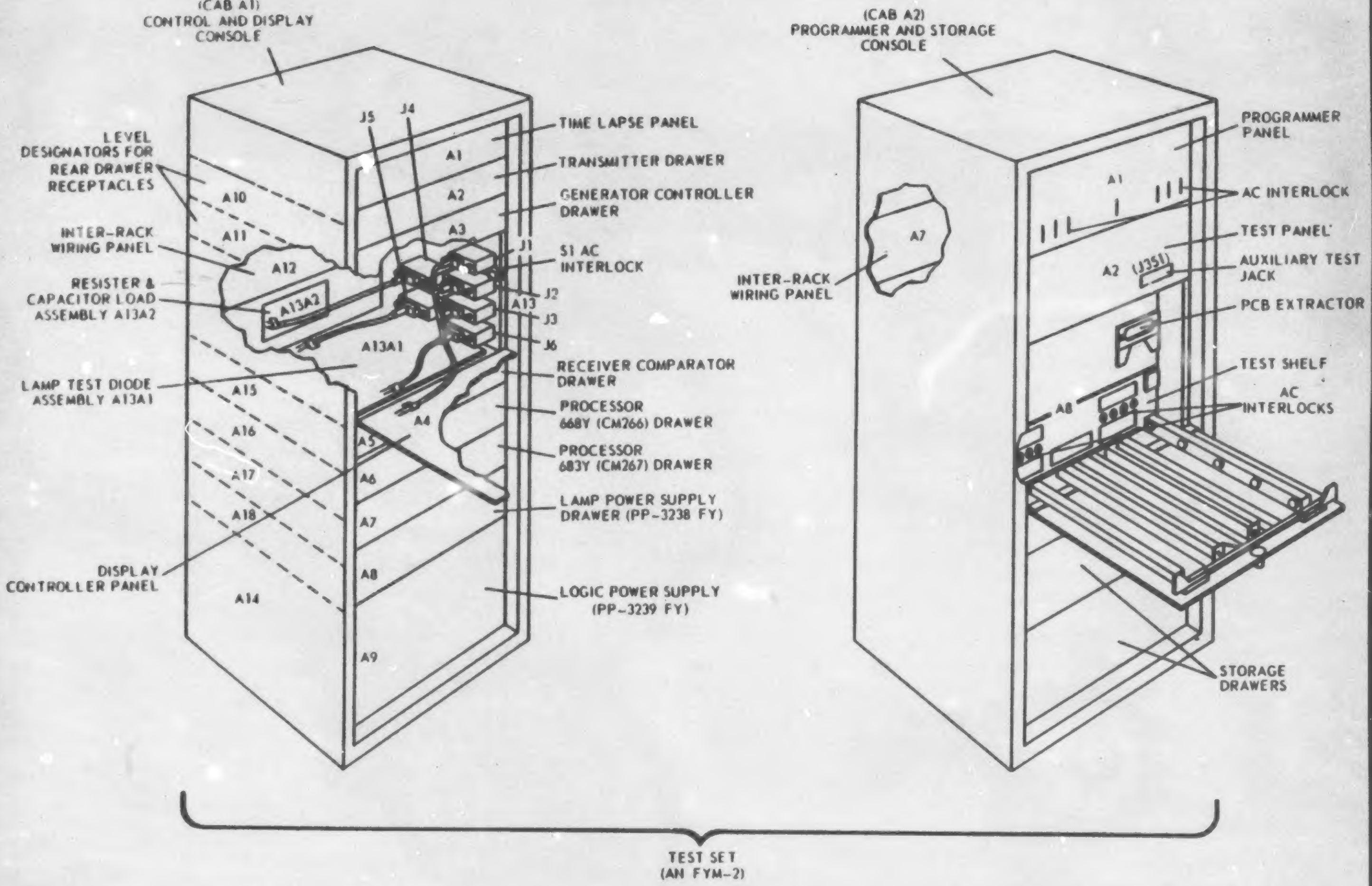

(CAB A1)
CONTROL AND DISPLAY CONSOLE
LEVEL DESIGNATORS FOR REAR DRAWER RECEPTACLES
INTER-RACK WIRING PANEL
RESISTER & CAPACITOR LOAD ASSEMBLY A13A2
LAMP TEST DIODE ASSEMBLY A13A1
DISPLAY CONTROLLER PANEL
A10
A11
A12
A13A2
A13A1
A15
A16
A17
A18
A14
J5
J4
A1
A2
A3
J1
J2
A13
J3
J6
A4
A5
A6
A7
A8
A9
TIME LAPSE PANEL
TRANSMITTER DRAWER
GENERATOR CONTROLLER DRAWER
S1 AC INTERLOCK
RECEIVER COMPARATOR DRAWER
PROCESSOR 668Y (CM266) DRAWER
PROCESSOR 683Y (CM267) DRAWER
LAMP POWER SUPPLY DRAWER (PP-3238 FY)
LOGIC POWER SUPPLY (PP-3239 FY)
(CAB A2)
PROGRAMMER AND STORAGE CONSOLE
A7
INTER-RACK WIRING PANEL
A1
A2
(J351)
A8
PROGRAMMER PANEL
AC INTERLOCK
TEST PANEL
AUXILIARY TEST JACK
PCB EXTRACTOR
TEST SHELF
AC INTERLOCKS
STORAGE DRAWERS
TEST SET
(AN FYM-2)

Figure 91. Test set, reference designations.

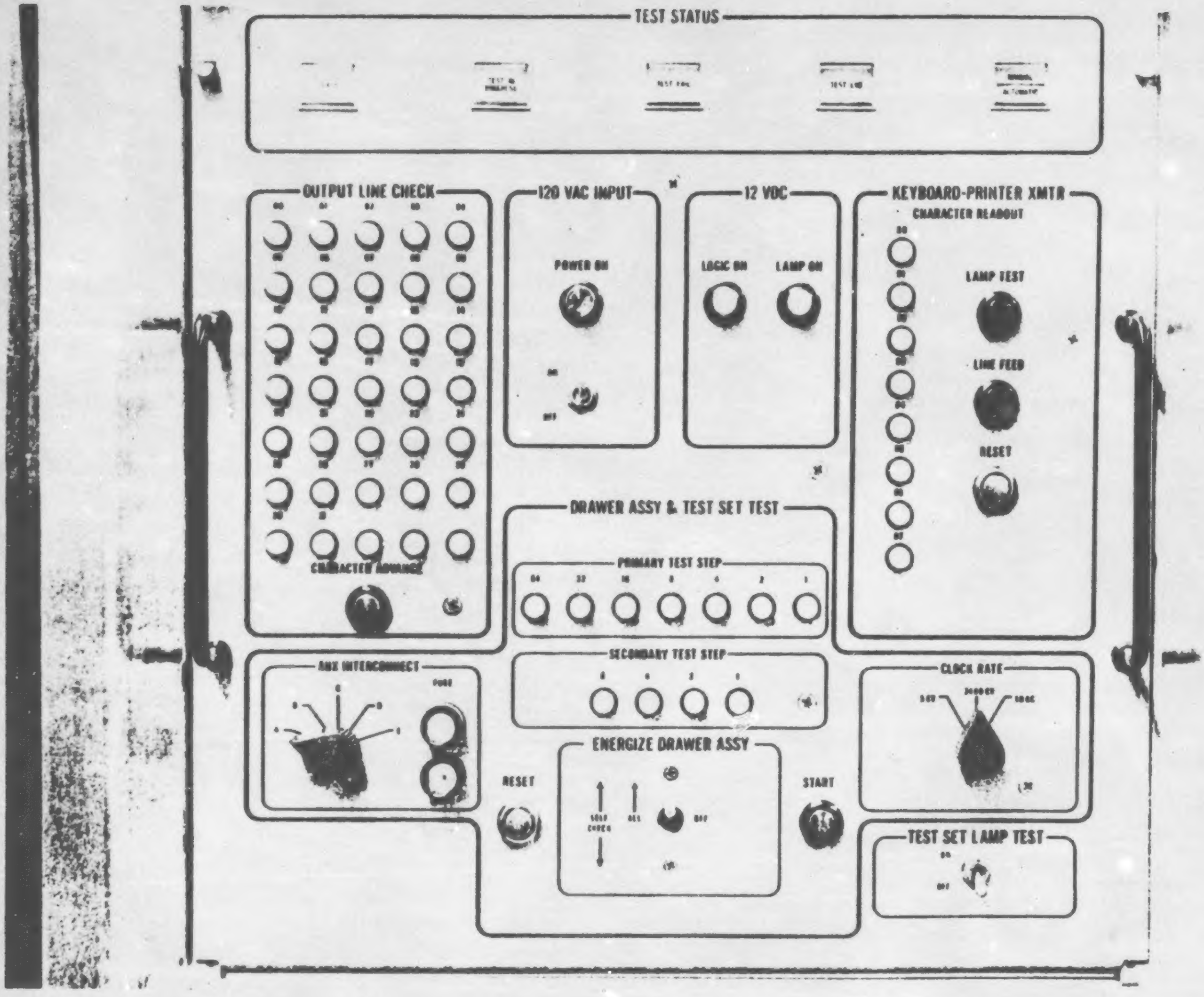

TEST STATUS
OUTPUT LINE CHECK
CHARACTER ADVANCE
120 VAC INPUT
POWER ON
12 VDC
LOGIC ON
LAMP ON
KEYBOARD-PRINTER XMTR
CHARACTER READOUT
LAMP TEST
LINE FEED
RESET
DRAWER ASSY & TEST SET TEST
PRIMARY TEST STEP
SECONDARY TEST STEP
AUX INTERCONNECT
FUSE
CLOCK RATE
RESET
ENERGIZE DRAWER ASSY
START
TEST SET LAMP TEST

Figure 93. Control panel.

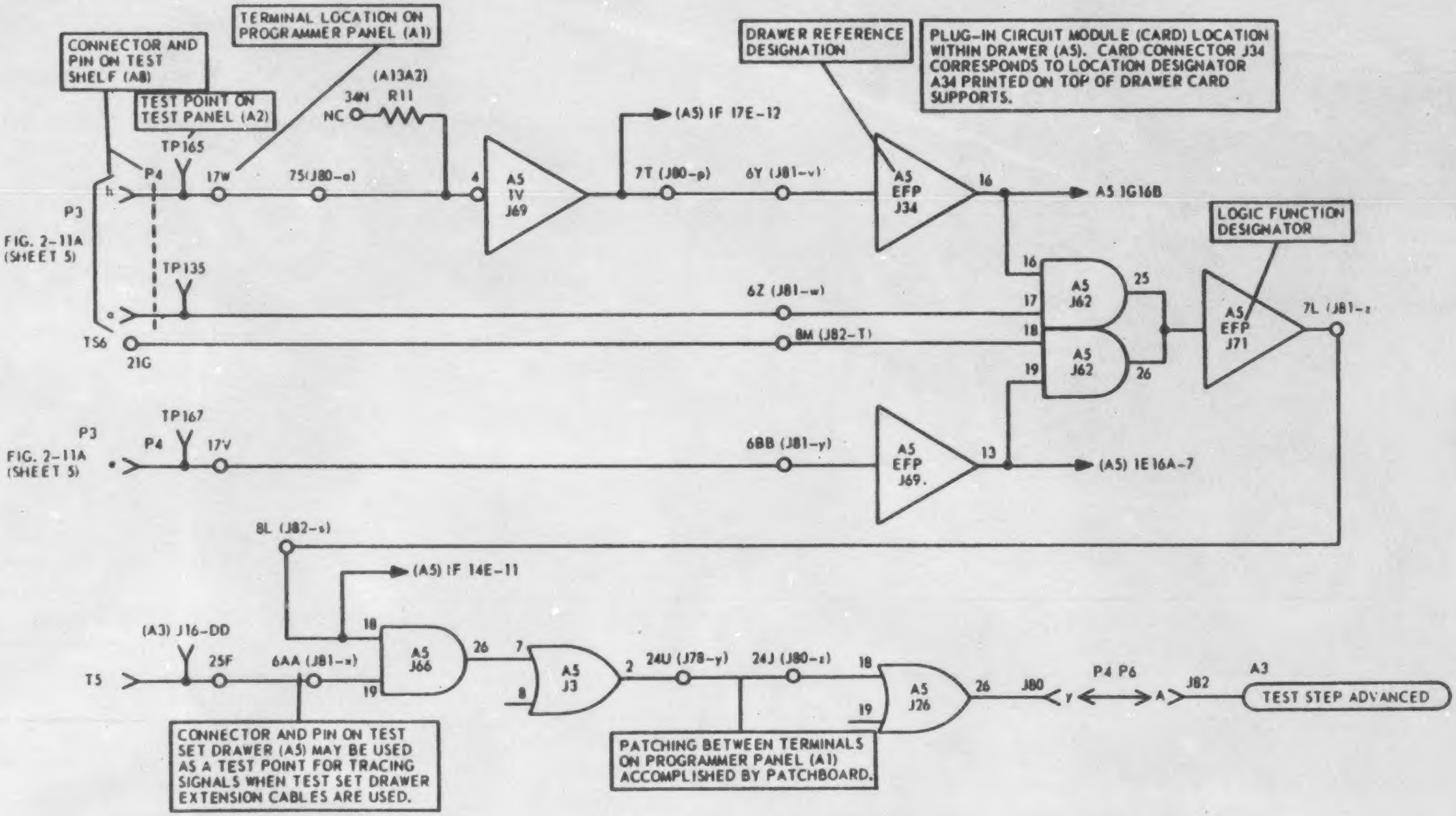

CONNECTOR AND PIN ON TEST SHELF (A8)
TEST POINT ON TEST PANEL (A2)
TERMINAL LOCATION ON PROGRAMMER PANEL (A1)
DRAWER REFERENCE DESIGNATION
PLUG-IN CIRCUIT MODULE (CARD) LOCATION WITHIN DRAWER (A5). CARD CONNECTOR J34 CORRESPONDS TO LOCATION DESIGNATOR A34 PRINTED ON TOP OF DRAWER CARD SUPPORTS.
LOGIC FUNCTION DESIGNATOR
(A13A2)
34N
R11
NC
TP165
P4
17W
75(J80-a)
4
A5
1V
J69
(A5) 1F 17E-12
7T (J80-p)
6Y (J81-v)
A5
EFP
J34
16
A5 1G16B
P3
FIG. 2-11A
(SHEET 5)
h
a
TP135
6Z (J81-w)
TS6
21G
8M (J82-T)
16
17
18
19
A5
J62
A5
J62
25
26
A5
EFP
J71
7L (J81-z)
P3
FIG. 2-11A
(SHEET 5)
P4
TP167
17V
6BB (J81-y)
A5
EFP
J69.
13
(A5) 1E16A-7
8L (J82-s)
(A5) 1F 14E-11
(A3) J16-DD
T5
25F
6AA (J81-x)
18
19
A5
J66
26
7
8
A5
J3
2
24U (J78-y)
24J (J80-z)
18
19
A5
J26
26
J80
P4 P6
y
A
J82
A3
TEST STEP ADVANCED
CONNECTOR AND PIN ON TEST SET DRAWER (A5) MAY BE USED AS A TEST POINT FOR TRACING SIGNALS WHEN TEST SET DRAWER EXTENSION CABLES ARE USED.
PATCHING BETWEEN TERMINALS ON PROGRAMMER PANEL (A1) ACCOMPLISHED BY PATCHBOARD.

Figure 98. Typical logic diagram with symbology and coding.

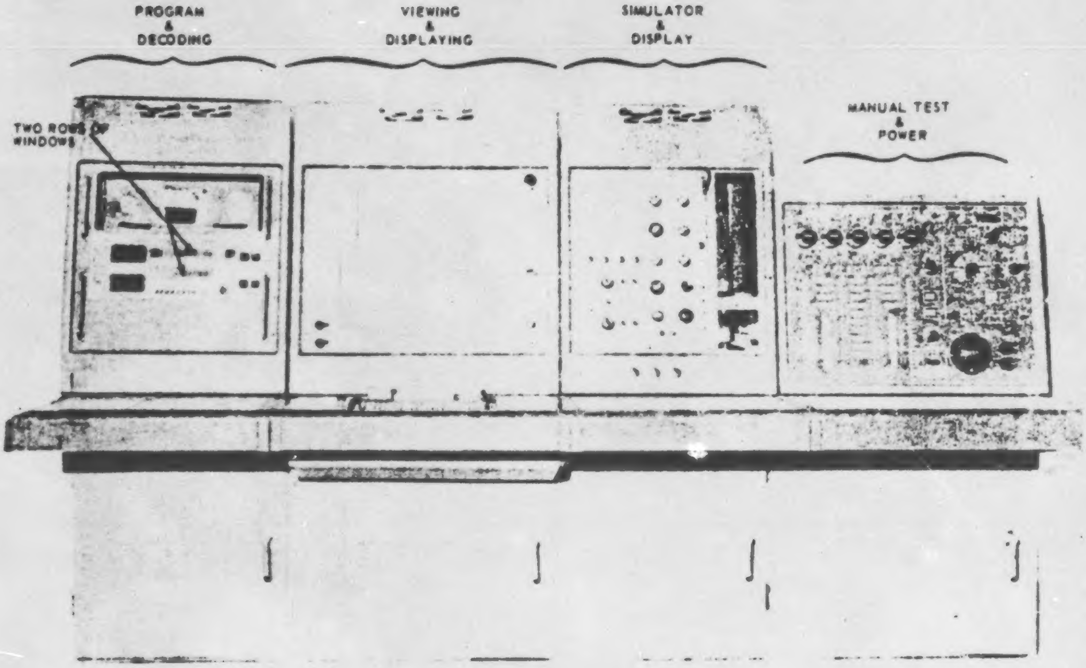

PROGRAM & DECODING
VIEWING & DISPLAYING
SIMULATOR & DISPLAY
MANUAL TEST & POWER
TWO ROWS OF WINDOWS

Figure 102. Card tester. AN/GPM-50.

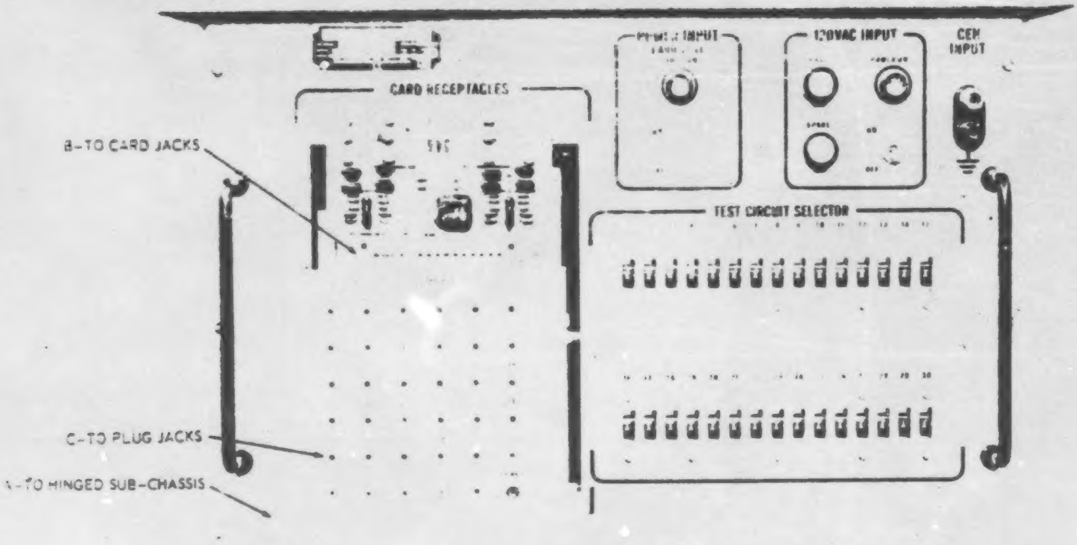

CARD RECEPTACLES
POWER INPUT
120VAC INPUT
CEM INPUT
TEST CIRCUIT SELECTOR
B-TO CARD JACKS
C-TO PLUG JACKS
A-TO HINGED SUB-CHASSIS

Figure 103. Card tester, TS1996/FYQ.

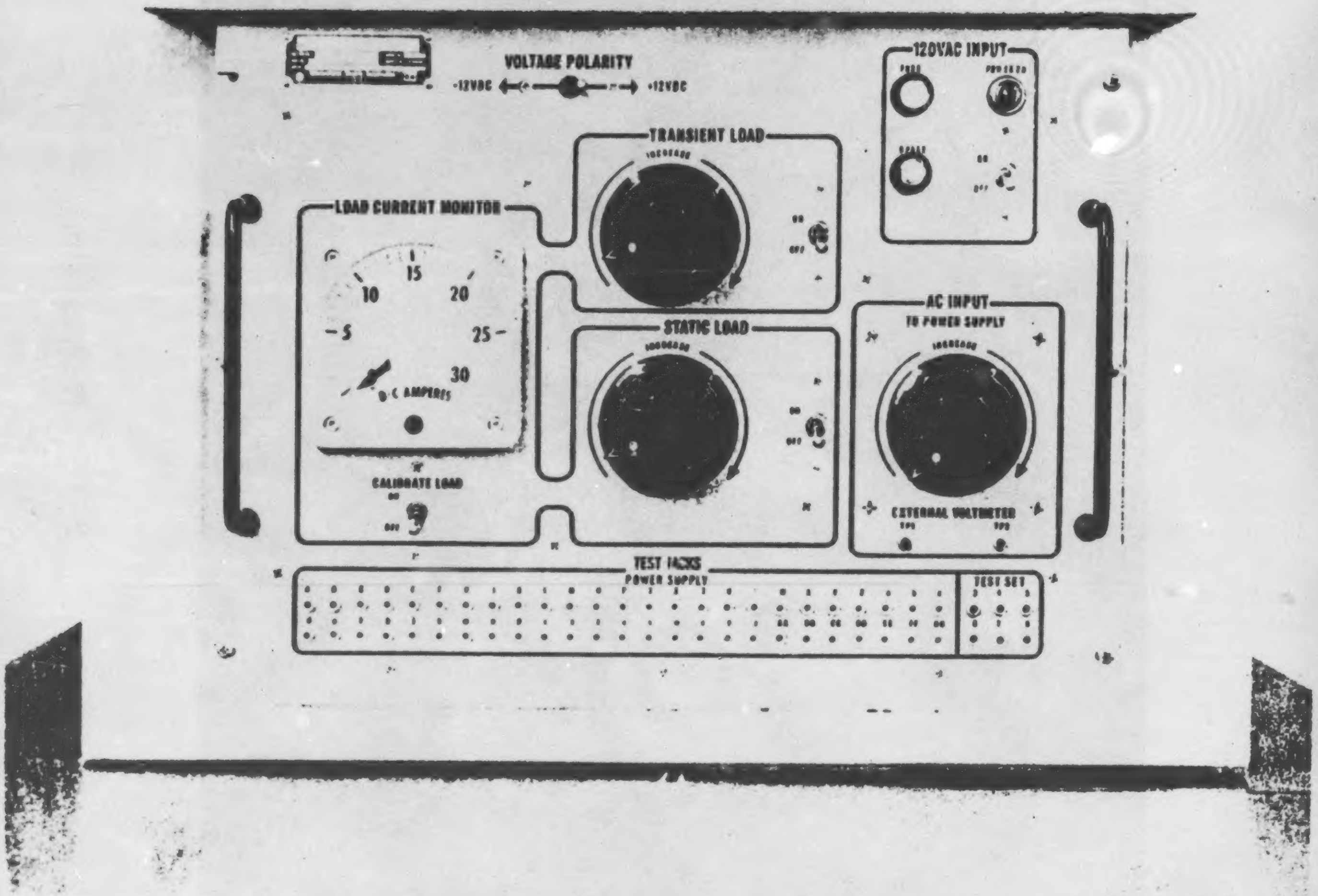
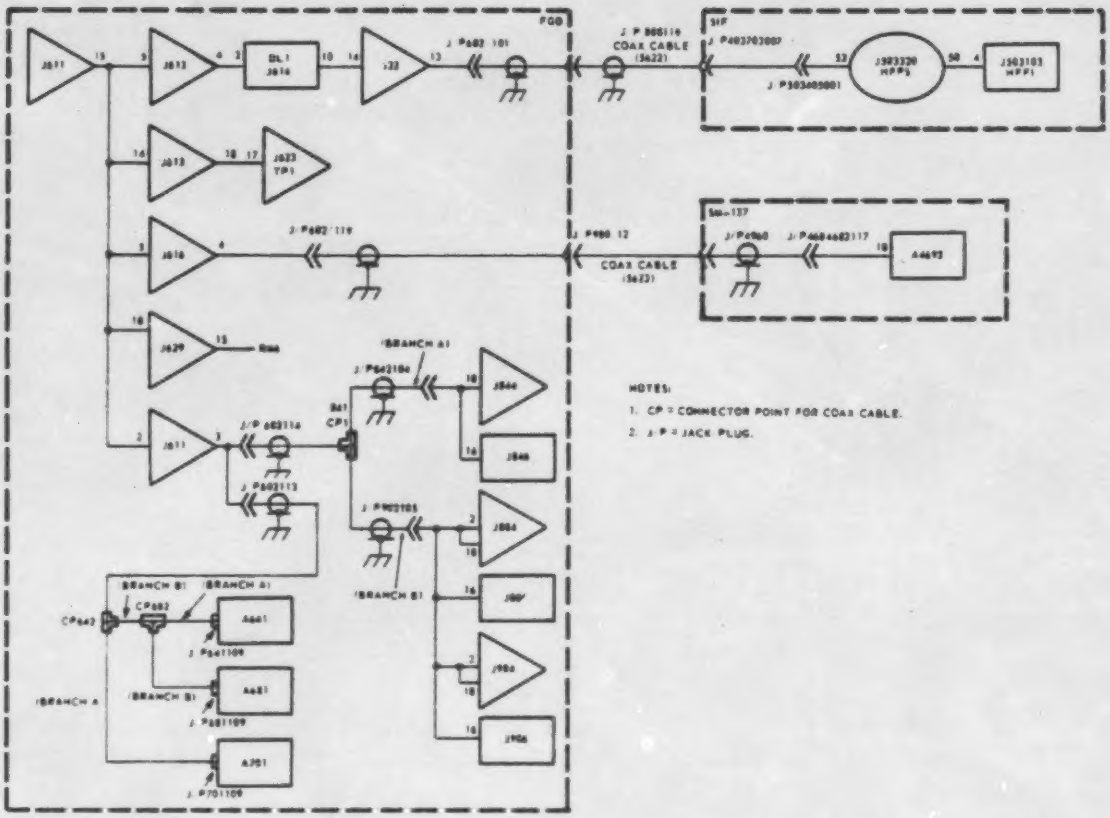

VOLTAGE POLARITY
-12VDC
+12VDC
120VAC INPUT
FUSE
POWER ON
SPARE
ON
OFF
TRANSIENT LOAD
INCREASE
LOAD CURRENT MONITOR
5
10
15
20
25
30
D.C AMPERES
CALIBRATE LOAD
STATIC LOAD
AC INPUT
TO POWER SUPPLY
EXTERNAL VOLTMETER
TEST JACKS
POWER SUPPLY
TEST SET

Figure 105. Power supply test set, TS1846/FYQ.

MODIFICATIONS

Pages 69-71 of this publication has (have) been deleted in adapting this material for inclusion in the "Trial Implementation of a Model System to Provide Military Curriculum Materials for Use in Vocational and Technical Education." Deleted material involves extensive use of military forms, procedures, systems, etc. and was not considered appropriate for use in vocational and technical education.


FGD
J611
J613
DL1
J616
J22
J/P682 101
J/P 888116
COAX CABLE
(3622)
SIP
J/P403703007
J/P303405001
J303320
HPPS
J303103
HPP1
J613
J623
TP1
J616
J/P682 119
J/P980 12
COAX CABLE
(3623)
J/P4960
J/P4684682117
A4693
J629
(BRANCH A)
J/P842106
841
CP1
J844
J848
J611
J/P 682114
J/P682113
J/P902105
J884
J887
J904
J906
(BRANCH B)
BRANCH B)
(BRANCH A)
CP642
CP682
A641
J/P641109
(BRANCH B)
A681
J/P681109
(BRANCH A
A701
J/P701109

NOTES:

1. CP = CONNECTOR POINT FOR COAX CABLE.
2. J/P = JACK PLUG.

Figure 53. Signal RM3 routing.

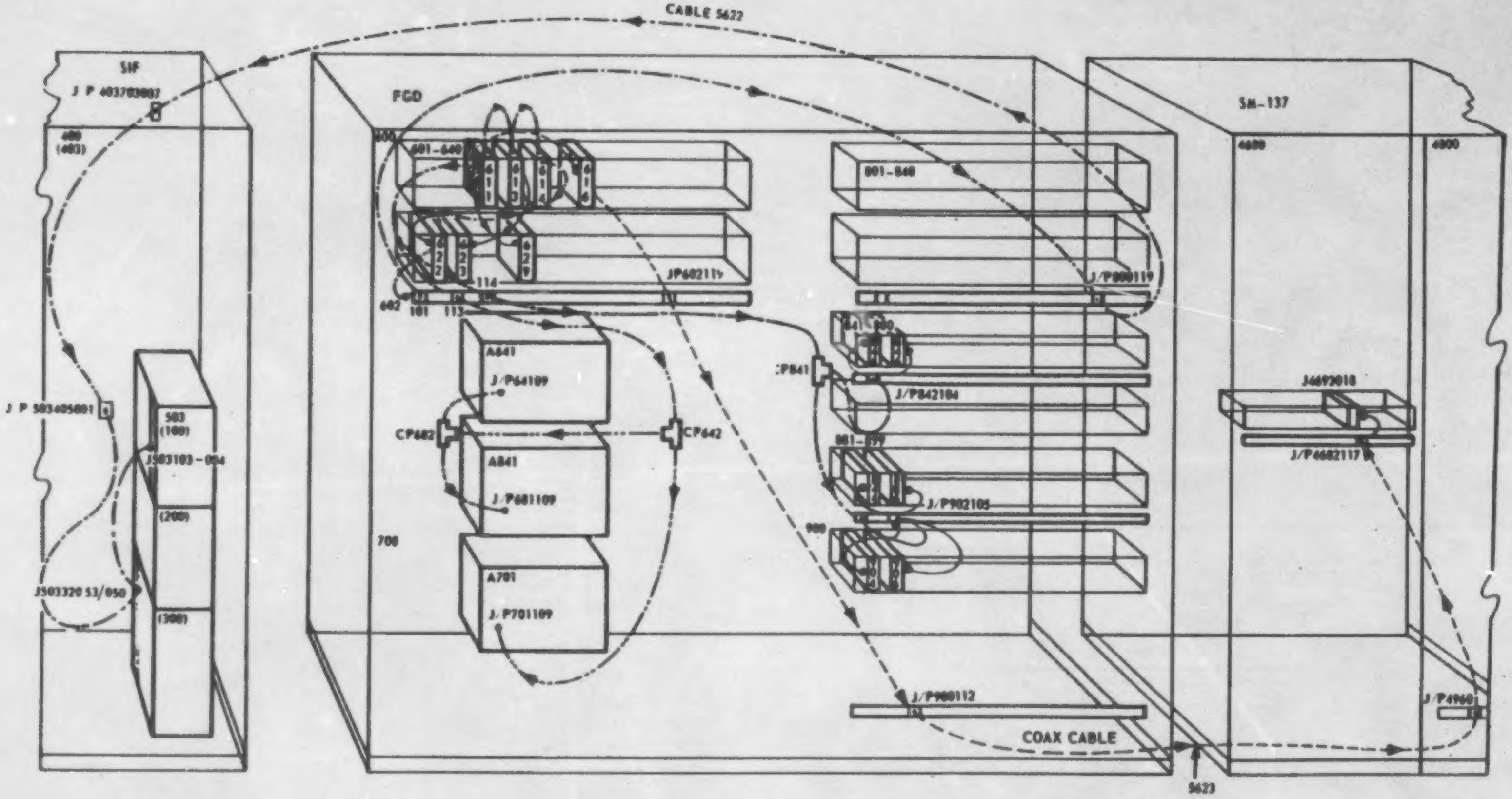

CABLE 5622
SIF
J P 403703007
400
(403)
J P 503405001
503
(100)
J503103-004
(200)
J503320 53/050
(300)
FGD
600
601-640
611
613
614
616
622
623
629
114
JP602119
602
101
113
A641
J/P64109
CP682
CP642
A841
J/P681109
700
A701
J/P701109
801-840
J/P800119
841-880
:P841
J/P842104
881-899
J/P902105
900
J/P900112
COAX CABLE
5623
SM-137
4600
4900
J4693018
J/P4682117
J/P4960

Figure 54. Signal RMS routing pictorial.

1. Origin (RM3 to RM6) ________ ________ Terminating Jack.

2. Origin (RM3 to TP1) ________ ________ ________ Terminating Jack.

3. Origin (RM3 to SIF) ________ ► ________ ► ________ ► ________ ► ________ Bay Jack/Plug ________ Bay Jack/Plug

________ Cable ________ Cabinet Jack ________ Drawer Jack ________ ________ Terminating Jack.

4. Origin (RM3 to SM 137) ________ ________ ________ Bay Jack ________ Bay Jack ________ Cable ________ Rack Jack

________ Rack Jack ________ Terminating Jack.

5. Origin (RM3 to Assemblies in Bay 600) ________ ________ ________ Bay Jack ________ Connector Pt Branch A / Branch B

Branch A ________ Jack/Plug ________ Terminating Assembly. Branch B ________ Connecting Pt ________ A to Jack/Plug ________ Terminating Assembly.

________ B to Jack/Plug ________ Terminating Assembly.

6. Origin (RM3 to Bay 800 - 900 ________ ________ ________ Bay Jack/Plug ________ Connector Pt ________ Branch A Jack/Plug / ________ Branch B Jack/Plug

Branch A ________.

________. Terminating Jacks

Branch B ________. ________.

________. ________. Terminating Jacks

CHART 1

WIRING LIST FOR SIGNALS (HORIZONTAL TECHNIQUES)

AU GAFB, ALA. (7304

30554 01A 7505

CDC 30554

ELECTRONIC COMPUTER SYSTEMS REPAIRMAN

(AFSCs 30554/54A/54B/54C/54D)

Volume 1A

Computer Principles

7-4

Extension Course Institute
Air University

177

Preface

THIS VOLUME 1A of Course 30554, *Electronic Computer Systems Repairman*, is a refresher course to review and extend your basic knowledge of computer principles. This review is to prepare you for upgrading in your AFSC.

You will find that the principles presented in this volume will enhance your understanding of computer circuits. In Chapter 1, we discuss numbering systems. Chapter 2 is devoted to computer circuits. Chapters 3, 4, and 5 deal with computer components, computer units, and input and output units. Chapter 6 discusses computer power supplies.

Foldout 1 is included as a separate insert in the back of this volume.

If you have questions on the accuracy or currency of the subject matter of this text, or recommendations for its improvement, send them to USAFSAAS/TTOC, Keesler AFB MS 39534. NOTE: Do not use the suggestion program to submit corrections for typographical or other errors.

If you have questions on course enrollment or administration, or on any of ECI's instructional aids (Your Key to Career Development, Study Reference Guides, Chapter Review Exercises, Volume Review Exercise, and Course Examination), consult your education officer, training officer, or NCO, as appropriate. If he can't answer your questions, send them to ECI, Gunter AFS AL 36118, preferably on ECI Form 17, Student Request for Assistance.

This volume is valued at 36 hours (12 points).

Material in this volume is technically accurate, adequate, and current as of December 1974.

Contents

Page

Preface . . . . *iii*

Chapter

1 **Number Systems** 1

2 **Computer Circuits** 11

3 **Computer Components** 54

4 **Computer Units** 84

5 **Input-Output Units** 114

6 **Computer Power Supplies** 142

LIST OF CHANGES

COURSE NO. 30554	CAREER FIELDS, POLICIES, PROCEDURES AND EQUIPMENT CHANGE. ALSO ERRORS OCCASIONALLY GET INTO PRINT. THE FOLLOWING ITEMS UPDATE AND CORRECT YOUR COURSE MATERIALS. PLEASE MAKE THE INDICATED CHANGES.
EFFECTIVE DATE OF SHIPPING LIST 10 Feb 76	

1. CHANGES FOR THE TEXT: VOLUME 2

a. Page 16, Figure 24: Change "CURRENT ADJ (CAPACITIVE IN EMITTER CKT)" to "CURRENT ADJ (RISISTIVE IN EMITTER CKT)." Change "PEAKING ADJ (RESISTIVE IN EMITTER CKT)" to "PEAKING ADJ (CAPACITIVE IN EMITTER CKT)."

b. Page 57, para 13-5, table: Change "d. tape" from the column labeled "Either or Combined Mode" to the column labeled "Sequential."

c. Page 84, Figure 107: Change "C/N" to "C/M."

2. CHANGES FOR THE VOLUME WORKBOOK: VOLUME 1

a. Page 3, Chapter Review Exercises, question 18: Delete.

b. Page 17, Chapter Review Exercises, question 5: Change "Records" to "Documentation." Change "Workload Control" to "Plans and Scheduling."

c. Page 18, Chapter Review Exercises, question 17: Delete.

d. Page 20, Chapter Review Exercises, answer 18: Delete.

e. Page 25, Chapter Review Exercises, answer 22: Change ".02 x 3.5 = .07V peak to peak" to ".2 x 3.5 = .7V peak to peak."

f. Page 27, Chapter Review Exercises, answer 3: Change "500" to "501."

g. Page 28, Chapter Review Exercises, answer 14: Change "DD Form 829-1" to "AFTO Form 95." Answer 17: Delete.

h. The following questions are no longer scored and need not be answered: 16, 56, 57, 74, 76, 88, 96, 98, 100, 101, 103 and 110.

3. CHANGES FOR THE VOLUME WORKBOOK: VOLUME 1A

a. Page 13, Chapter Review Exercises, question 34: Delete the period at the end of statement and add "with Q2 conducting prior to TO."

b. Page 16, Chapter Review Exercises, question 48: Delete.

c. Page 18, Chapter Review Exercises, question 8: Change "12" to "13."

d. Page 22, Chapter Review Exercises, question 30: Delete the question mark and add "at the 7 detect line?"

LIST OF CHANGES

COURSE NO. 30554	CAREER FIELDS, POLICIES, PROCEDURES AND EQUIPMENT CHANGE. ALSO ERRORS OCCASIONALLY GET INTO PRINT. THE FOLLOWING ITEMS UPDATE AND CORRECT YOUR COURSE MATERIALS. PLEASE MAKE THE INDICATED CHANGES.
EFFECTIVE DATE OF SHIPPING LIST 10 Feb 76	

3. CHANGES FOR THE VOLUME WORKBOOK: VOLUME 1A (Continued)

e. Page 32, Chapter Review Exercise, answer 6: Change "b. Shunt negative limiter" to "b. Negative clamper." Change "c. Negative clamper" to "c. Series positive limiter." Change "d. Positive clamper" to "d. Shunt negative limiter." Change "e. Series positive limiter" to "e. Positive clamper."

f. Page 35, Chapter Review Exercise, answer 48: Delete.

4. CHANGE FOR THE VOLUME WORKBOOK: VOLUME 2

The following questions are no longer scored and need not be answered: 1, 41, 51 and 84.

NOTE: Change the currency date on all volumes to "December 1975."

Number Systems

REMEMBER YOUR formal school training days? Many of us just about "flipped out" when first introduced to the binary, octal, and hexadecimal number systems. We were so oriented to working with one number system (namely, the decimal system) that it was difficult for us to adapt our thinking to another number system, let alone three of them. However, you were able to "weather the storm," complete your technical training course, and make it out into the field of computer maintenance. But, we tend to forget the basic rules of mathematics if not used often enough. How is your memory concerning the basic rules involved in using the decimal, binary, octal, and hexadecimal number systems? Have you forgotten them since leaving formal technical training? Because a good working knowledge of these number systems is so important in computer maintenance, a review of each system is presented in this chapter.

1. Number System Features

1-1. In this section, we review five features of a number system and explain how the decimal, binary, octal, and hexadecimal number systems are used in association with computers.

1-2. **Place-Value.** The decimal number system, which is widely used today, uses 10 different basic symbols: 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. Each of these symbols is called a *digit.* A decimal number, regardless of its value, is comprised of one or more of these digits. In order to represent a number larger than 9, place-values are used; *place,* in this case, is the position of a digit with respect to the decimal point. Place value is sometimes referred to as *positional notation.* For example, take a look at the place-value of each digit in the number (1,023.754) below.

Digit	*Place-Value*
1	Thousands
0	Hundreds
2	Tens
3	Units
.	Point
7	Tenths
5	Hundredths
4	Thousandths

1-3. When the idea of place-value was first developed, a space was used to indicate that no quantity appeared in a place-position. For example, 205 was written 2 5 and 5,008 appeared as 5,   8. You can see that this leads to confusion. Does 2 5 mean 25 or 205, etc.? This defect led to the development of the place-holder system using a zero. Although zero has a numerical value meaning "no quantity," it serves a very important function as a place-holder in mathematics. The idea of place-value is familiar to us through its use in the decimal number system; for example, the zeros in 505, 5,005, and 50,005 are used to insure that the place-positions of all digits in the numbers are positively located and identified.

1-4. **Radix.** The number of different digits used in a number system is called its *radix* or *base*. Although many number systems are possible that have a radix larger than 1, only a few of them lend themselves to computer use. Some of these are the binary system with a radix of 2, the octal system with a radix of 8, and the hexadecimal system with a radix of 16.

1-5. The radix of a number system is written as a subscript to a number. For example, in the number 10_2, the subscript 2 identifies the number system and the total quantity of different numerals that are used with the particular system. Let us say that we want to indicate any and all quantities of a number system by the use of only two digits: 0 and 1. Since the quantity of different digits

TABLE 1-1
NUMBER SYSTEMS

NUMBERING SYSTEM BASES (RADIX)

TWO	THREE	FOUR	FIVE	SIX	SEVEN	EIGHT	NINE	TEN	ELEVEN	TWELVE	SIXTEEN
0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1
10	2	2	2	2	2	2	2	2	2	2	2
11	10	3	3	3	3	3	3	3	3	3	3
100	11	10	4	4	4	4	4	4	4	4	4
101	12	11	10	5	5	5	5	5	5	5	5
110	20	12	11	10	6	6	6	6	6	6	6
111	21	13	12	11	10	7	7	7	7	7	7
1000	22	20	13	12	11	10	8	8	8	8	8
1001	100	21	14	13	12	11	10	9	9	9	9
1010	101	22	20	14	13	12	11	10	A	A	A
1011	102	23	21	15	14	13	12	11	10	B	B
1100	110	30	22	20	15	14	13	12	11	10	C
1101	111	31	23	21	16	15	14	13	12	11	D
1110	112	32	24	22	20	16	15	14	13	12	E
1111	120	33	30	23	21	17	16	15	14	13	F
10000	121	100	31	24	22	20	17	16	15	14	10
10001	122	101	32	25	23	21	18	17	16	15	11
10010	200	102	33	30	24	22	20	18	17	16	12
10011	201	103	34	31	25	23	21	19	18	17	13
10100	202	110	40	32	26	24	22	20	19	18	14
10101	210	111	41	33	30	25	23	21	1A	19	15
10110	211	112	42	34	31	26	24	22	20	1A	16
10111	212	113	43	35	32	27	25	23	21	1B	17
11000	220	120	44	40	33	30	26	24	22	20	18
11001	221	121	100	41	34	31	27	25	23	21	19

NDA6-2

used is 2, the radix is 2, and the *binary number system* is indicated. In the binary system, only a 0 or a 1 occurs in a place-position of the number. Examples: 11011_2, 1010101_2, 11111_2, etc.

1-6. For another example of radix, let's use eight digits (0, 1, 2, 3, 4, 5, 6, and 7) to write any or all numbers. Since eight different digits are used, the radix is 8, and the *octal number system* is indicated. In the octal system, only 0 through 7 occurs in a place-position of the number. Examples: 725_8, 5063_8, 77413_8, etc.

1-7. Now refer to table 1-1 and notice that in each system represented, the point where the system increases to the next position (next higher power) is equal to the total number of digits used in that system. For example, base two system has a *zero* and a *one*, then increments to its next position at the decimal count of 2 (its radix). Also, note at this time that any number system with a radix larger than 10 uses alpha characters as well as digits.

1-8. The Point. A point (.) is a period that is used to separate fractional parts of a number from whole parts. The point assumes the name of the number system in which it is used; that is, in the binary system it is called the *binary point*, and it is called the *octal point* when used in the octal system.

1-9. Least Significant Digit. In number systems using positional value notation, the digit that carries the least weight (value) is called the *least significant digit* (LSD). The LSD occupies the *units column* in whole numbers. In the decimal system, the LSD seldom occupies any position other than the one on the extreme right of the number. However, in other systems, the LSD may not always occur on the right of the number, especially if it is a number that has been manipulated by a computer. Some computers have been known to show the LSD of a number on the left. This should not present any confusion, however, as long as it is indicated that the LSD is on the left.

1-10. Most Significant Digit. The *most significant digit* (MSD) of a number is the digit that carries the most weight, and, unless otherwise noted, it is the digit to the extreme left of a number. For example, in the number $3,286_{10}$, the 3 is the MSD because it represents 3,000. Also, the 6 is the LSD because it represents only six.

1-11. The application of these features simplifies the understanding of any number system, regardless of its radix. Therefore, in the discussion of specific number systems that follow, we utilize these features to simplify your understanding of determining the value of a number in a given number system.

2. Basic Numbering System

2-1. In the following text, we discuss four basic numbering systems. They are: decimal, binary, octal, and hexadecimal. There are other number systems, but these four are commonly used in computers.

2-2. Decimal System. As stated earlier, place-value is an important concept in determining the value of a number. Each digit position in the decimal system is called a *decade*, which is sometimes referred to as an *order*. Each decade is valued at 10 times the decade positioned to its right, as in the following example:

$$
\begin{array}{rr}
512_{(10)} = & +500 \\
 & +\ 10 \\
 & +\ \ 2 \\
\hline
 & 512_{(10)}
\end{array}
$$

To determine the place-value of a number in the decimal system, you start at the point and, working to the left, the radix is raised to successive *positive* powers. If the number contains digits to the right of the decimal point, start at the point and, working to the right, the radix is raised to successive *negative* powers. An example of this concept for the number 7,538.75 follows. Note that any number raised to 0 power is equal to 1.

Power of Radix	10^3	10^2	10^1	10^0	10^{-1}	10^{-2}
Decimal Value	1,000	100	10	1	1/10 or .1	1/100 or .01
Example Decimal #	7	5	3	8	7	5
Decimal Equivalent	7,000	500	30	8	.7	.05

To determine the decimal value of our example number, multiply the decimal place-value of each place-position by the decimal digit occupying that particular position:

$$
\begin{array}{rrcr}
7 \times & 1,000 & = & 7,000 \\
5 \times & 100 & = & 500 \\
3 \times & 10 & = & 30 \\
8 \times & 1 & = & 8 \\
7 \times & .1 & = & .7 \\
5 \times & .01 & = & .05 \\
\hline
 & & & 7,538.75
\end{array}
$$

2-3. Binary System. This system is based on a radix of 2. Only digits 0 and 1 are used

TABLE 1-2
RELATIONSHIP BETWEEN NUMBERS IN DECIMAL, BINARY, AND GRAY CODE

Decimal	Binary	Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000
16	10000	11000

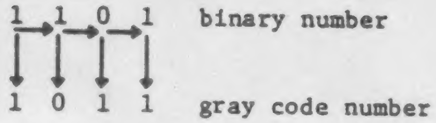
NDA6-3

to represent a binary number. Place-value is determined in the same manner as in the decimal system. That is, the radix is raised to successive powers starting at the point (binary point in this case) and working in either direction. This means that the first position to the left of the point is equal to 2^0, the next location 2^1, etc. The first position to the right of the point is 2^{-1}, the next location 2^{-2}, etc. An example of this concept for the binary number 1011.011 follows:

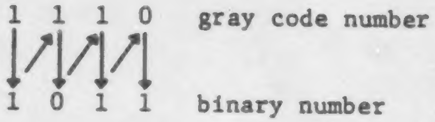
Power of Radix	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}
Decimal Value	8	4	2	1	1/2 or .5	1/4 or .25	1/8 or .125
Example Binary #	1	0	1	1	0	1	1
Decimal Equivalent	8	0	2	1	0	.25	.125

To determine the decimal value of our example number, multiply the decimal place-value of each place-position by the binary digit occupying that particular position:

$$\begin{array}{lcr} 1 \times 8 & = & 8 \\ 0 \times 4 & = & 0 \\ 1 \times 2 & = & 2 \\ 1 \times 1 & = & 1 \\ 0 \times 1/2 & = & 0 \\ 1 \times 1/4 & = & .25 \\ 1 \times 1/8 & = & .125 \\ \hline & & 11.375 \end{array}$$



A. Binary To Gray



B. Gray To Binary

NDA6-1

Figure 1-1. Converting.

2-4. Binary Number System Variations. Two variations of the binary number system are the *gray code* and the *binary coded decimal*. They are considered a variation of the basic binary number system because of their use of binary symbols 0 and 1.

2-5. *Gray code*. This variation is also called the *reflected or cyclic code*. A useful application of this code is found in some types of analog-to-digital and digital-to-analog conversion equipment. Its advantage over the basic binary system is derived from the fact that successive integers differ one from the next by only one digit. This reduces the degree of error which might possibly occur when numbers are transferred within a computer system. Table 1-2 shows the relationships between numbers in decimal, binary, and gray codes. Notice that a change from $0111_{(2)}$ to $1000_{(2)}$ requires a change from three ones and a zero to three zeros and a one. Thus, all digits were changed simultaneously for a consecutive count; whereas in the gray code, consecutive numbers differ by a change of only one digit. The usefulness of the gray code does not extend to arithmetic operations; even simple addition is relatively difficult in the gray code. For this reason, a computer working with this code converts back and forth between gray code and binary during arithmetic operations.

2-6. A pencil-and-paper method of gray-code conversions is shown in figure 1-1. Part A of the figure illustrates a binary-to-gray conversion; refer to part A for this discussion. To convert a binary number to gray code, write the MSD (a 1) of the binary number as the MSD of the gray code number. The sum of the first (MSD) and second (a 1) binary digits (disregard a carry, if any) becomes the second digit (a 0) of the gray code number. The sum of the second and third (a 0) binary digits (again disregard a carry, if any) becomes the third digit (a 1) of the gray code number. The sum of the third and fourth (a 1) binary digits (again disregard a carry, if any) becomes the fourth digit (a 1) of the gray code number. The result of the binary-to-gray conversion in our example is binary number 1101 converts to gray code number 1011. For larger numbers requiring conversion, the summing process of using the next digit to the right would continue until the LSD of the binary number was converted. Now, let's convert a gray code number to a binary number.

2-7. Part B of figure 1-1 illustrates a gray-to-binary conversion; refer to part B for this discussion. Note that we also disregard any carry when summing digits in a gray-to-binary conversion. The MSD (a 1) of the gray code number becomes the MSD of the binary number. The second binary number (a 0) is the sum of the binary number just found (the MSD) and the second gray code digit (a 1). The third binary number (a 1) is the sum of the second binary digit just found and the third gray code digit (a 1). The fourth binary number (a 1) is the sum of the third binary digit just found and the fourth gray code digit (a 0). The result of the gray-to-binary conversion in our example is that gray code number 1110 converts to binary number 1011. For larger numbers requiring conversion, the summing process would continue until the LSD of the gray code number was converted.

TABLE 1-3
RELATIONSHIP BETWEEN NUMBERS IN DECIMAL AND BINARY CODED DECIMAL

Decimal	Binary Coded Decimal
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

NDA6-4

2-8 *Binary-coded decimal.* In certain applications of computer operation, it is desirable to convert an entire decimal number into a binary equivalent. Instead of a true conversion to binary, the binary-coded decimal (BCD) codes each of the 10 decimal numerals into a four-digit binary number. Another name for this system is the 8421 code. This name is derived from the fact that the symbols 8, 4, 2, and 1 are the place-values of the digits in a four-digit binary number. The 10 decimal numerals are coded in BCD as shown in table 1-3.

2-9. In BCD, decimal number 74 is written 0111 0100, and decimal number 3,084 is written 0011 0000 1000 0100. You can see from these examples that in BCD each decimal digit is coded separately to a binary form; that is, $01110100_{(2)}$ is not equal to $74_{(10)}$, but $0111\ 0100_{(BCD)}$ is equal to $74_{(10)}$. There are many more uses for BCD than we have explained here. For example, in Section 3 of this chapter, BCD is used for converting hex numbers to a usable form for computer arithmetic operations. Also, in many systems using light emitting diodes (LEDs) or nixie tubes for displays (or fault indicators), you might find that a BCD code is used in the selection of a character to be displayed.

2-10. **Octal System.** The radix of the octal system is 8. Only digits 0 through 7 are used to represent an octal number. Place-value is determined in the same manner as in the decimal system. That is, the radix is raised to successive powers starting at the point (octal point in this case). An example of this concept for the octal number 7014.36 follows:

Power of Radix	8^3	8^2	8^1	8^0	8^{-1}	8^{-2}
Decimal Value	512	64	8	1	1/8 or .125	1/64 or .015625
Example Octal #	7	0	1	4	3	6
Decimal Equivalent	3584	0	8	4	.375	.093750

To determine the decimal value of our example, multiply the decimal place-value of each place-position by the octal digit occupying that particular position:

$$\begin{array}{rrcr}
7 \times & 512 & = & 3584 \\
0 \times & 64 & = & 0 \\
1 \times & 8 & = & 8 \\
4 \times & 1 & = & 4 \\
3 \times & .125 & = & .375 \\
6 \times & .015625 & = & .093750 \\
\hline
 & & & 3{,}596.46875
\end{array}$$

2-11. **Hexadecimal System.** The hexadecimal system (sometimes called hex) is based on a radix of 16. The representation of 16 possible digits presents a problem because there are only 10 decimal digits to work with. However, this problem is resolved by using the letters A, B, C, D, E, and F to represent numbers 10, 11, 12, 13, 14, and 15, respectively. Thus, the complete character set for hex is 0 through 9 and A through F; this is shown in table 1-1 under the base 16 column. Again, place-value is determined in the same manner as in the decimal system. That is, the radix is raised to successive powers starting at the point (hex point, in this case). An example of this concept for the hex number 9A1B.4C follows:

Power of Radix	16^3	16^2	16^1	16^0	16^{-1}	16^{-2}
Decimal Value	4096	256	16	1	1/16 or .0625	1/256 or .00390625
Example Hex #	9	A	1	B	4	C
Decimal Equivalent	36,864	2,560	16	11	.25	.046875

To determine the decimal value of our example, multiply the decimal place-value of each place-position by the hex digit (where a letter is used as the digit equivalent) occupying that particular position:

$$\begin{array}{lcrcr}
9 & \times & 4096 & = & 36{,}864 \\
A(10) & \times & 256 & = & 2{,}560 \\
1 & \times & 16 & = & 16 \\
B(11) & \times & 1 & = & 11 \\
4 & \times & .0625 & = & .25 \\
C(12) & \times & .00390625 & = & .046875 \\
\hline
 & & & & 39{,}451.296875
\end{array}$$

2-12. It has been said, "The easiest way for a person to do something is to do it the way that is easiest for him." This is also true when determining the decimal value of a number, regardless of the number system involved. We discussed only one method of determining the value of a specific number. No doubt there are countless other methods of doing the same thing. Your personal method might be quicker and easier than that presented here; if it is, by all means use it on the job. But, if you do not have your own method, use the one we have presented. This same fact holds true for number systems conversion; that is, converting a binary number to octal, hexadecimal to binary, etc. The methods we present may or may not be as easy or as quick as yours. However, if you do not have a method of converting numbers from one system to another, use those that are presented in this chapter.

3. Number System Conversions

3-1. In order to check results of calculations as they appear internally in a computer, it is often helpful to be able to convert numbers from one number system to another. Conversion also aids troubleshooting by enabling the maintenance man to determine the contents of registers or the specific address of a failing memory location.

3-2. Conversion from Decimal to Any System. Successive divisions of a decimal number by the base (radix) of another system enables you to convert a decimal number to that system. The division process is completed when the quotient of zero is reached. The equivalent in the new system is formed by listing the remainder of each division beginning with the last one produced. The first remainder becomes the least significant (LSD) and the last remainder becomes the most significant (MSD) for the equivalent number. In the case of the hexadecimal system (or any system which uses letters to represent numbers), these remainders may have to be individually translated to their proper letter equivalents. Let's look at a few examples.

3-3. *Decimal to binary:* $25_{(10)} = ?_{(2)}$

- Divide $25_{(10)}$ by base 2.

	Quotient		*Remainder*
25 ÷ 2 =	12	+	1 (LSD)
12 ÷ 2 =	6	+	0
6 ÷ 2 =	3	+	0
3 ÷ 2 =	1	+	1
1 ÷ 2 =	0	+	1 (MSD)

- Result: $25_{(10)} = 11001_{(2)}$

3-4. *Decimal to octal:* $5{,}175_{(10)} = ?_{(8)}$

- Divide $5{,}175_{(10)}$ by base 8.

	Quotient		*Remainder*
5,175 ÷ 8 =	646	+	7 (LSD)
646 ÷ 8 =	80	+	6
80 ÷ 8 =	10	+	0
10 ÷ 8 =	1	+	2
1 ÷ 8 =	0	+	1 (MSD)

- Result: $5{,}175_{(10)} = 12{,}067_{(8)}$

3-5. *Decimal to hexadecimal:* $4{,}987_{(10)} = ?_{(16)}$

- Divide $4{,}987_{(10)}$ by base 16.

	Quotient		*Remainder*
4,987 ÷ 16 =	311	+	11 = B (LSD)
311 ÷ 16 =	19	+	7
19 ÷ 16 =	1	+	3
1 ÷ 16 =	0	+	1 (MSD)

- Result: $4{,}987_{(10)} = 137B_{(16)}$

3-6. **Conversion from Any System to Decimal.** There are two methods commonly used for converting numbers from a specific system to decimal. The first method is the same as that presented in Section 2 of this chapter. That is, determine each digit's place-value, multiply this place-value by the number coded in that position, and then add up the values of all the positions to determine the overall decimal value. This particular method becomes cumbersome when converting large numbers of one system to its equivalent value in another number system. Another method of converting any number (especially large numbers) to the decimal system does away with the need of determining place-values. This second method of converting any system to decimal is called the *double-dabble* method. In using this method, the digit to the extreme left is multiplied by the radix of the system, and the next position to the right is added to the result. This process is continued until the units digit is reached. Once the units digit is added in, the conversion to decimal is completed.

3-7. *Binary to decimal:* $1101_{(2)} = ?_{(10)}$

- Double dabble: $1 \times 2 = 2 + 1 = 3 \times 2 = 6 + 0 = 6 \times 2 = 12 + 1 = 13_{(10)}$
- Result: $1101_{(2)} = 13_{(10)}$

3-8. *Octal to decimal:* $2{,}067_{(8)} = ?_{(10)}$

- Double dabble: $2 \times 8 = 16 + 0 = 16 \times 8 = 128 + 6 = 134 \times 8 = 1{,}072 + 7 = 1{,}079_{(10)}$
- Result: $2{,}067_{(8)} = 1{,}079_{(10)}$

3-9. *Hexadecimal to decimal:* $137B_{(16)} = ?_{(10)}$

- Double dabble: $1 \times 16 = 16 + 3 = 19 \times 16 = 304 + 7 = 311 \times 16 = 4{,}976 + B_{(11)} = 4{,}987_{(10)}$
- Result: $137B_{(16)} = 4{,}987_{(10)}$

3-10. **Converting Decimal Fractions to Any Number System.** You are probably wondering at this point why most of our examples of number system conversions haven't included numbers containing fractions. The reason for this omission is that in most instances the fractional portion of a number must be handled differently from the whole portion when converting to another number system. Examples of determining the decimal value of a binary, octal, or hexadecimal fraction were presented in Section 2. You should review this section at this time. Our discussion now concerns converting decimal fractions to any number system. This is accomplished by multiplying the given decimal fraction and each successive product (*fractional part only*) by the radix, or base, of the new system. In each multiplication, if a carry into the unit column (left of the point) occurs, this carry is a digit of the new number; otherwise, the digit is zero. The required new system digits are obtained in order from left to right. The operation can be carried out for as many places as necessary for accuracy, but once the fractional portion becomes equal to zero, you'll have the answer. Let's look at some examples.

3-11. *Decimal to binary.*

- $.15_{(10)} = ?_{(2)}$

```
•        .15
           2 (Base of new system)
(MSD)   0.30
           2
        0.60
           2
        1.20
           2 (Note: multiply only the
        0.40          fractional part)
           2
        0.80
           2
(LSD)   1.60
```

- Answer: $.15_{(10)} = .001001_{(2)}$

  (Note: answer carried only six places)

3-12. *Decimal to octal.*

- $.468750_{(10)} = ?_{(8)}$

```
             .468750
                   8 (Base of new system)
(MSD)       3.750000
                   8 (Note: multiply only the
(LSD)       6.000000          fractional part)
```

- Answer: $.468750_{(10)} = .36_{(8)}$

3-13. *Decimal to hexadecimal.*

- $.296875_{(10)} = ?_{(16)}$

```
          .296875
               16 (Base of new system)
          1781250
          296875
(MSD)    4.750000
               16 (Note: multiply only the
          4500000          fractional part)
          750000
(LSD)   12.000000
```

- Answer: $.296875_{(10)} = .4C_{(16)}$

  (Note: 12 in hex equals C)

3-14. Knowing how to use place-value (discussed in Section 2) to determine the decimal value of a fraction, and knowing how to convert this decimal value to another number system (as we just discussed), enables you to convert the fractional portion of a number from one number system to another. Stated briefly, the rules to follow when converting the fractional portion of a number from one number system to another are:

- If the fraction is in a number system other than decimal, convert the fraction to its decimal fraction equivalent using place-value notation.
- Convert the decimal fraction to the desired number system, using the radix multiplication method.

3-15. Conversion of Number Systems by Relationships. Because there are definite relationships between certain number systems, conversion from one system to another is possible by an inspection method. Let's look at some examples.

3-16. *Binary to octal.* The binary number is simply broken into groups of three and read as an octal digit. This is possible since three binary place-positions can represent digits 0 through 7, and these are all the digits used in the octal system. To break a binary number into groups of three, start at the binary point and work in both directions. If at either end of the number (that is, left or right of the binary point) there are less than three binary digits, assume zeros to form a group of three:

- $10110001111010.10110_{(2)} = ?_{(8)}$

  $\dfrac{010}{2}\ \dfrac{110}{6}\ \dfrac{001}{1}\ \dfrac{111}{7}\ \dfrac{010.}{2.}\ \dfrac{101}{5}\ \dfrac{100_{(2)}}{4_{(8)}}$

- By inspection, $10110001111010.10110_{(2)} = 26172.54_{(8)}$

3-17. *Octal to binary.* Each octal digit is written as a group of three binary digits since the digits of the octal system range from 0 through 7.

- $562.7_{(8)} = ?_{(2)}$

  $\dfrac{5}{101}\ \dfrac{6}{110}\ \dfrac{2}{010.}\ \ \dfrac{7_{(8)}}{111_{(2)}}$

- By inspection, $562.7_{(8)} = 101110010.111_{(2)}$

3-18. *Hexadecimal to BCD.* Each hex digit is written as a group of four binary digits (recall that this grouping is BCD). This is possible since four binary place-positions can represent numbers 0 through 15, and these are all the numbers used in the hex system; that is, digits 0 through 9 and letters A (10) through F (15):

- $31A4_{(16)} = ?_{(BCD)}$

  $\dfrac{3}{0011}\ \dfrac{1}{0001}\ \dfrac{A}{1010}\ \dfrac{4_{(16)}}{0100_{(BCD)}}$

- By inspection, $31A4_{(16)} = 0011\ 0001\ 1010\ 0100_{(BCD)}$

4. Binary Arithmetic

4-1. Since the majority of computers use the binary system in performing arithmetic operations, a review of binary addition, subtraction, multiplication, and division is presented in this section. The examples presented are referred to as direct binary arithmetic, and they are typical of the binary arithmetic operations that are performed with pencil and paper. Some of our examples presented in this section are similar to actual computer arithmetic operations. Also, examples of the recommended pencil-and-paper method of performing binary arithmetic are presented—that is, convert the binary number (especially large numbers) to their decimal equivalent and perform the indicated operation. When you have your answer, convert it back to binary. Our recommended method is presented as a check of the direct method in our examples.

4-2. **Addition.** The direct addition of binary numbers follows the rules for binary addition that follow:

0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0 with a 1 carry to the next higher place position.

4-3. Here is a binary addition problem:

- Add $1101_{(2)}$ to $110_{(2)}$
- Check:

$$\begin{array}{rcl} 1101 & = & 13_{(10)} \\ \underline{+110} & = & \underline{6}_{(10)} \\ 10011 & = & 19 \end{array}$$

- Result: In the first column (LSD), 1 + 0 = 1. In the second column, 0 + 1 = 1. In the third column, 1 + 1 = 0 with a 1 carry to the next higher column. In the fourth column, 1 + 0 + the carried 1 = 0 with a 1 carry to the next column; this 1 must be carried to an additional or fifth position (the MSD) in the answer.

4-4. **Subtraction.** There are several direct methods for binary subtraction. We'll present two of them here. The first is similar to decimal subtraction, and the second (complement method) is very similar to the way many computers perform subtraction.

4-5. *Direct subtraction.* This method of binary subtraction is similar to decimal subtraction in that it involves the process of borrowing from a higher order column when required. The following rules are involved in this method of subtraction:

Minuend	*Subtrahend*	*Difference*	*Borrow*
1	1	0	0
1	0	1	0
0	1	1	two 1's from higher order column
0	0	0	0

Example:

$$\begin{array}{rl} 1\ \ \ 1 & \\ 01\ 01 & \\ \cancel{10}11\cancel{0} & \text{Minuend} = 22_{(10)} \\ \underline{-01101} & \text{Subtrahend} = \underline{13}_{(10)} \\ 01001 & \text{Difference} = 9 \end{array}$$

NOTE: This problem necessitated borrowing in two instances. In both cases, the borrow was obtained from the adjacent higher order column. A direct subtraction may require a borrow from a higher order which is not adjacent. For example:

$$\begin{array}{rcrcr} & & 1 & & 1 \\ 100 & = & 010 & = & 011 \\ \underline{-\ 1} & & \underline{-\ 1} & & \underline{-\ 1} \\ & & & & 011 \end{array}$$

4-6. *Complement method of subtraction.* Many computers perform binary subtraction using a method very similar to this complement method. This method involves complementing the subtrahend and performing binary addition of the minuend and subtrahend. The final answer will depend on whether or not a carry occurs in the MSD position. First, we'll look at the rules for this method; then, two examples are presented.

- Complement the subtrahend and perform binary addition. (Note: Before complementing, insure that there are the same number of place-positions in the subtrahend and minuend by adding an appropriate number of zeros.
- The answer will be positive if a 1 carry occurs in the MSD position. This carry must be added to the LSD position of the answer to derive the correct positive answer.
- The answer will be negative if no carry occurs in the MSD position. In this case, the answer and its sign must be complemented to derive the correct negative answer.

4-7. Binary subtraction problem #1:

- Subtract $10_{(2)}$ from $1001_{(2)}$

$$\begin{array}{rl} 1001 & \\ \underline{+1101} & \text{(complement the subtrahend and add)} \\ \underline{+1} & \text{(carry of 1 from MSD column)} \\ 111 & \text{(answer is positive 7)} \end{array}$$

- **Check:**

1001 = $9_{(10)}$
-10 = $\underline{-2}_{(10)}$
7 (check answer is positive 7)

- **Result:** Since there was a carry from the MSD column, the answer is positive. The 1 carry is added to the LSD position of the answer to derive the correct positive answer.

4-8. Binary subtraction problem #2:

- Subtract $1010_{(2)}$ from $111_{(2)}$

0111
$\underline{+0101}$ (complement the subtrahend and add)
1100 (Note: no carry from MSD; answer and sign must be complemented)
-0011 (answer and sign complemented = -3)

- Check:

111 = $7_{(10)}$
-1010 = $-\underline{10}_{(10)}$
-3 (check answer is negative 3)

- Result: Since a carry did not occur from the MSD column, the answer and its sign must be complemented to derive the correct negative answer.

4-9. **Multiplication.** A computer normally performs multiplication through a process of adding and shifting. Depending on the values of the numbers to be multiplied, computer multiplication is a long, involved process. The direct method presented here is much shorter than the computer method, and it involves the following rules:

1 × 1 = 1
1 × 0 = 0
0 × 1 = 0
0 × 0 = 0

4-10. Direct multiplication problem:

- $1101_{(2)} \times 0011_{(2)}$

1101 = $13_{(10)}$
$\underline{\times\ 11}$ = $\underline{3}$
1101
$\underline{1101}$
100111 = $39_{(10)}$

- Result: Note the numbers are lined up exactly as in decimal multiplication, and the addition steps were accomplished using the rules for binary addition.

4-11. **Division.** The process of division is the most time-consuming of the four arithmetic operations performed in a computer. In the direct method of binary division presented here, the numbers are set up as in decimal division, and the rules of binary multiplication, subtraction, and addition are applied.

4-12. Direct division problem:

- $1111_{(2)}$ divided by $10_{(2)}$

$\underline{0111}$
10/1111
10 (1 × 10)
$\underline{01}$ (complement subtrahend)
100 (add)
$\underline{1}$ (carry)
11 (add and bring down 1)
10 (1 × 10)
$\underline{01}$ (complement subtrahend)
100 (add)
$\underline{1}$ (carry)
11 (add and bring down 1)
10 (1 × 10)
$\underline{01}$ (complement subtrahend)
100 (add)
$\underline{1}$ (carry)
1 (remainder)

- Check:

$1111_{(2)} = 15_{(10)}$
$10_{(2)} = 2_{(10)}$
15 divided by 2 = 7 with a remainder of 1. And, $7_{(10)}$ is equal to $111_{(2)}$.

- Result: Note that all the rules discussed in this section for the direct method of binary addition, subtraction, and multiplication were employed in our direct division problem.

Computer Circuits

THE BUILDING blocks of a digital computer system are its individual circuits. Hundreds, often thousands of them, are interconnected to accomplish the operation of transferring and processing data. Actually, only a few different types of basic circuits are used, but they are used over again and again in different combinations. This has the advantage of simplifying the design of the computer, increasing its reliability by using only a few well-tested circuits, and making maintenance simpler and faster.

2. The circuits used in digital computers are categorized as logic and nonlogic. Logic circuits enable the computer to make decisions, to manipulate data, and to store data. Nonlogic circuits perform functions such as supplying the necessary AC and DC voltages, shaping pulses, coupling logic circuits to indicators, converting data from and to analog values, and operating electromechanical devices. It would be impractical to describe every circuit now in use; however, this chapter reviews many basic circuits from the standpoint of electronic principles, symbology, and Boolean equations. An in-depth discussion of Boolean techniques is included to emphasize its usefulness for analyzing and troubleshooting complex logic circuitry.

1. Waveshaping and Referencing Circuits

1-1. These circuits are important in computers for several reasons. First, timing and data signals must adhere to the waveshape and voltage requirements specified by the designer. Second, these circuits may require adjustment by a repairman to keep computer signals in tolerance. Such circuits include differentiators, integrators, limiters, and clampers. Waveshaping and referencing circuits usually appear as an integral part of other circuits such as flip-flops (F/Fs) or amplifiers. Therefore, it is important that you be able to recognize these circuits and determine when one of them is the cause of a malfunction.

1-2. **Differentiators.** Differentiating circuits produce an output voltage that is proportional to the rate of change of the input. Note that in the RC differentiator illustrated in figure 2-1, an output voltage occurs only when the square wave rises or falls. An RC differentiator requires a short-time constant (1/10 the input frequency) with the output taken across the resistor. At T_0, the input changes rapidly from one steady state to another; that is, the rate of change is maximum and the output voltage is maximum. From T_0 to T_1, there is zero rate of change and the output drops to zero at T_1. How fast the output drops to zero depends on the RC time constant of the circuit which determines the charge rate of the capacitor. At T_1, there is another sudden change of input voltage in the opposite direction with a maximum rate of change, and the output voltage is again maximum but in the opposite direction. The sharpness of the output spike depends on the shortness of the

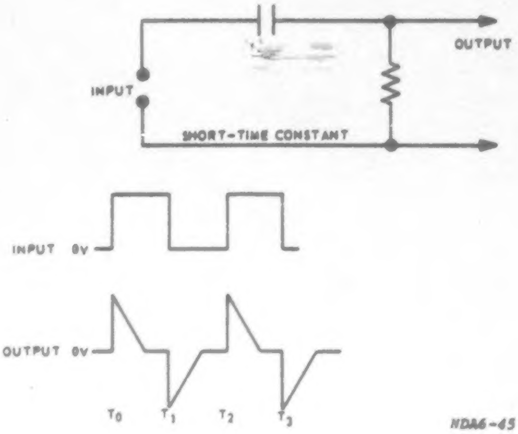


Figure 2-1. RC differentiator.

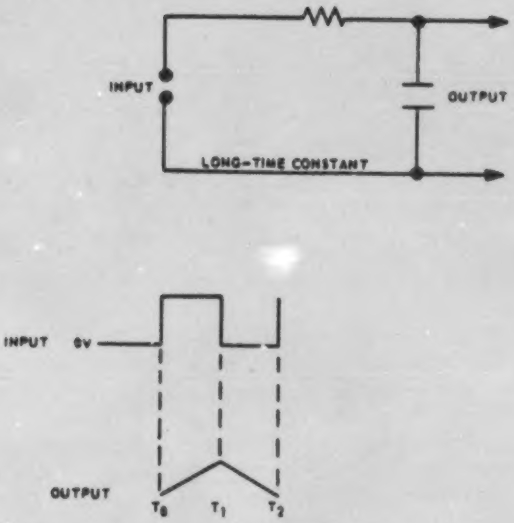


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Figure 2-2. RC integrator.

RC time constant. Differentiators, such as described here, are used as part of the input circuitry of F/Fs where a sharp spike is needed to trigger the circuit.

1-3. **Integrators.** Recall that integration is the process of summing up an infinite number of minute quantities. An integrating circuit produces an output voltage that is essentially the time integral of its input waveform. In an RC integrator circuit, a long-time constant (10 times the input frequency) is used, and the output voltage is taken across the capacitor. Refer to figure 2-2 for this discussion of an integrator circuit. At time T_0, the area under the square-wave input is zero. As time progresses from T_0 to T_1, the same amount of area is added with each increment of time. The output increases in a linear fashion, and it reaches a maximum at time T_1. The input voltage during the time integral from T_1 to T_2 is negative, and the output decreases linearly toward zero volts.

1-4. An integrating circuit can be used as an input to a Schmitt trigger circuit where a predetermined threshold voltage must be reached before the circuit fires (or conducts). This threshold voltage could be a function of an integrator circuit that is receiving valid radar returns or tape drive sync pulse inputs.

1-5. We should note here that RC coupling circuits are similar to integrator circuits, and this fact could cause confusion. RC coupling circuits are used primarily to transfer waveforms from one circuit to another so that the output closely resembles the input. Like the RC integrator, RC coupling circuits use a long-time constant (10 times the input frequency), but the output is taken across a resistor.

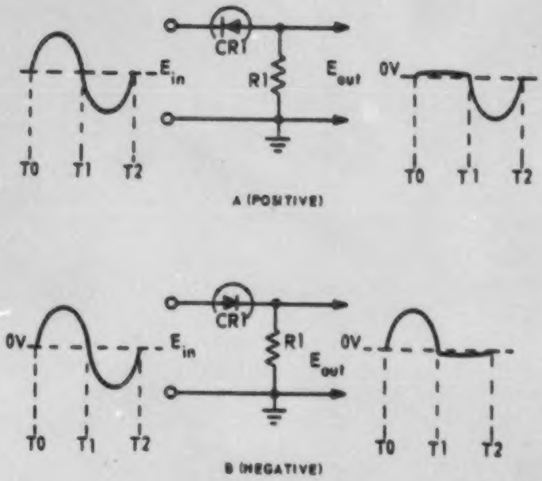

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Figure 2-3. Series limiter.

1-6. **Limiters.** A limiter is defined as a device which prevents some characteristics of a waveform from exceeding a predetermined value. Limiting is used for waveshaping or for circuit protection by preventing a voltage from becoming too large. The two types of limiters discussed here are the series and shunt (parallel).

1-7. *Series limiter.* A limiter can be designed using a diode and a resistor. When the output is in series with the diode, the circuit is called a series limiter. Parts A and B of figure 2-3 are diagrams of a positive and a

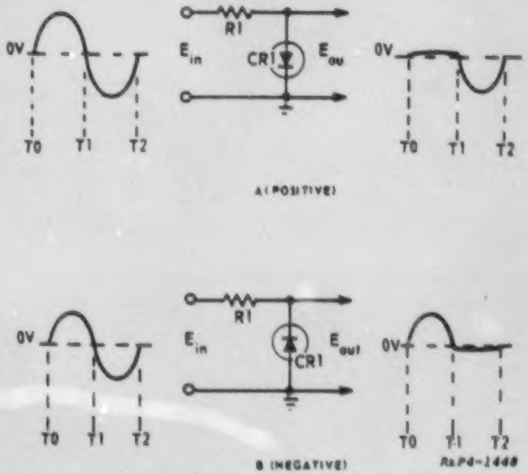

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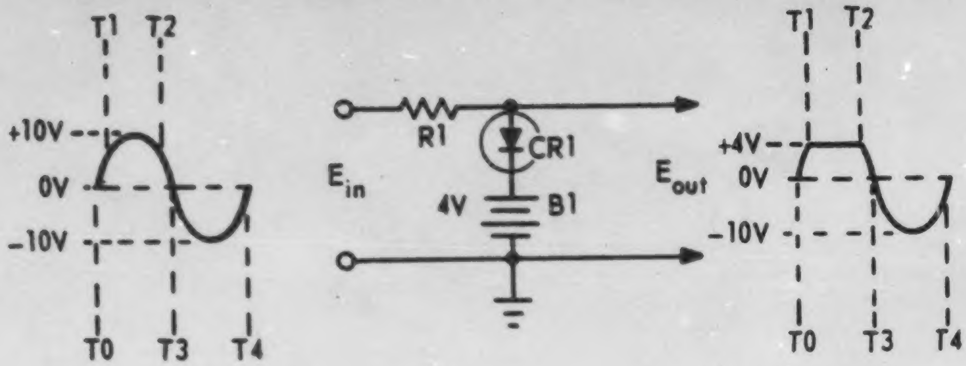
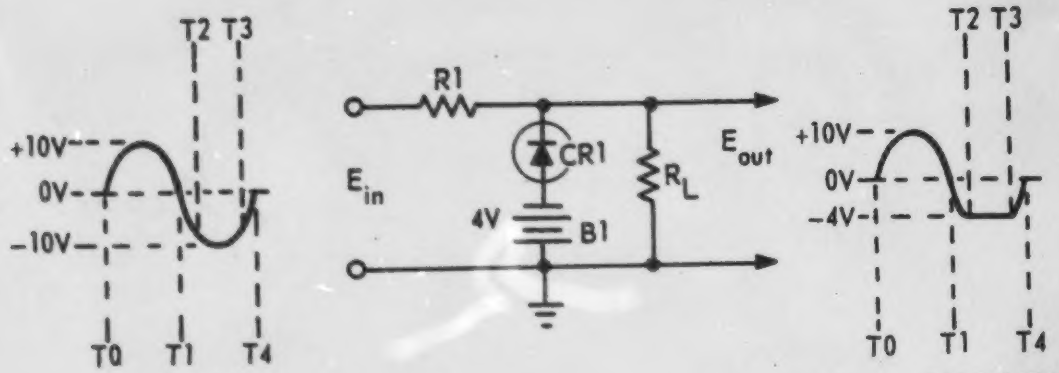
Figure 2-4. Shunt limiter.



A

POSITIVE LIMITER WITH POSITIVE BIAS



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B

NEGATIVE LIMITER WITH NEGATIVE BIAS

Figure 2-5. Shunt limiter, with bias voltage.

negative series limiter. Note that the diode allows conduction in only one direction and blocks or limits the signal in the opposite direction. In part A of the figure, the diode is reverse-biased by the positive alternation of the input; this prevents the positive alternation from being developed at the output. The diode is forward-biased by the negative alternation of the input, and this alternation is developed at the output. In part B, the diode is forward-biased by the positive and reverse-biased by the negative alternation. Therefore, the negative alternation is blocked or limited.

1-8. *Shunt limiter.* When the output is in shunt (parallel) with the limiting device, a shunt limiter is formed. Shunt positive and negative limiters are illustrated in figure 2-4,A and B. The function of the shunt limiter is the same as the series limiter; that is, limit a portion of the input signal. However, note that, in the shunt limiter, limiting occurs during the conduction of the limiting device.

1-9. In the shunt limiters just discussed, limiting occurred near a zero-reference level. This reference level could be controlled by providing a bias voltage for the limiting device. Depending on the value of this bias voltage, limiting may remove only a portion of one alternation of an input sine wave.

Figure 2-5,A, illustrates a positive shunt limiter with positive bias. Note that in this particular circuit, the battery causes the diode to be reverse-biased until the input goes more positive than a +4 volts. Therefore, limiting does not occur until the input reaches this positive bias voltage level from T_1 to T_2. Note that this is the only time that the diode conducts. Now look at the shunt negative limiter with negative bias, illustrated in figure 2-5,B. In this circuit, the battery causes the diode to be reverse-biased until the input goes more negative than - 4 volts. Once the input reaches this level, the diode conducts—causing limiting to occur from T_2 to T_3.

1-10. **Clampers.** There are certain circuit applications within computers which require the upper or lower extremity of a waveform to be fixed at a specified value. This function is accomplished with a clamping circuit which effectively clamps or ties the upper or lower extremity of a waveform to a fixed DC potential.

1-11. *Positive clamper.* Figure 2-6,A, illustrates a positive clamper. The identifying feature to note here is that *the diode's cathode is connected to the capacitor.* At T_0, the - 25-volt input causes CR1 to conduct and C charges to 25 volts. At T_1, the 25 volts across C and the +25-volt input are series-aiding. Thus, +50 volts appears across R and CR1. At this time, CR1 is reverse-biased. From T_1 to T_2, C discharges to approximately 23 volts (determined by the value of R and C), and the output (part B of the figure) drops from 50 to 48 volts. At T_2, the input is - 25 volts, CR1 conducts, and the output goes to approximately - 2 volts. From T_2 to T_3, C charges quickly through CR1, from 23 volts to 25 volts, and the output goes from - 2 to 0 volts. Note that the peak-to-peak value of the output is the same as the input (50 volts), but its lower extremity is clamped to zero volts.

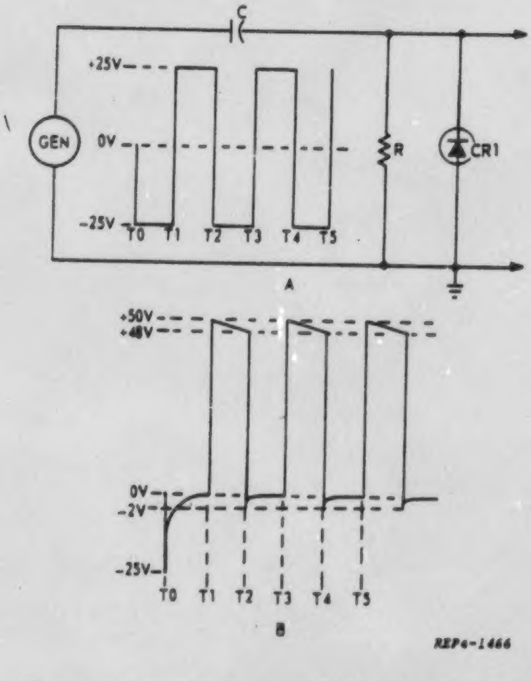

Figure 2-6. Positive clamper circuit and waveforms.

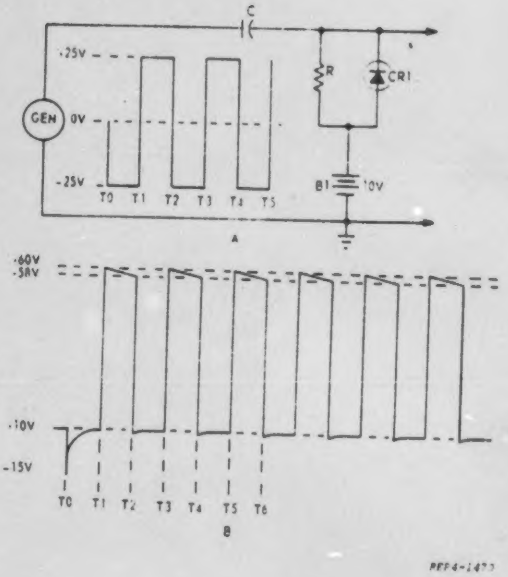

Figure 2-7. Positive clamper with positive bias (10V).

1-12. *Negative clamper.* The identifying feature of this type of clamper is that *the diode's anode is connected to the capacitor.* If the clamper in figure 2-6 were a negative clamper, the diode would be turned around (anode connected to capacitor), and the output would vary between 0 and - 50 volts.

1-13. *Establishing the clamping reference.* Some circuit applications require a signal clamped to a voltage other than ground. If we add a +10-volt bias battery between the signal return line and the resistor and diode, as shown in figure 2-7, we would change the clamping reference from 0 to +10 volts. In the positive clamper shown, the minimum value of the signal is clamped to the +10-volt bias voltage. In a negative clamper, the maximum value of the signal would be clamped to this bias voltage.

1-14. *Determining the output of a clamper.* In troubleshooting a clamper circuit, you must know how to determine its output for a given input; otherwise, you will not know whether the output is correct. The following steps are a guide for determining a clamper's output.

- Determine whether it is a positive or negative clamper from the position of the diode in the circuit.
- Draw the clamping reference level which is ground or a bias voltage.
- Draw the input waveshape exactly as it is with respect to shape and peak-to-peak amplitude; however, the lower extremity should be drawn on the clamping reference level for a positive clamper or the upper extremity drawn on the clamping reference level for a negative clamper.

Figure 2-8 illustrates the use of these three steps for a square wave and a sawtooth. Note in part A of the figure that the peak-to-peak amplitude of these waveshapes is 250 volts (-50 to +200 volts). B and C of the figure illustrate positive clamping, because the lower extremity is clamped to the reference level. D and E illustrate negative clamping, because the upper extremity is clamped. This figure also shows that clamping does not change the amplitude of the signal to any great extent.

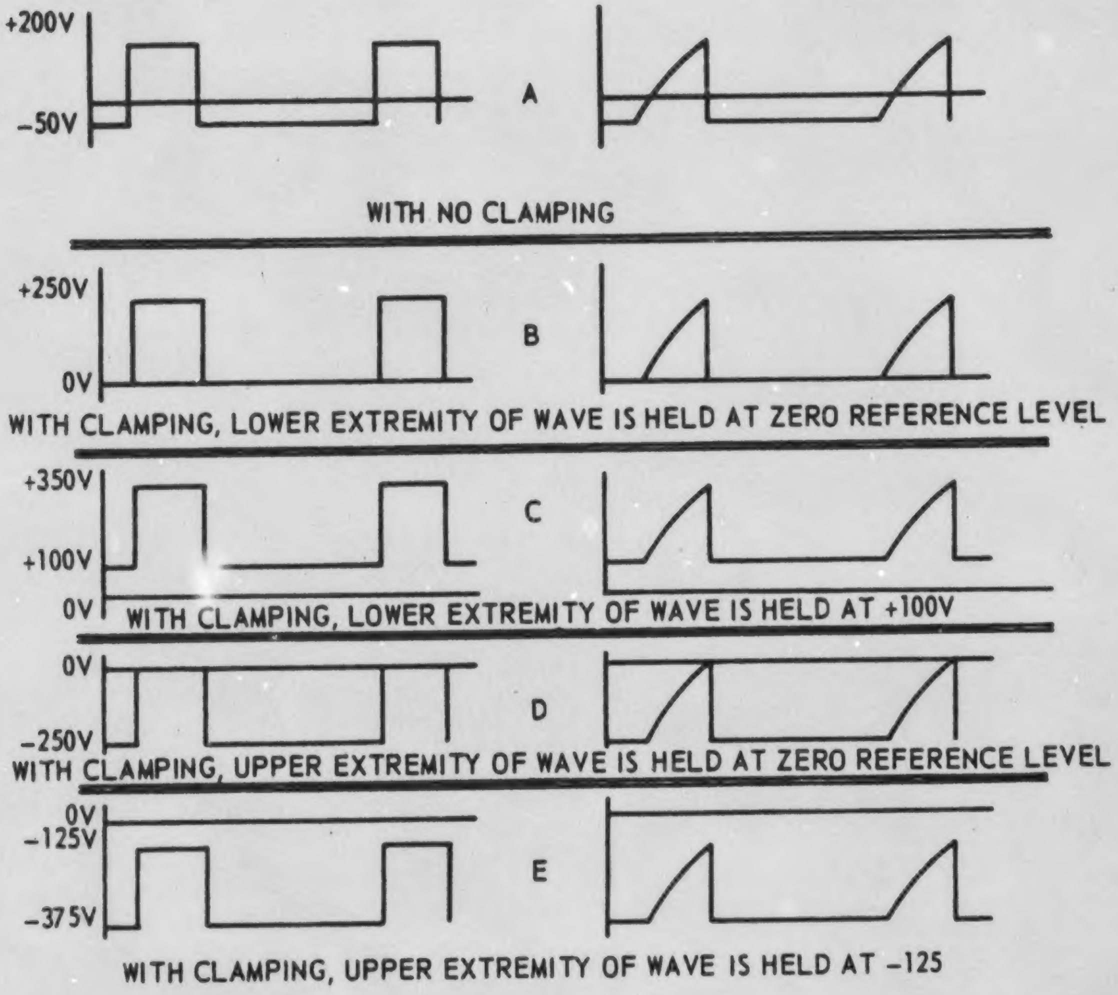
+200V
-50V
A
WITH NO CLAMPING
+250V
0V
B
WITH CLAMPING, LOWER EXTREMITY OF WAVE IS HELD AT ZERO REFERENCE LEVEL
+350V
+100V
0V
C
WITH CLAMPING, LOWER EXTREMITY OF WAVE IS HELD AT +100V
0V
-250V
D
WITH CLAMPING, UPPER EXTREMITY OF WAVE IS HELD AT ZERO REFERENCE LEVEL
0V
-125V
-375V
E
WITH CLAMPING, UPPER EXTREMITY OF WAVE IS HELD AT -125

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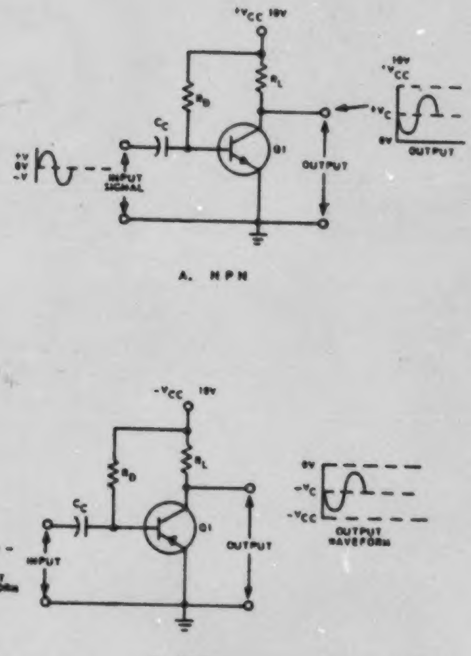
Figure 2-8. Clamping waveforms.



A. NPN

B. PNP

NDA6-76

Figure 2-9. Common-emitter circuit.

1-15. So far in our review of computer circuits, we have discussed basic waveshaping and referencing circuits. Computer signals and levels also need to be amplified as well as shaped and referenced. The circuit that performs this function is called an *amplifier.*

2. Basic Amplifier Circuits

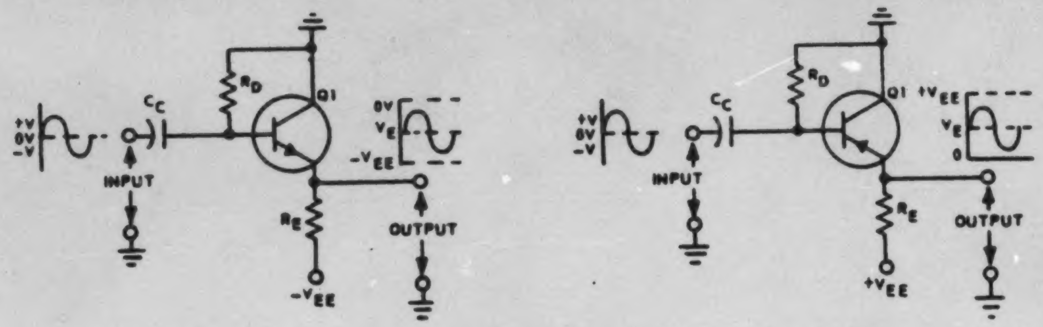
2-1. Recall that an amplifier is a circuit whose output is an enlarged reproduction of its input. The three basic amplifier circuits you should have a good working knowledge of are the common emitter (CE), common base (CB), and common collector (CC). The common (or grounded) element in these circuits is that which is common to both the input and output circuitry.

2-2. Common Emitter (CE). This amplifier circuit is shown in figure 2-9. Note in part A that the input is applied between the base and emitter of the NPN transistor and that the output is taken between the collector and emitter. The emitter is therefore common to both the input and output circuitry; hence, the name common emitter or grounded emitter. Resistor R_L is called the collector load resistor. It allows the voltage on the collector (V_C) to swing between V_{CC} and ground as the transistor decreases and increases conduction with an input signal applied. This change in voltage on the collector contributes to the amplification factor of the circuit. Resistor R_D (divider) provides the necessary forward bias for the base-emitter junction of the transistor. Forward-bias current (I_B, base current) flows from ground, through the emitter, out the base lead, and through R_D to V_{CC}. I_B is a few hundred microamperes, and the DC voltage on the transistor's base is a few tenths of a volt. The coupling capacitor (C_C) used in the input line passes the AC component of the input signal and blocks its DC component. This prevents the DC in the circuitry to the left of C_C from affecting the bias on the transistor. C_C also blocks the bias voltage from the input signal source. This blocking action allows the input signal to act like an AC generator connected to an RC circuit.

2-3. The input signal to our circuit is a sine wave that varies a few millivolts above and below zero. With the positive alternation of this signal, the forward bias across the base-emitter junction of the transistor starts to increase. This, in turn, causes the transistor's junction resistance to decrease. As the input signal continues to go positive, the transistor's conduction increases with a corresponding increase in emitter (I_E) and collector (I_C) current, but only a very small increase in I_B. Note in figure 2-9,A, that the output goes toward ground as the input goes positive. This is due to more voltage dropping across R_L as I_C increases. Since the voltage across R_L and the voltage dropped across the transistor must add up to V_{CC}, an increase in the voltage dropped across R_L results in an equal *decrease* in the voltage dropped across the transistor. Consequently, the output voltage is a negative-going alternation. In short, the positive-going alternation of the input was amplified, but a phase inversion took place through this CE amplifier.

2-4. During the negative alternation of the input signal, the forward bias on the transistor decreases, causing the transistor's junction resistance to increase. This, in turn, causes the current through the transistor to decrease. The voltage across R_L makes a corresponding decrease, which results in an increase voltage drop across the transistor. This action is reflected in the output by a positive-going alternation.

2-5. A PNP transistor version of the common-emitter circuit is shown in figure 2-9,B. The primary difference between the NPN and PNP configurations is the polarity of V_{CC}. With a negative V_{CC}, the base voltage (forward bias) is negative with respect to ground. Forward-bias current flows from V_{CC}, through R_D, through the base-emitter



A. NPN

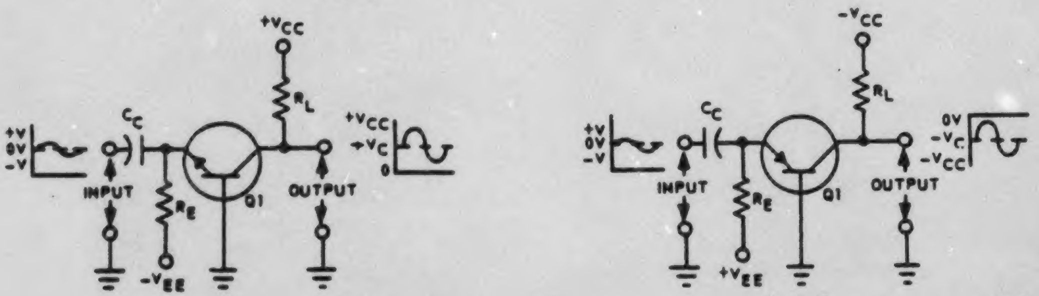
B. PNP

NDA6-78

Figure 2-10. Common-collector configuration.

junction of the PNP transistor, then to ground. On the positive alternation of the input signal, this negative forward-bias voltage goes positive, which reduces the current flow through the transistor. As I_C decreases, the voltage drop across the load resistor (R_L) decreases, causing the voltage drop across the transistor to increase. Since V_{CC} is negative, the voltage on the collector (output voltage) goes in a negative direction toward V_{CC}. The negative alternation of the input signal causes the current flow through the transistor to increase. As I_C increases, the voltage drop across R_L increases, which results in the voltage drop across the transistor to decrease (goes in a positive direction). The overall effect is amplification of the input signal with phase inversion at the output.

2-6. Common Collector (CC). Another name for this circuit is *emitter follower*. The circuit is illustrated in figure 2-10. Note in part A that the input signal is applied between the base and collector of the NPN transistor and that the output is developed between the emitter and the grounded collector. The collector is therefore common to both the input and output circuitry; hence, the name common collector (or grounded collector). Forward-bias current for the NPN transistor circuit flows from $-V_{EE}$, through R_E, through the emitter-base junction, and through R_D to ground. Recall that the emitter resistor (R_E) is sometimes called a swamping resistor, because it also functions to swamp (overcome) the effects of temperature on the emitter-base junction of a transistor. Forward-bias current for the PNP transistor circuit (fig. 2-10,B) flows from ground through R_D, through the base-emitter junction, and through R_E to $+V_{EE}$. The base current, or forward-bias current, increases with the application of the positive alternation of the input signal to the NPN transistor. This also causes an increase in I_E, which results in an increase in the voltage dropped across the emitter resistor R_E. The end result is reflected in the output as it goes in a positive (less negative) direction. On the negative alternation of the input signal, base



A. NPN

B. PNP

NDA6-75

Figure 2-11. Common-base configuration.

TABLE 2-1
GENERAL CHARACTERISTICS OF TRANSISTOR AMPLIFIER CIRCUITS

CIRCUIT CONFIGURATION	Power Gain	Input Resistance	Current Gain	Output Resistance	Voltage Gain	Similar to Vacuum Tube Circuit
COMMON EMITTER Input signal to the base: Output signal from the collector	Highest 25-40 db	Low 500-1500 ohms	Large 25-50	High 30K-50K	Large 300-1000	Grounded cathode amplifier
COMMON COLLECTOR Input signal to the base: Output signal from the emitter	Lowest 10-20 db	High 20K-500K	Large 25-50	Low 50 ohms-1K	Less than 1	Generally like a cathode follower
COMMON BASE Input signal to the emitter: Output signal from the collector	Medium 20-30 db	Very Low 30-150 ohms	Less than 1	Very high 300K-500K	Large 500-1500	Grounded grid amplifier

NDA6-35

current decreases—causing a decrease in I_E and a smaller voltage drop across R_E. The end result is reflected in the output as it goes in a negative direction. Note that the input and output are in phase.

2-7. The positive alternation of the input signal causes base current to decrease when it is applied to the base of the PNP circuit in figure 2-10,B. This results in a decrease in I_E, with a decrease in the voltage dropped across R_E. Therefore, the output voltage goes in a positive direction. Base current increases as the negative alternation of the input signal is applied to the base of the transistor. This results in an increase in I_E, with an increase in the voltage dropped across R_E. Therefore, the output voltage goes in a negative direction. Note that the input and output of both circuits are in phase.

2-8. **Common Base (CB).** In the common base (or grounded base) transistor amplifier circuit, the base element is common to the input and output circuitry. Circuit arrangements for NPN and PNP transistors are shown in figure 2-11,A and B. Forward bias for the emitter-base junctions is provided by V_{EE} and resistor R_E. When the positive alternation of the input signal is applied to the emitter of the NPN transistor, I_E decreases. This decrease in I_E causes a decrease in I_C, which causes a decrease in the voltage dropped across R_L. Therefore, the output goes in a positive direction. The negative alternation of the input causes an increase in I_E. This increase in I_E causes an increase in I_C, which causes an increase in the voltage dropped across R_L. Therefore, the output goes in a negative direction (less positive).

2-9. In the PNP CB amplifier circuit (fig. 2-11,B), the positive alternation of the input signal causes I_E and I_C to increase. The increase in I_C causes the voltage drop across R_L to increase, which causes the output voltage to go in a positive direction (less negative). On the negative alternation of the input, I_E and I_C decrease and the output voltage goes in a negative direction (more negative). The overall output signal taken from the collector is an amplified reproduction of the input signal. Note that the input and output signals are in phase.

2-10. **Comparison of Amplifier Circuits.** Refer to table 2-1 for a simplified comparison of the characteristics associated with the CE, CC, and CB transistor amplifier circuits. Note from this table that the CC amplifier has a voltage gain less than 1, but its current gain is relatively high; whereas the CB amplifier has a current gain less than 1, but its voltage gain is high. In contrast, note that the CE amplifier's current and voltage gain are both high. However, we know from our study of this circuit that it is characterized by a phase inversion between the input and output signal.

3. Oscillator Circuits

3-1. An oscillator is an electronic device which generates AC power at a frequency determined by the values of certain constants in the circuit. An oscillator may be considered an amplifier with regenerative feedback and circuit parameters that restrict the oscillations of the device to a single frequency. Some of the uses of oscillator circuits in computer systems include clock pulse generation, timing generation, and signal generation. It is imperative that the oscillators used within a computer system provide an output consisting of the constant amplitude and frequency for which it was designed. The oscillators presented in this section are typical of those used in computer systems.

3-2. Functional Parts of an Oscillator. The basic requirements for oscillations within an oscillator circuit are:

- A frequency-determining device (FDD).
- Amplification.
- Regenerative feedback.

3-3. *Frequency-determining device.* As the name implies, the FDD determines the frequency at which the oscillator circuit operates. Some common FDDs used are inductance capacitance (LC) tank circuits, crystals, and resistance capacitance (RC) networks.

3-4. *Amplification.* The amplifier used within an oscillator must be capable of providing enough gain in the output to maintain constant amplitude and frequency and to provide regenerative feedback.

3-5. *Regenerative feedback.* To sustain oscillations in the amplifier stage of an oscillator circuit, the output circuit must be coupled to the input circuit in such a way that part of the output energy is returned to the input. This energy (feedback) is amplified, and when it is increased beyond a certain critical point, sustained oscillations result. For oscillations to occur within transistor oscillator circuits, two conditions must be satisfied. First, there must be feedback (regenerative) from the output to the input in such a way as to aid, or reinforce, the transistor's forward bias. Recall that degenerative feedback in a transistor circuit opposes the forward bias. Second, it is necessary that the regenerative feedback be of sufficient amplitude to transfer enough power back to the input circuit so as to overcome any losses in the FDD. Feedback may be accomplished by inductive, capacitive, or resistive coupling.

3-6. Inductance-Capacitance (LC) Oscillators. The FDD in this type of an oscillator is called an LC tank or LC tuned circuit. The frequency at which the circuit oscillates is determined by the resonant frequency of the LC tuned circuit. The approximate frequency (F) of oscillations may be determined by the relation:

$$F = \frac{0.159}{\sqrt{LC}}$$

By simple mathematical analysis, decreasing any factor in the denominator (other factors remaining constant) increases the value of the fraction. Conversely, increasing any factor in the denominator (other factors remaining constant) decreases the value of the fraction. Thus, in the formula above, decreasing either L or C causes an increase in the frequency of oscillations. Increasing either L or C causes a decrease in the frequency of oscillations. For example, to determine the frequency of oscillations in an LC tuned oscillator where L = 16 microhenries and C = 100 picofarads, you must first convert to the proper units for the formula:

$16\ \mu h = 16 \times 10^{-6}$ henries
$100\ pf = 100 \times 10^{-12}$ farads

then:

$$\begin{aligned} F &= \frac{0.159}{\sqrt{LC}} \\ &= \frac{0.159}{\sqrt{16 \times 100 \times 10^{-12} \times 10^{-6}}} \\ &= \frac{0.159}{\sqrt{1600 \times 10^{-18}}} \\ &= \frac{0.159}{40} \times 10^{9} \\ &= 3.98 \text{ MHz} \end{aligned}$$

Now that we have reviewed the requirements for oscillations within this particular type of circuit, let's take a look at a few specific LC oscillator circuits.

3-7. *Armstrong oscillator.* A transistorized version of this type of oscillator is illustrated in figure 2-12. The circuit is comprised of an NPN common-emitter amplifier with R2 providing the forward bias for Q1. The secondary L2 (sometimes called the tickler coil) of T1, and C1, make up the FDD. Adjustment of C1 determines the frequency

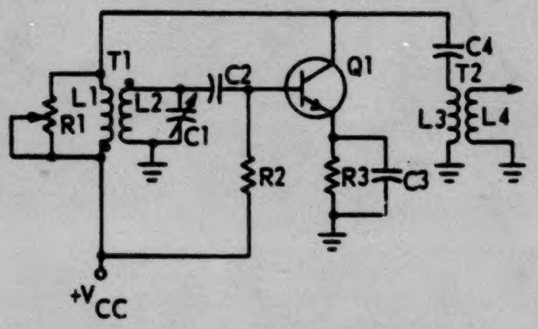


Figure 2-12. Armstrong oscillator.

of oscillations. Note that the FDD is in the base circuit; therefore, this particular circuit could be referred to as a tuned base Armstrong oscillator. R3 is the swamping resistor that provides temperature stability for Q1, and C3 is a bypass capacitor for R3 to prevent amplifier degeneration. C4 is a coupling capacitor, and T2 provides a method of coupling the output signal. The primary (L1) and R1 determines the amount of regenerative feedback to the base of Q1. This amount is controlled by adjusting R1 which, in turn, controls the amount of current through L1. With R1 adjusted for maximum resistance, most of the current flows through L1 and a larger amount of feedback is coupled back to the base of Q1.

3-8. Circuit operation is as follows: When V_{CC} is applied to the circuit, a small amount of base current (I_B) flows through R2 which sets the forward bias for Q1. With Q1 forward biased, collector current (I_C) flows from ground through Q1, splits through R1 and L1, and terminates at $+V_{CC}$. The current through L1 develops a magnetic field which induces a voltage into the tank circuit. This induced voltage is + at the top of L2 and C1. At this time, two actions occur. First, tank capacitor C1 charges to this positive voltage, which means the tank circuit now has stored energy. Second, C2 couples this positive voltage to the base of Q1, causing it to conduct more. With an increase in the conduction of Q1, more current flows through L1, a larger voltage is induced into L2, and a larger positive signal is coupled to the base of Q1. While all this is taking place, the FDD is storing more energy because C1 is charging to the voltage induced into L2. Q1 continues to increase in conduction until it reaches saturation. At saturation, I_C is at its maximum and cannot increase further. This means the current through L1 is steady, L1's magnetic field is not moving, and no voltage is being induced into L2. Without voltage being induced into L2, C1 now acts as the voltage source for the tank by discharging through L2. As C1 discharges, it transfers its energy into the magnetic field of L2. As C1 continues to discharge, its voltage decreases. The discharge of C1 also has an effect on coupling capacitor C2.

3-9. Coupling capacitor C2 is charged to approximately the same voltage as C1; therefore, as C1 discharges, C2 also discharges. C2's prime discharge path is through R2. As C2 discharges, the voltage drop across R2 reduces the forward bias on Q1 (base becomes less positive). This decrease of forward bias causes a decrease in I_C. A decrease in I_C allows the magnetic field of L1 to collapse. This collapsing field induces a negative voltage into L2 which is coupled through C2 to the base of Q1. In other words, the base of Q1 feels a negative voltage which causes the forward bias to decrease further. This action continues until Q1 is driven to cutoff. While Q1 is cut off, the tank circuit continues to flywheel (oscillate). This flywheel effect not only produces a sine wave, which is induced back into L1 and coupled through C4 to the primary (L3) of output transformer T2, but it also aids in keeping Q1 cut off. Without feedback, the oscillations of the tank would dampen out after several cycles. To insure that the amplitude of the signal remains constant, regenerative feedback is supplied to the tank once each cycle as explained below.

3-10. As the voltage across C1 reaches a maximum negative, C1 begins discharging toward zero volts. It continues to discharge through zero and becomes charged positively. As this positive is coupled to the base of Q1, it is brought out of cutoff and I_C begins to flow again. This I_C causes a magnetic field in L1 which is coupled into the tank to replace any lost energy caused by tank oscillations. In

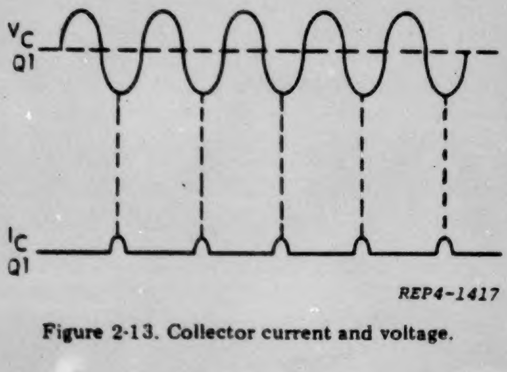


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Figure 2-13. Collector current and voltage.

192

turn, this feedback drives Q1 back into saturation. After saturation is reached, Q1 is again driven into cutoff.

3-11. The waveforms shown in figure 2-13 illustrate the relationship between the collector voltage and collector current. Notice that I_C flows for only a short time during each cycle. And, while the tank circuit is oscillating, L2 of T1 acts as the primary and L1 acts as the secondary. Therefore, the output signal (sine wave) from the tank is coupled through T1, to coupling capacitor C4, and through output transformer T2.

3-12. The operation of the Armstrong oscillator is basically this: Power being applied to the transistor allows energy to be applied to the tank circuit. When the transistor cuts off, the tank circuit oscillates. Once every cycle, the transistor conducts for a short period of time (recall that this is referred to as Class C amplifier operation) and returns enough energy to the tank to insure a constant amplitude sine wave out. The basic operation of other LC tank oscillators is very similar to that of the Armstrong.

3-13. *Colpitts oscillator.* The Colpitts is another type oscillator that uses an LC tank circuit. Refer to figure 2-14 for this discussion. The identifying feature of this oscillator is split capacitors (C3 and C4) in the tank circuit. The regenerative feedback obtained from the tank circuit to sustain oscillations is applied to the emitter of Q1. Base bias is provided by resistors R2 and R3. R4 is the collector load resistor. The emitter resistor, R1, develops the feedback signal and also acts as the emitter swamping resistor. C1 provides an AC bypass around the emitter swamping resistor. C2 provides the required coupling between the collector and the tank circuit. The tuned circuit (FDD) consists of C3 and C4 in parallel with transformer winding L1. A Colpitts may be tuned by varying the inductance of capacitance in the tank circuit. Our example illustrates capacitive tuning. C3 and C4 form a voltage divider network—the voltage developed across C4 being the feedback voltage. Either or both capacitors may be adjusted to control the frequency and amount of feedback voltage. However, for minimum feedback loss, the ratio of the capacitive reactance of C1 and C2 should be approximately equal. To maintain this ratio and thus reduce the possibility of distortion or loss of oscillations, capacitors connected on the same shaft (ganged) are normally used with capacitive tuning.

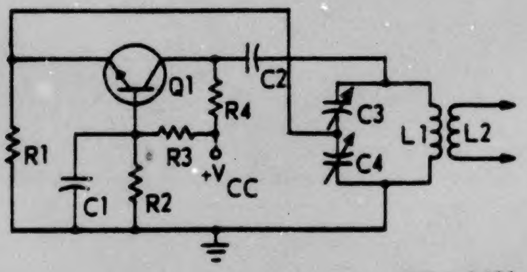
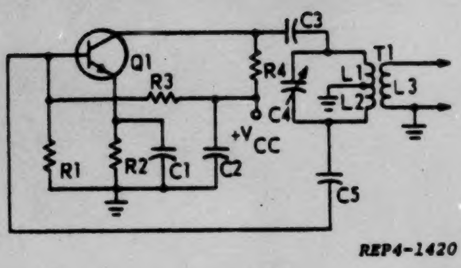
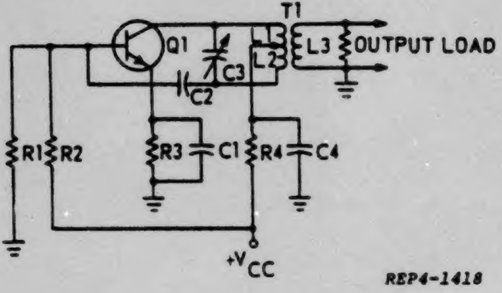


Figure 2-14. Colpitts oscillator.



A. SHUNT-FED



B. SERIES-FED

Figure 2-15. Hartley oscillator.

3-14. *Hartley oscillator.* One of the most common oscillator circuits used within computer systems is the Hartley. This circuit is similar to the Colpitts oscillator except that it uses a split inductance in the tank circuit instead of a split capacitance to obtain feedback. The shunt and series-fed oscillator illustrated in figures 2-15,A and B, is operationally similar except for the method of obtaining collector bias.

a. In the shunt-fed Hartley (fig. 2-15,A), resistors R1, R3, and R4 provide the

202

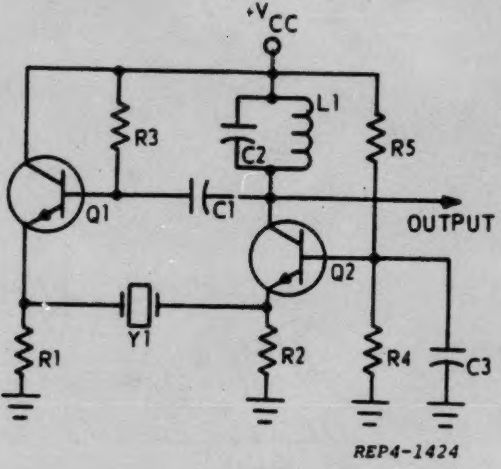


Figure 2-16. Crystal oscillator (Butler type).

necessary bias conditions. Capacitor C1 provides an AC bypass around emitter swamping resistor R2. The FDD network consists of the series combination of transformer windings L1 and L2 in parallel with C4. Since capacitor C4 is variable, the circuit may be tuned through a range of frequencies. C2 is a decoupling capacitor for the power source. T1 windings L1 and L2 function as an autotransformer (identifiable by the single tapped winding) to provide the regenerative feedback signal. The feedback is obtained from the induced voltage in L2 which is coupled through C5 to the base of Q1. By shunt feeding the collector through resistor R4, direct-current flow through transformer T1 is avoided.

b. In the series-fed Hartley (fig. 2-15,B), the oscillator is series-fed because DC flows through the tank. Observe that DC flows from ground, through R3, through Q1 and L1, and then through R4 to +V_{CC}. When a part of the tank circuit is in series with the power supply so that DC flows through it, the circuit is said to be *series-fed.* Regenerative feedback from the collector to the base of Q1 is through autotransformer action between L1 and L2.

3-15. *Crystal-Controlled Oscillators.* In order to obtain a higher degree of frequency stability, crystal oscillators are often used. Recall that when a crystal is subjected to mechanical pressure, it produces a minute voltage and, conversely, when it is subjected to electrical pressure, it tends to vibrate mechanically. This interrelation between the electrical and mechanical properties of a crystal is termed the piezoelectric effect. The quartz is the most commonly used crystal for frequency control of oscillators. Its cost is comparatively cheaper than other crystals, and it expands very little with heat. Quartz crystals used in oscillator circuits must be cut and ground to accurate dimensions in order to function as the FDD. Oscillator circuits that require a very high degree of frequency stability use temperature-controlled ovens to prevent variations in crystal temperature which affects crystal frequency. These ovens are thermostatically controlled containers in which the crystal is placed. There are many oscillator circuits that use crystals, and the one we discuss below is typical of their operation.

3-16. *Butler oscillator.* This oscillator (shown in fig. 2-16) has two primary identifying features: two transistors are used, and a crystal is is connected between the emitters. The purpose of the circuit components is listed below.

R1	- Emitter resistor of Q1, develops the output of Q1.
R2	- Emitter resistor of Q2, develops the input signal to Q2.
Y1	- Frequency-determining device (FDD).
R4 & R5	- Forward bias voltage divider for Q2.
C3	- Base bypass capacitor for Q2.
L1 & C2	- Resonant tank load impedance for collector of Q2.
C1	- Coupling capacitor.
R3	- Forward bias resistor for Q1.

Q1 is a common-collector configuration, and Q2 is a common-base configuration. The regenerative feedback path is as follows: from the collector of Q2, through C1 to the base of Q1, to the emitter of Q1, through the crystal Y1, and back to the emitter of Q2. The regenerative feedback must pass through the crystal. The crystal is operated in its series-resonant mode. At its resonant frequency, the crystal has a very low impedance and passes the feedback signal to the emitter of Q2. All other frequencies are blocked because of the high impedance of the crystal.

3-17. *Circuit operation.* The output signal from this circuit is obtained directly from the collector of Q2. The tank circuit, L1 and C2, flywheels and produces a signal on the collector. At the same time, the crystal is vibrating to produce a signal on the emitter of Q2. With both transistors operated Class C (transistors cutoff for all but a small portion of the input signal), Q2 is cut off for the majority of the time. This condition provides buffer action between the collector circuit of Q2 and the crystal. When the output is taken from the collector, the external load has very little effect on the crystal operation; this eliminates the need for another circuit to provide buffer action. Remember, the FDD is the crystal and NOT L1 and C2. The L1 and C2 resonant frequency should be near that of the crystal. When both transistors are operated Class A (transistor always conducting), L1 and C2 can be replaced by a resistor.

3-18. **Nonsinusoidal Oscillators.** An oscillator circuit in which the output waveform is nonsinusoidal (other than a sine wave) is generally classified as a *relaxation oscillator.* Relaxation oscillators use a regenerative circuit in conjunction with RC or RL components to provide switching action. The charge and discharge times of the reactive elements are used to produce sawtooth, square, or pulse output waveforms. Blocking oscillators, Miller integrators, and multivibrators are examples of relaxation oscillators. They generally use an RC or RL time constant for determination of the output waveform and frequency. Also, these circuits can be further classified as either free-running or driven (triggered). The free-running oscillator is a circuit in which the oscillations begin once power is applied to the circuit. The triggered oscillator is controlled by a synchronizing or triggering external signal.

3-19. **Blocking Oscillator.** This is a special type of circuit which is normally used to produce a narrow pulse, sometimes called a trigger. The output from the blocking oscillator has many uses, most of which are concerned with the timing of various circuits. They are used as frequency dividers, or counter circuits, and for switching other circuits on and off at specific times. Before discussing a specific blocking oscillator circuit, several general considerations which apply to the blocking oscillator need to be discussed first.

3-20. *Pulse considerations.* As you know from your previous training, the timing pulses used within computer circuitry have strict requirements in relation to rise time, fall time, frequency, etc. Therefore, the circuit parameters of blocking oscillators used in computer systems must be such as to provide the required pulses for effective system operation. Figure 2-17 illustrates some of the basic requirements of typical pulses used within computer systems. These requirements include:

- Fast rise time—the leading edge of the pulse should be as steep as possible; that is, the rise time should be short.
- Flat top—this is especially true when the pulse width is relatively long.
- Fast fall time—the trailing edge of the pulse should also be as steep as possible; that is, the fall time should be short.
- Specific and accurately controllable frequency—the pulse occurrence time (PRT) must be stable and accurately controllable because it determines the pulse recurrence frequency (PRF).

3-21. *Circuit parameters.* Recall that circuit parameters, such as resistance, inductance, mutual inductance, or capacitance, directly control the PW (pulse width), PRT, and PRF. In the blocking oscillator we'll be discussing, a transformer is used to determine the duration and shape of the output. Because of its importance, let's

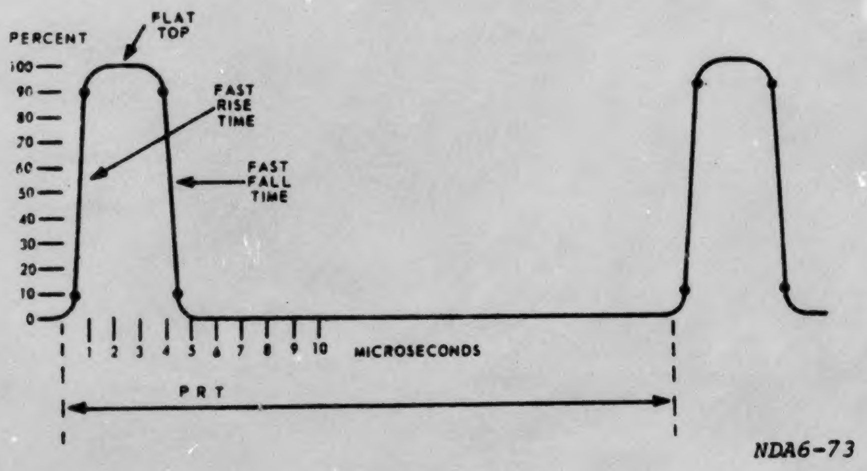


Figure 2-17. Timing pulses.

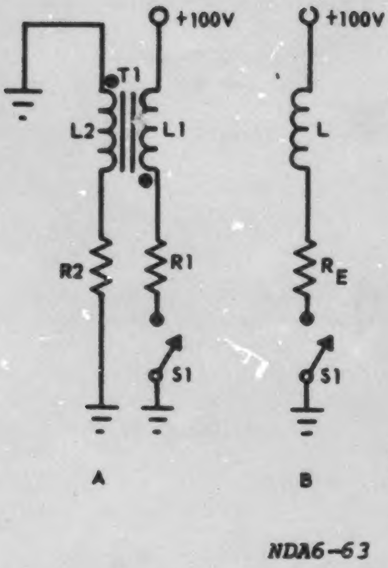


Figure 2-18. RL circuits.

briefly review transformer action when used as part of a series RL (resistance, inductance) circuit.

3-22. *Series RL circuit.* Figure 2-18,A, shows a transformer with series resistance in both the primary and secondary circuits. If S1 is closed, current flows through R1 and L1. As the current increases, it induces a voltage into L2. With induced voltage in L2, a current flows through R2. The voltage across L2 depends on the turns ratio between L1 and L2. The secondary load impedance, R2, affects the primary impedance through reflection from secondary to primary. If the load on the secondary is increased (by decreasing R2), the load on the primary also increases. Similarly, if we decrease R1, primary and secondary currents increase. Since T1 has an effective inductance, and any change in R1 or R2 causes a change in current, we can show T1 as an inductor and R1/R2 as a combined or equivalent series resistance. This equivalent circuit is shown in figure 2-18,B, and it acts as a simple series RL circuit; we'll discuss it in those terms.

3-23. With S1 closed in figure 2-18,B, L acts as an open at the first instant, and the source voltage appears across it. As current begins to flow, E_L decreases and E_R and I increase at an exponential rate. This action is shown by the curves in figure 2-19,A. That is, with S1 closed, circuit current follows curve 1 and E_L follows curve 2. In a time equal to five time constants, the resistor voltage and current are maximum and E_L is effectively zero. The time required for the current to reach maximum depends on the size of L and R_E. If R_E is small, then we have a long-time constant RL circuit. If we use only a small portion of curve 1 (from A to B), then the current rise would have maximum change in a small time period. Further, the smaller the time increment, the more nearly linear is the current rise. A constant current rise through the coil is a key factor in a blocking oscillator. Recall that a basic principle of inductance is that if the rise of current through a coil is linear (that is, the rate of current rise is constant with respect to time), then the induced voltage will be constant. This fact is true in both the primary and secondary of a transformer. Figure 2-19,B, shows the voltage across the coil when the current through it rises at a constant rate. Notice that this is very similar to the typical pulse used within a computer that was shown in figure 2-17.

3-24. *Free-running blocking oscillator.* The circuit illustrated in figure 2-20,A, is a simplified free-running blocking oscillator chosen for this explanation. When power is applied to the circuit, R1 provides forward bias and Q1 conducts. Current flow through Q1 and the primary of T1 induces a voltage in L2. Recall that phasing dots on a transformer indicate a 180° phase shift between L1 and L2. So, as the bottom side of L1 is going negative, the bottom side of L2 is going positive. This positive is coupled to the base of Q1 through C1 which causes Q1 to conduct harder. Thus, we have our regenerative feedback and Q1 saturates. While Q1 is in saturation, the voltage across L1 is a constant value as long as the current rise through it is linear. Figure 2-20,B, shows the ideal collector and base waveforms. At T1, L1 saturates. At this time, there is no change in the magnetic flux coupled from L1 to L2. This results in C1 (which charged from T_0 to T_1) to discharge through R1. This places a negative voltage on the base of Q1 which cuts it off. I_C now stops and the voltage across L1 returns to zero. The

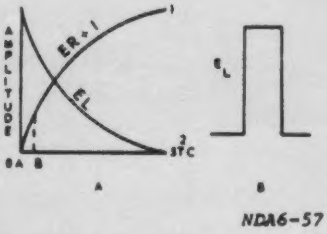


Figure 2-19. Voltage across a coil.

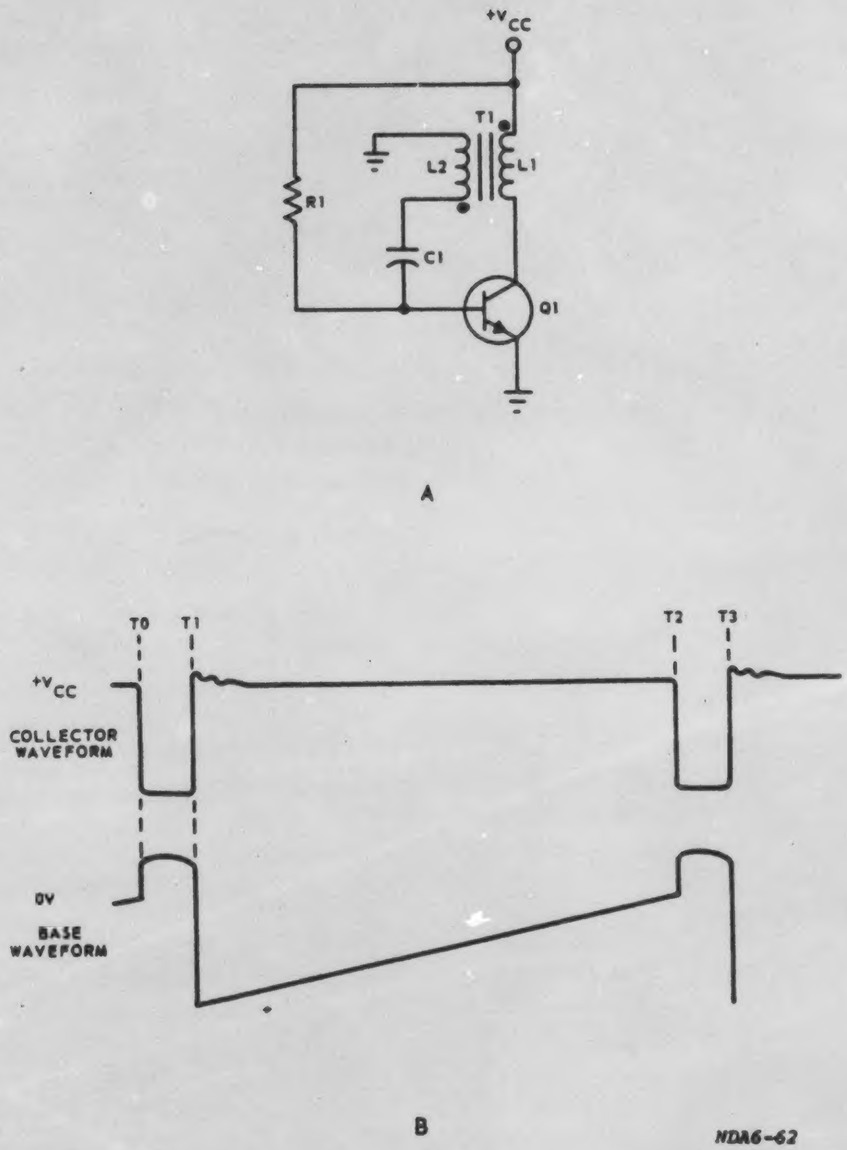

+VCC
T1
L2
L1
R1
C1
Q1
A
T0
T1
T2
T3
+VCC
COLLECTOR WAVEFORM
0V
BASE WAVEFORM
B
NDA6-62

Figure 2-20. Blocking oscillator and waveforms.

length of time between T_0 and T_1 is the PW which depends mainly on the characteristics of the transformer, and the point at which it saturates.

3-25. From T_1 to T_2 (fig. 2-20,B), Q1 is held at cutoff by C1 discharging through R1. Q1 is now said to be *blocked* or *resting*, and the time it is blocked determines the PRT. The PRT is controlled by the time constant of R1 and C1. As C1 gradually loses its charge, the voltage on the base of Q1 gradually returns to a forward-bias condition. At T_2, Q1 is again in a forward-biased condition, and the cycle repeats.

3-26. Note in figure 2-20,B, that the collector waveform indicates positive overshoot at the end of the pulse. This is commonly called *inductive overshoot* or *parasitic oscillation.* It is caused by the collapsing action of the magnetic field in the primary of T_1 when Q1 cuts off. In most computer applications, these oscillations are not desirable, and some means to reduce or dampen them out is required. Recall that this may be accomplished by the use of a transformer whose primary has a high DC resistance and thus a low Q. Also, recall that Q is a quality factor of a coil or resonant circuit that is equal to the inductive reactance (X_L) divided by the resistance. In some applications, damping out these parasitic oscillations is so critical that an external swamping or damping resistor is placed in parallel with the coil (L1 in this case). When

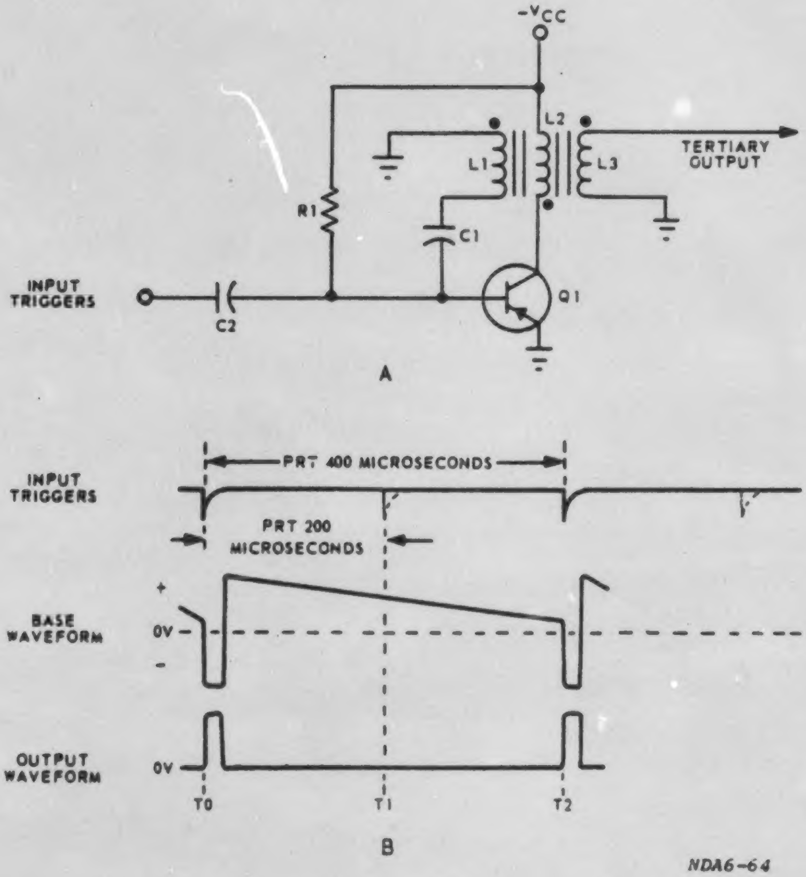

-VCC
L2
TERTIARY OUTPUT
L1
L3
R1
C1
INPUT TRIGGERS
C2
Q1
A
PRT 400 MICROSECONDS
INPUT TRIGGERS
PRT 200 MICROSECONDS
+
BASE WAVEFORM
0V
-
OUTPUT WAVEFORM
0V
T0
T1
T2
B
NDA6-64

Figure 2-21. Synchronized blocking oscillator.

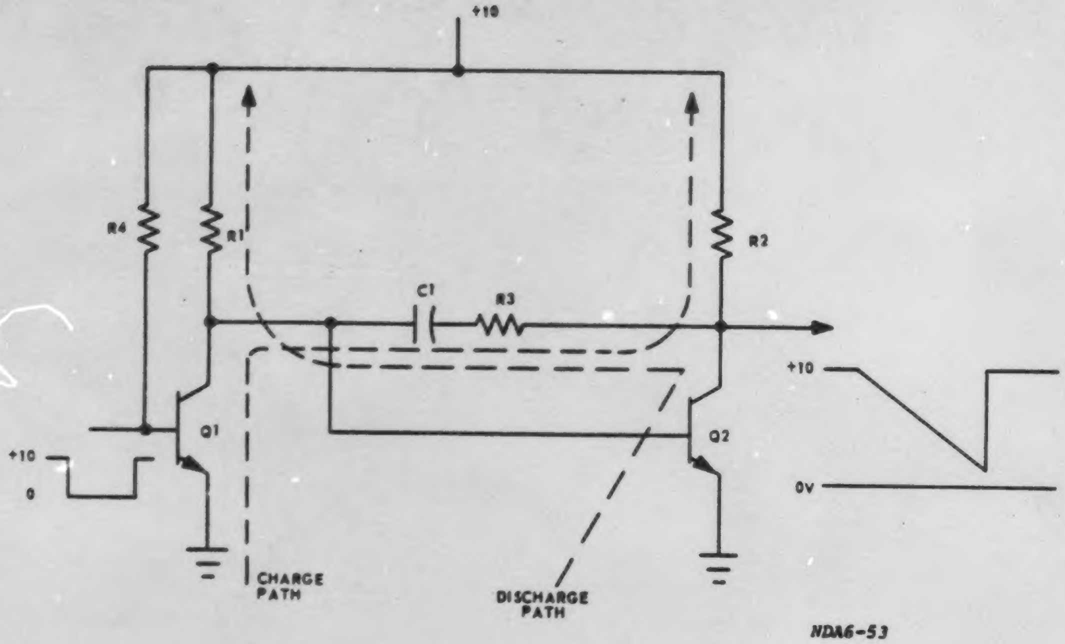


Figure 2-22. Miller integrator.

an external damping resistor is placed across the tank, its Q is then equal to R divided by X_L, where R is the equivalent total circuit resistance in parallel with L.

3-27. *Synchronized blocking oscillator.* If a fixed PRF other than that established by the free-running oscillator is required, the synchronized blocking oscillator illustrated in figure 2-21,A, would be used. Coupling capacitor C2 feeds input synchronization (sync) triggers to the base of Q1, and the PRT output of the circuit is now controlled by the PRT of the sync pulses. That is, if we make the trigger frequency slightly higher than the free-running frequency, the oscillator *locks on* at the higher frequency. For example, in figure 2-21,B, assume the free-running frequency (not shown) is 2 kHz, thus a PRT of 500 microseconds; and the sync pulses shown are occurring at a frequency of 2.5 kHz for a PRT of 400 microseconds (this PRT is indicated in the figure by T_0 and T_2). The oscillator will now *lock on* and run at 2.5 kHz instead of its free-running frequency of 2 kHz. However, when the frequency of the sync triggers is too high, there is a good chance that frequency division could take place. For example, in figure 2-21,B, assume the free-running frequency (not shown) is again 2 kHz, thus a PRT of 500 microseconds. Now we'll apply input triggers at a frequency of 5 kHz, thus a PRT of 200 microseconds (this PRT is indicated in the figure by T_0, T_1, and T_2). Note that the trigger occurring at T_1 is not of sufficient amplitude to overcome the positive cutoff bias on the base of the PNP transistor and turn Q1 on. At T_2, capacitor C1 has nearly discharged and the input trigger does cause Q1 to conduct. This action results in the output frequency of the circuit to be one-half (or 2.5 kHz) of the input trigger frequency (5 kHz). A feature such as this could be used in a computer for frequency division of clock pulses.

3-28. **Miller Integrator.** Another type of nonsinusoidal oscillator circuit is the Miller integrator. A common use for this circuit is to develop a sawtooth wave that is used for generating a sweep voltage; this sweep voltage is then used to move an electron beam across the face of a CRT (cathode-ray tube). This circuit is illustrated in figure 2-22. Circuit operation is as follows: If the base of Q1 is at +10 volts, Q1 conducts and Q2 is cut off. This action provides a low-resistance charge path for C1 through R3 and R2. When the input gate goes to zero volts, Q1 cuts off and Q2 starts to conduct. C1 had charged to some value less than +10 volts. With Q1 cut off, C1 discharges as indicated in the figure; that is, through R1, Q2, and R3. As C1 discharges, the voltage on the base of Q2 becomes more positive and the transistor slowly increases conduction. This, in turn, causes the output

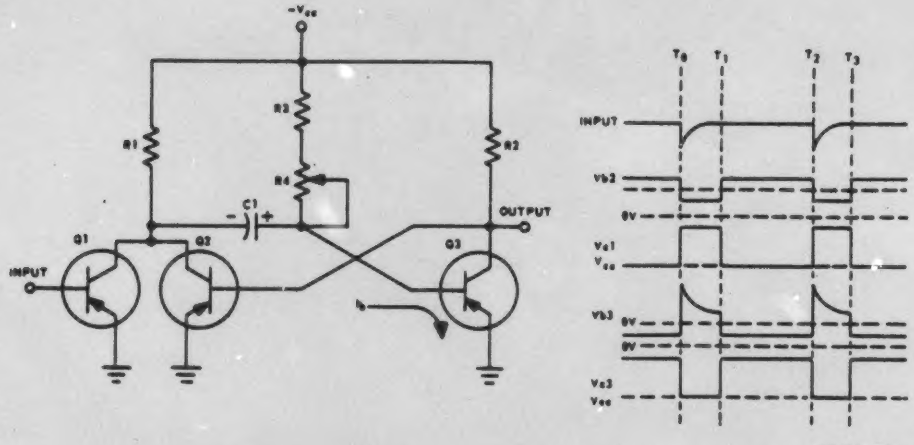


Figure 2-23. One-shot multivibrator.

at the collector to slowly decrease toward zero volts as C1 discharges. When the input returns to +10 volts, Q1 conducts again and Q2 is cut off. Note that the output illustrated at the collector of Q2 is a sawtooth.

3-29. Multivibrators. A multivibrator is a form of relaxation oscillator which comprises two stages, so coupled that the input of each stage is derived from the output of the other. A multivibrator can be free-running or driven, according to whether its frequency is determined by its own circuit constants or by an external synchronizing input. In computers, the multivibrators used most often are the type which require an input signal to cause a particular stage to turn on or off. Recall that multivibrators used in computers are normally called flip-flops (F/Fs). Since a F/F circuit has two stable states, it is used to represent the digits of the binary number system: 0 and 1. When the F/F is used to perform logical binary operations, such as addition, subtraction, multiplication, division, or comparison, it is called a logic F/F.

3-30. *Monostable multivibrator.* Recall that this type of circuit is also called a one-shot or single-shot multivibrator. The one-shot is used in computers for pulse stretching, pulse shaping, gate conditioning, and pulse delaying. Figure 2-23 illustrates a one-shot and its waveshapes; refer to this figure for our discussion of its operation. In the quiescent state (power applied and no input signal), Q3 conducts and Q2 is cut off. Q1 is a switching transistor and conducts only when an input pulse is applied. Prior to time T_0, the circuit is in its quiescent state which means the collector of Q3 is approximately - 0.3 volts. This is sufficient to keep Q2 cut off. The collector of Q2 is, in turn, at the negative V_{CC} voltage. We will assume a negative 9-volt V_{CC} for our discussion.

3-31. At time T_0, a negative pulse is applied to the base of Q1. This negative pulse is inverted at the collector of Q1, which means a positive pulse is coupled by C1 to the base of Q3. This causes Q3 to stop conducting. The collector of Q3 now starts going toward V_{CC}, and this negative-going

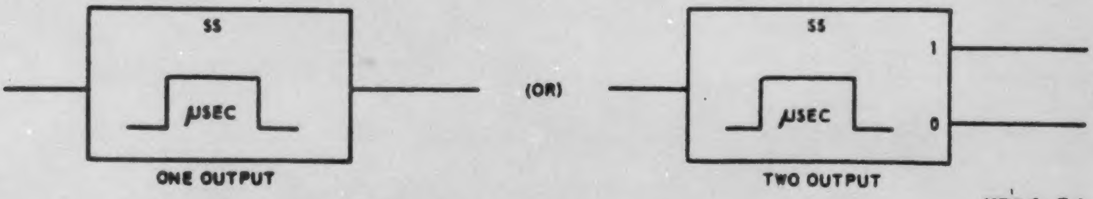


Figure 2-24. Symbol for one-shot multivibrator.

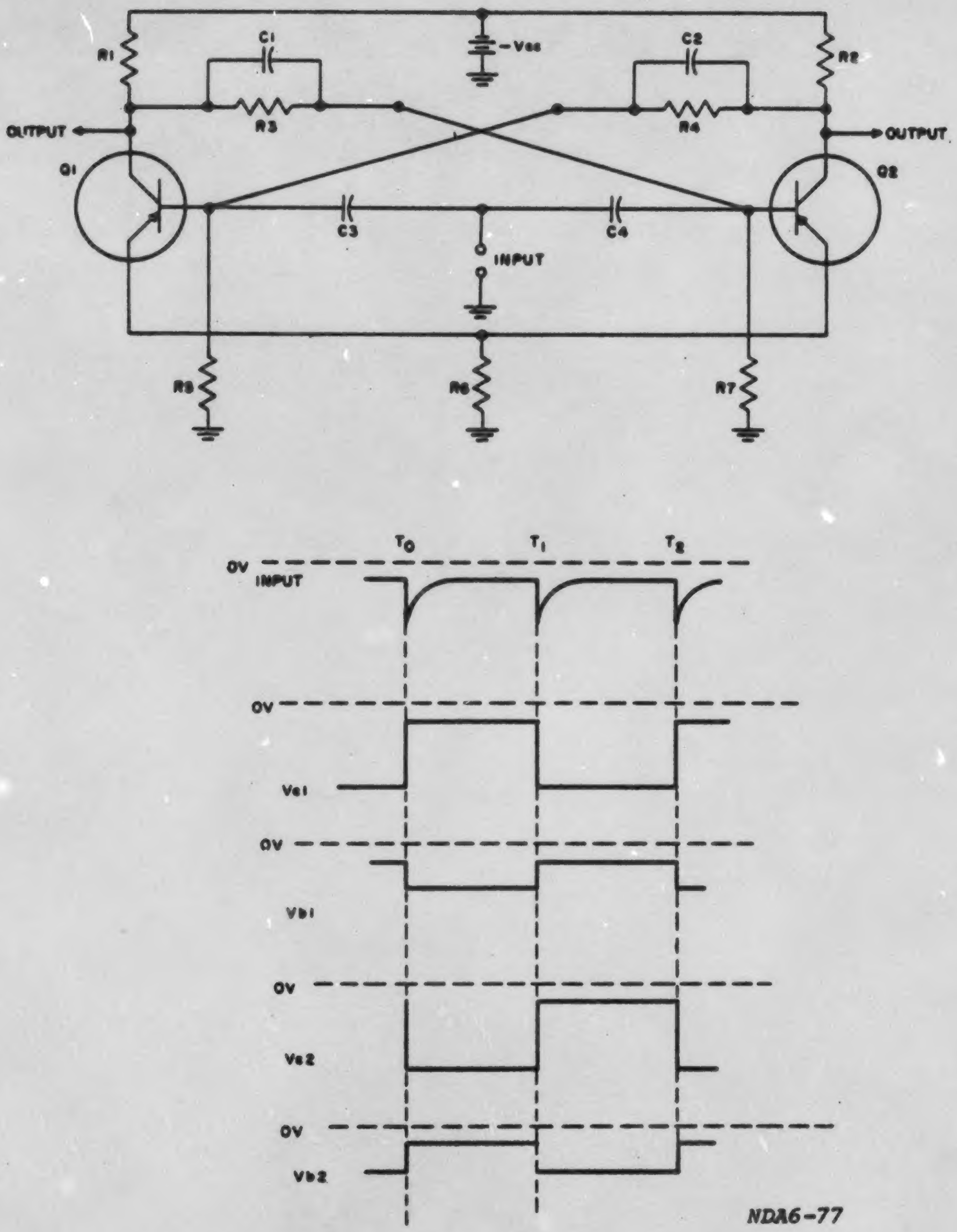

C1
C2
R1
R2
−Vcc
R3
R4
OUTPUT
OUTPUT
Q1
Q2
C3
C4
INPUT
R5
R6
R7
T0
T1
T2
OV
INPUT
OV
Vc1
OV
Vb1
OV
Vc2
OV
Vb2
NDA6-77

Figure 2-25. Bistable multivibrator.

signal (V_{C3}) is directly coupled to the base of Q2, causing it to go into conduction. Q2 conducts as long as Q3 remains cut off. As Q2 conducts, its collector voltage becomes less negative. When this happens, there is nothing to keep the charge on C1. C1 discharges from collector to emitter of Q2, through V_{CC} and then through R3 and R4 to the other plate of C1.

3-32. The voltage drop across R3 and R4 (due to C1 discharging) keeps Q3 cut off until C1 discharges to the cutoff voltage of Q3. Referring to the waveshapes in figure 2-23, notice that the base voltage of Q3 (V_{B3})

follows the discharge of C1 between times T_0 and T_1. Since this voltage determines how long Q3 is cut off, the discharge time determines the width of the output pulse. At time T_1, Q3 starts to conduct and its collector voltage starts to go less negative. This drives Q2 toward cutoff, and C1 is charged again by the base current of Q3. The multivibrator is now back in the quiescent condition and ready to receive the next trigger. The output may be taken from either collector. The width of the output pulse is determined by the values of R1, R3, R4, and C1, since these values determine the discharge time of C1. Two logic symbols for a one-shot multivibrator are shown in figure 2-24.

3-33. *Bistable multivibrator.* The most common F/F circuit used in computers is the bistable (also called an Eccles-Jordan multivibrator). The circuit of a basic bistable multivibrator and its waveforms are shown in figure 2-25. Refer to this figure for our discussion of the circuit operation. In either stable state, one transistor is conducting and the other is cut off. The states are switched by applying the proper trigger pulse. Resistors R1, R3, and R7 form the voltage divider network that develops the forward bias for Q2. R2, R4, and R5 develop the forward bias for Q1. C1 and C2 are called speedup capacitors, and they are used to couple fast changes in the collector circuits to the base circuits which increases the circuits' switching speed.

3-34. Assume that prior to time T_0, Q1 is cut off, the collector voltage (V_{C1}) is near negative V_{CC}, and the base voltage (V_{B1}) is near zero volts. Also assume that just prior to time T_0, Q2 is saturated, the collector voltage (V_{C2}) is near zero volts, and the base voltage (V_{B2}) is negative. At time T_0, a negative trigger pulse is applied to the input. This negative trigger is coupled through C3 and C4 to the base of Q1 and Q2. Q2 is already conducting, so the trigger has no effect on the conduction of Q2. Q1 is cut off and the negative trigger increases the forward bias to a point where Q1 conducts. V_{C1} then goes from near negative V_{CC} to slightly less negative than zero volts. This causes the base voltage of Q2 to change toward zero volts (cutoff). V_{C2} then changes toward the negative V_{CC}. This negative voltage is coupled to the base of Q1 and drives Q1 to saturation. Thus, a stable state of Q1 conducting and Q2 cutoff is reached. The flip-flop remains in this state until another negative trigger is applied at time T_1. At this time, the circuit is flipped back to its other stable state.

3-35. You can now see that the flip-flop has two stable states, In one state, the collector of Q1 is high and the collector of Q2 is low. The opposite is true for the other state. Thus, the output of Q1 could represent yes, true, present, 1, etc., and the output of Q2 could represent the opposite values; that is, no, false, absent, 0, etc. This two-value system is the basis for digital computer logic, and it is for this reason that the bistable multivibrator is widely used in computers. However, the basic Eccles-Jordan F/F we have just discussed must undergo certain circuit

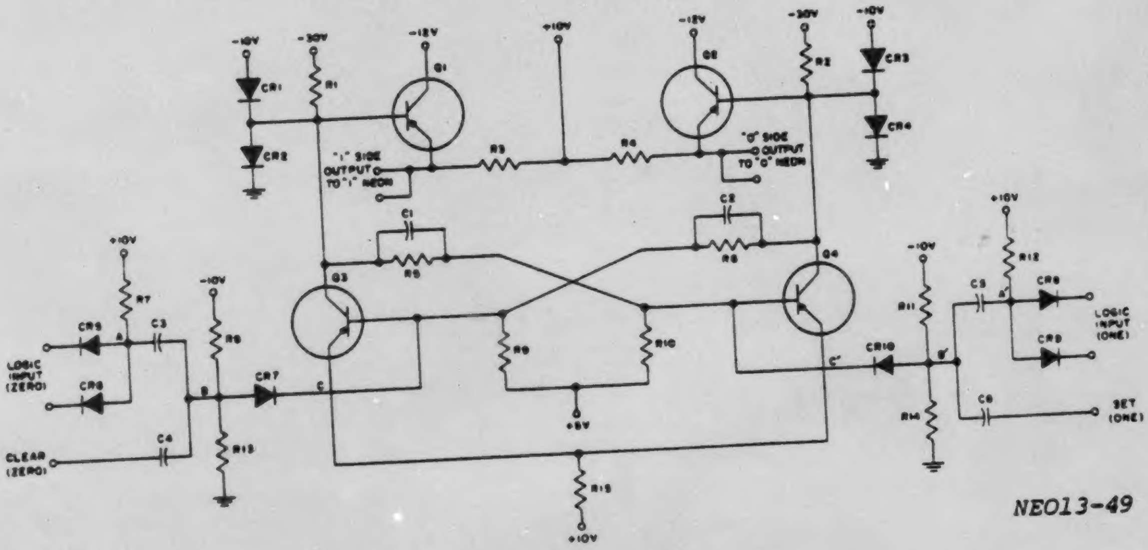


Figure 2-26A. Logic flip-flop.

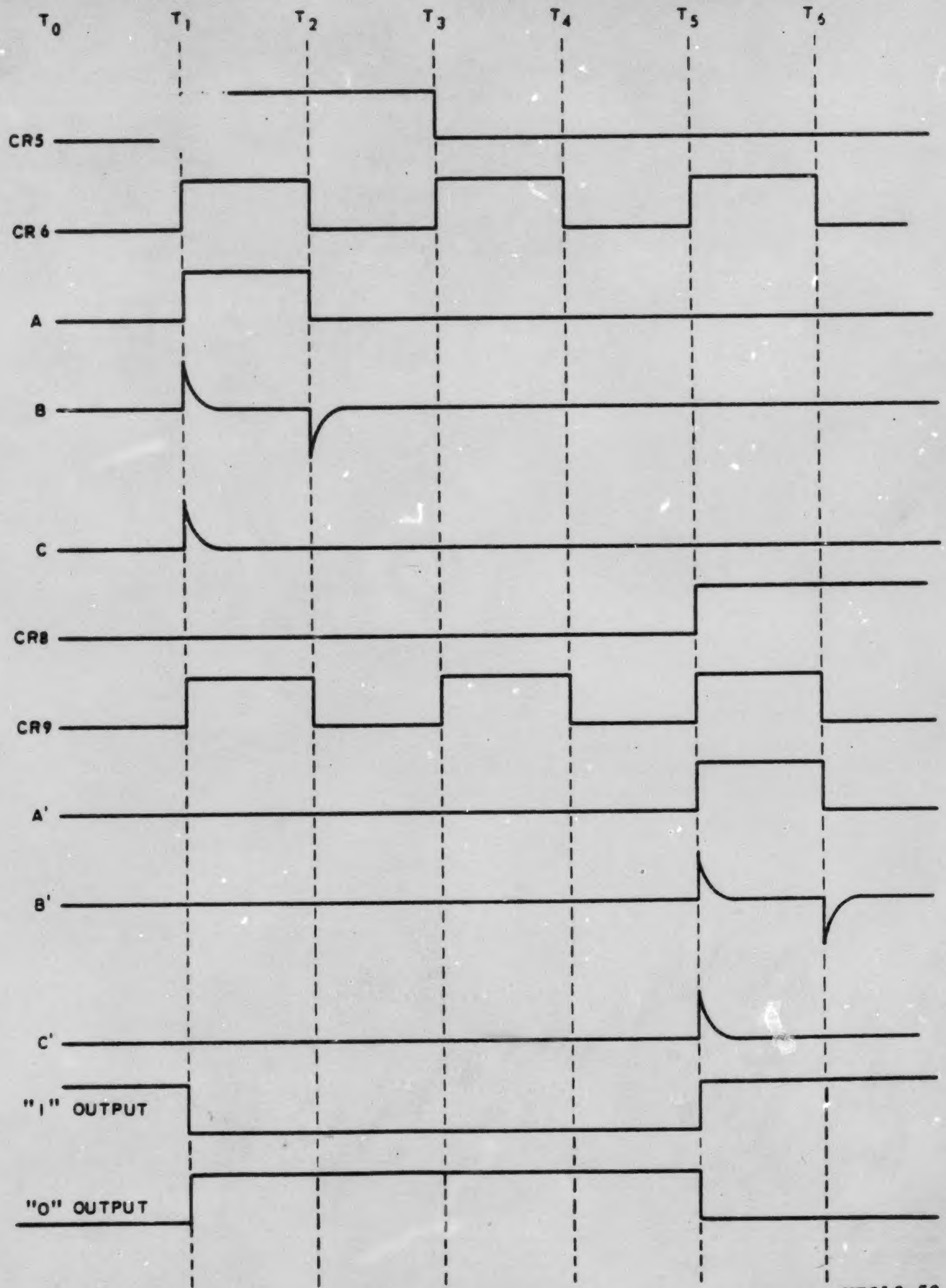

T0
T1
T2
T3
T4
T5
T6
CR5
CR6
A
B
C
CR8
CR9
A'
B'
C'
"1" OUTPUT
"0" OUTPUT
NE013-50

Figure 2-26B. Flip-flop waveform.

changes to be used as a logic F/F within a computer.

3-36. *Logic flip-flop*. Just how does the basic Eccles-Jordan multivibrator differ from the logic flip-flop? Figure 2-26A illustrates a version of the computer logic F/F with several circuit modifications which render it compatible for use with other logic circuits. These modifications consist of the following:

- Logical switching circuits at the inputs to insure the F/F triggers at the desired time.
- Circuits for presetting the F/F to a desired state.
- Differentiating circuits to provide sharp trigger pulses.
- Visual indicators of the F/F's state: 1 or 0.
- Limiting circuits to establish the desired logic levels.

For the following circuit analysis of this particular logic F/F, positive logic is assumed. That is, a relatively high voltage represents the binary 1 and a low voltage represents a binary 0.

3-37. Transistors Q3 and Q4 form the basic multivibrator. Q3 is the ONE-side transistor and Q4 is the ZERO-side transistor. R1 and R2 are collector-load resistors. R2, R6, and R9 form the voltage divider network for forward-biasing Q3. R1, R5, and R10 form the voltage divider network for forward-biasing Q4. The important portion of the forward bias for operation of this circuit is developed across R9 and R10. C1 and C2 couple fast collector changes to the transistor bases in order to increase the switching speed of the flip-flop. The inputs to the flip-flop consist of SET and CLEAR circuits and logic input circuits. The logic circuits in this case are positive AND-gates. CR5, CR6, and R7 form the AND-gate that feeds the ONE-side transistor and clocks the flip-flop to the ZERO state. CR8, CR9, and R12 form the AND-gate that feeds the ZERO-side transistor and clocks the flip-flop to the ONE state. The CLEAR (ZERO) input is fed to C4 and the SET (ONE) input is fed to C6. These inputs make it possible to preset the flip-flop to a desired state.

3-38. C3, R13, C5, and R14 are differentiating networks that differentiate the outputs of the AND-gates. C4, R13, C6, and R14 form the differentiating networks for the CLEAR and SET inputs. R8, R13, R11, and R14 form voltage divider networks that place negative potentials on the anodes of CR7 and CR10. This negative potential allows them to conduct only on the positive spike of the differentiated wave and permits CR7 and CR10 to perform their functions as limiting diodes, clipping the negative spikes. Transistors Q1 and Q2 are emitter followers. The outputs are taken from their emitters. CR1, CR2, CR3, and CR4 are limiting diodes that maintain the logic levels at 0 volts (logic 1) and - 10 volts (logic 0). The outputs are connected to neon indicators so that the state of the flip-flop can be determined by visual inspection. These indicators are not shown in the figure.

3-39. At time T_0, the flip-flop is in the ONE state. This means Q3 is conducting and Q4 is cut off. The ONE-side output is at 0 volts and the ZERO-side output is at - 10 volts. At time T_1, signals are applied to CR5 and CR6, as shown in figure 2-26B. The signals identified as A, B, and C in figure 2-26B are the signals at points A, B, and C in the circuit. Signal A is the output of the AND-gate. Signal B is the output of the differentiating network. Signal C is the output of the limiting diode. Since both the ONE-side and the ZERO-side input circuits and their waveshapes will be the same, it is sufficient to explain only one input circuit.

3-40. The input signals (CR5 and CR6) to the circuit are both high during the time from T_1 to T_2. This is the only time an output from the AND-gate will be present, as illustrated by signal A. Signal A is then differentiated by C3 and R13 (signal B), and the negative spike is clipped by CR7 (signal C). The positive spike of the signal at C is applied to the base of Q3 at time T_1 and will cut off Q3. The collector voltage of Q3 goes to a negative potential. This negative change is coupled by C1 to the base of Q4. This causes Q4 to conduct. The collector voltage of Q4 decreases toward zero volts. This decrease is coupled by C2 to the base of Q3 and keeps Q3 cut off. With Q3 cut off, the collector voltage is at - 10 volts because of the logic level establishing diode CR1. This voltage (a low) is applied to the base of Q1, and the output of - 10 volts is taken from the emitter of Q1. This is the ONE-side output.

3-41. After time T_1, Q4 is saturated and the collector is at zero volts because of the clamping action of CR4. This voltage (a high) is applied to the base of Q2, and the output of zero volts is taken from the emitter of Q2. This is the ZERO-side output. The flip-flop is now in the ZERO state, and remains in this stable state—the ZERO state—until time T_5. At this time, the inputs to CR8 and CR9 (as shown in fig. 2-26B) activate the logic input (ONE) gate. Signals A′, B′, and C′ are generated and a positive trigger (C′) is applied

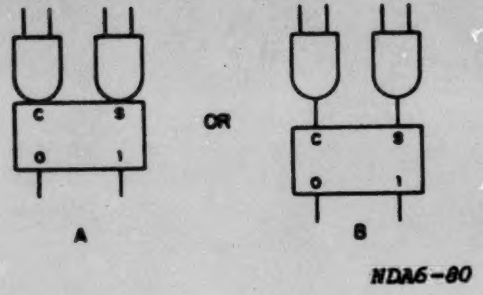


Figure 2-27. Flip-flop logic symbols.

to the base of Q4. This cuts off Q4 and clocks the flip-flop to the ONE state, with Q3 conducting and Q4 cut off. The multivibrator action is the same as was discussed in clocking the F/F to the ZERO state.

3-42. Two of the logic symbols that are used for the logic F/F are shown in figure 2-27. The symbol in part A of the figure is used when the logic input gates are physically integral with F/F functions. The symbol in part B is used when the logic gates are physically separated from the F/F.

3-43. Up to this point, our discussion of computer circuits has, with the exception of the logic F/F just discussed, primarily centered around the operation of nonlogic circuits. Our next discussion in Section 4 reviews the principles of Boolean algebra, which is an aid to understanding the operation and function of the logic switching gates that are discussed in detail in Section 5.

4. Boolean Algebra

4-1. Boolean algebra, the science of symbols and their combinations, is used to describe and represent mathematical functions according to the rules of logic. No practical use was made of this system of translating the rules of formal logic into mathematical terms until it was found that it could be used to indicate the logical functions of telephone and computer switching circuits. The increasing use of computers has created a rapid growth in the application of Boolean algebra.

4-2. Boolean algebra is very different from ordinary algebra and, for this reason, it may seem confusing at first. Actually, the part of it that you need to know is not very difficult. However, a good understanding of Boolean algebra will help you to understand logic circuits.

4-3. In ordinary algebra, there are four basic operations: addition, subtraction, multiplication, and division. In Boolean algebra, there are only three operations or functions: AND, OR, and NOT. The multiplication and addition symbols in ordinary arithmetic indicate the first two operations. For example, $A \cdot B$ means A AND B, and $A + B$ means A OR B. The multiplication sign ($\cdot$) means AND operation and the addition sign (+) means OR operation. The dot may be omitted in the AND operation, or parentheses may be used to indicate the AND operation. For example, $A \cdot B = AB = (AB)$. To denote the NOT operation, a bar (called the vinculum) is placed over the letter. For example, $\bar{A}$ means NOT A and $\bar{B}$ means NOT B.

4-4. Boolean algebra is the algebra of *true* or *false*, *on* or *off*, and *conducting* or *cut off*. Since this is true, the digits of the binary number system are well suited for Boolean representation. So there are only two numerical values in Boolean algebra: 1 and 0. Let's see how Boolean algebra applies to computer operations.

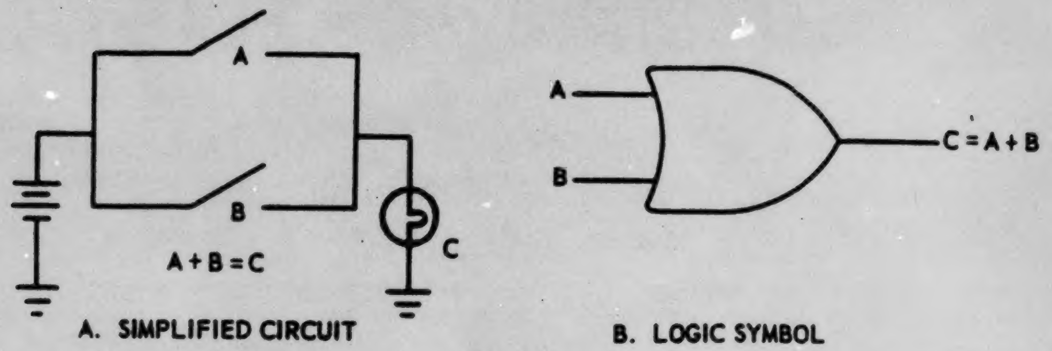
4-5. OR Function. An equation in ordinary algebra such as $A + B = C$ has an infinite number of possible values, since A and B can be assigned any value. On the other hand, an equation in Boolean algebra can have only two possible values. The values are either 0 or 1. Therefore, in the Boolean equation "A *OR* B equals C," there are only four possible numerical combinations. These are:

$A + B = C$
$0 + 0 = 0$
$0 + 1 = 1$
$1 + 0 = 1$
$1 + 1 = 1$

4-6. These results could represent a standard binary addition table, except for the last entry. When both A and B are 1, the result is 1. The + symbol, therefore, does not have the same meaning as in ordinary algebra but is a logic addition symbol. Also, from the equation $1 + 1 = 1$, you can see that there is no such quantity as 2 in Boolean algebra.

4-7. Any number of variables can be represented in an OR equation. For instance, in the equation $W + X + Y + Z = A$, if W, X, Y, Z all have the value of 1, the sum of the values, A, represents a 1. That is, if either one or all of the quantities in the equation are 1, the result is 1. Conversely, if all the quantities in the equation are 0, the result is 0.

4-8. Part A of figure 2-28 illustrates the OR function by the use of a simplified light switching circuit. Figure 2-28,B, shows the logic symbol for this circuit which is called a



A. SIMPLIFIED CIRCUIT

B. LOGIC SYMBOL

NEO13-1

Figure 2-28. OR function and logic symbol.

gate. Switches A and B are represented by a 1 when they are in the closed position and by a 0 when they are in the open position. Also, light C is represented by a 1 when it is on and by a 0 when it is off.

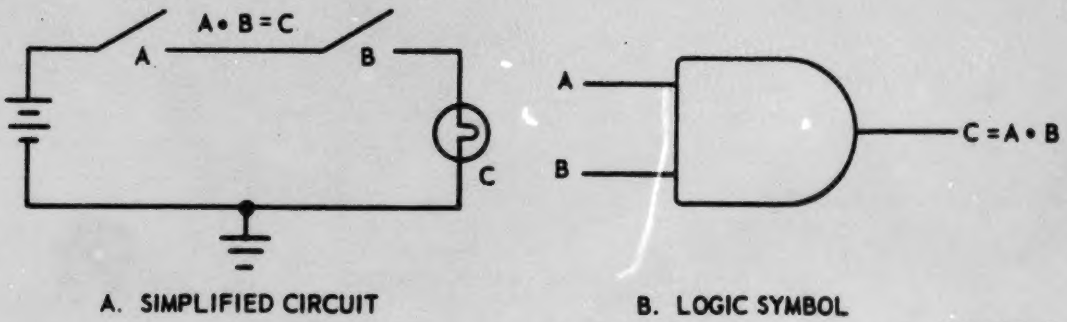
4-9. Let's see what conditions must exist for light C to be on. With switch A closed and switch B open, light C will be on and the circuit can be represented by the equation 1 + 0 = 1. With switch A open and switch B closed, light C will be on and the circuit can be represented by the equation 0 + 1 = 1. With both switches closed, light C will be on and the circuit can be represented by the equation 1 + 1 = 1. With both switches open, light C will be off and the equation for the circuit is 0 + 0 = 0. These four combinations are the same as the four possible combinations for the Boolean equation A + B = C. Therefore, this circuit performs the OR operation or function. The logic symbol in figure 2-28,B, represents the schematic shown in figure 2-28,A.

4-10. **AND Function.** In ordinary algebra, the equation $A \cdot B = C$ means A multiplied by B equals C. Because A and B can be assigned any value, the equation can have an infinite number of values. However, since Boolean algebra uses only the values 1 and 0, there are only four possible combinations in the Boolean equation A AND B equal C. These are:

$A \cdot B = C$
$0 \cdot 0 = 0$
$0 \cdot 1 = 0$
$1 \cdot 0 = 0$
$1 \cdot 1 = 1$

4-11. In the AND equation, the result is 1 only when all the variables are 1. Here, again, any number of variables can be represented in the AND equation. However, as in ordinary multiplication, the product is 1 only if all the factors are 1.

4-12. Figure 2-29,A, illustrates the AND function by the use of a simplified light switching circuit. Figure 2-29,B, shows the logic symbol for this circuit. Switches A and B are represented by a 1 when they are in the closed position and by a zero when they are in the open position. Also, light C is represented by a 1 when it is on and by a zero when it is off.

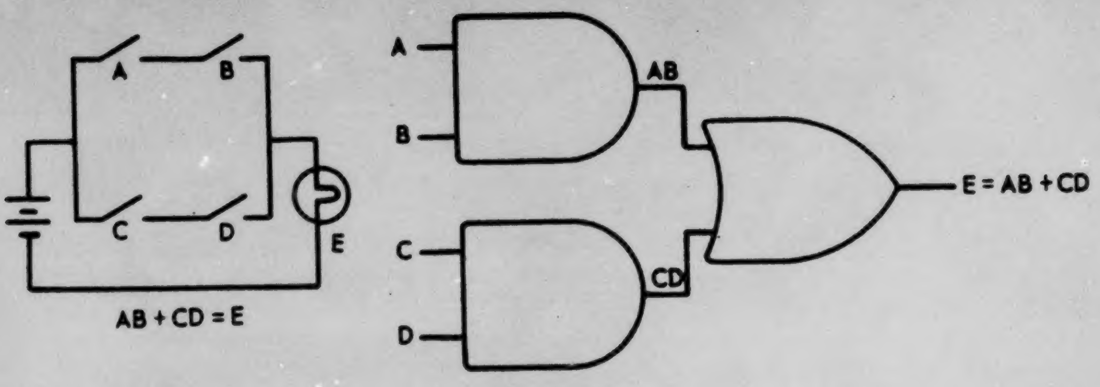


A. SIMPLIFIED CIRCUIT

B. LOGIC SYMBOL

NEO13-2

Figure 2-29. AND function and logic symbol.



A. SIMPLIFIED CIRCUIT

B. LOGIC DIAGRAM

NE013-3

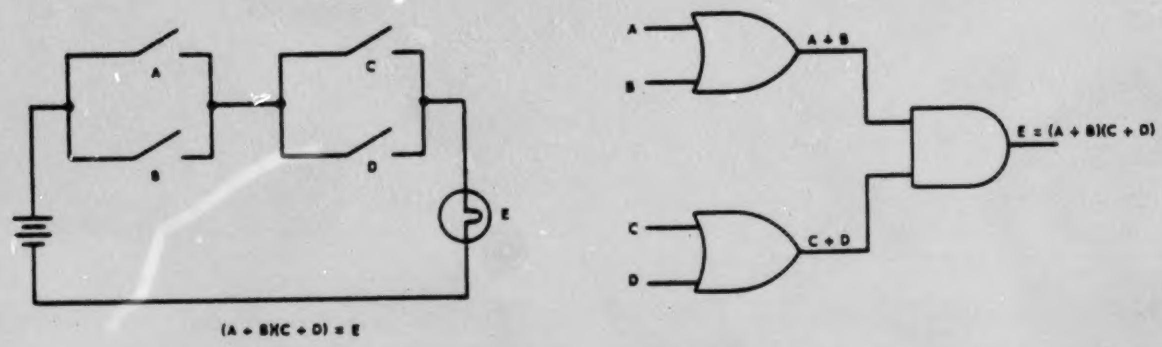
Figure 2-30. Combination AND-OR.

4-13. Let's see what conditions must exist for light C to be on. With switch A closed and switch B open, light C will be off and the circuit can be represented by the equation $1 \cdot 0 = 0$. With switch A open and switch B closed, light C will be off and the circuit can be represented by the equation $0 \cdot 1 = 0$. With both switches closed, light C will be on and the circuit can be represented by the equestion $1 \cdot 1 = 1$. With both switches open, light C will be off. The equation for the circuit now is $0 \cdot 0 = 0$. These four combinations are the same as the four possible combinations for the Boolean equation $A \cdot B = C$. Therefore, the circuit performs the AND operation or function. Instead of drawing the schematic, the symbol in figure 2-29,B, is used to represent this circuit.

4-14. **Combination AND-OR Functions.** Complex switching networks are frequently required to do a combination of logical functions. Figure 2-30,A, illustrates a circuit in which the light (E) is on when switches A and B or C and D are closed. This circuit illustrates an OR function combined with two AND functions. The Boolean equation for this circuit is $AB + CD = E$ and is read A AND B OR C AND D equals E. Figure 2-30,B, shows the logic diagram for this circuit. Study figure 2-30,A, to verify the equation.

4-15. Figure 2-31,A, shows a simplified light switching circuit in which two OR functions are combined with an AND function. The equation for this circuit is $(A + B)(C + D) = E$ and is read A OR B AND C OR D equals E. The logic diagram for this circuit is shown in figure 2-31,B. Study figure 2-31,A, to verify the equation.

4-16. **NOT Function.** A basic concept found in Boolean algebra that has no counterpart in ordinary algebra is the NOT function. The NOT function denotes the complement of a Boolean expression. A line

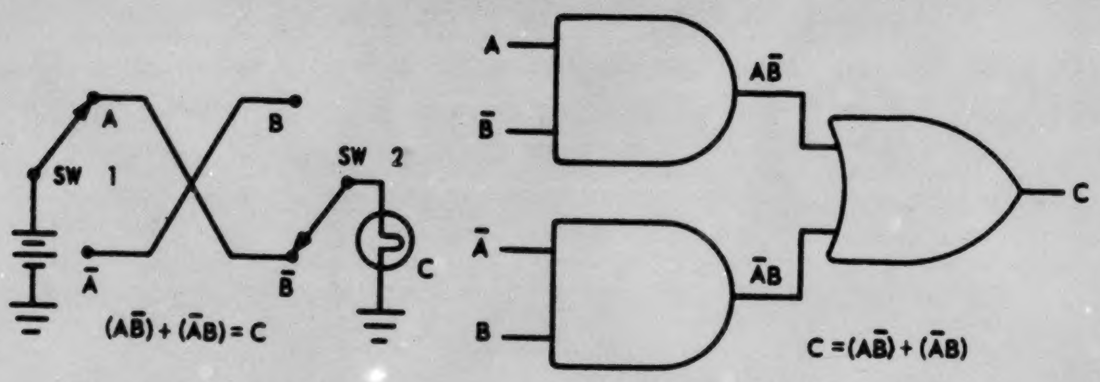


A. SIMPLIFIED CIRCUIT

B. LOGIC DIAGRAM

NE013-4

Figure 2-31. Combination OR-AND.



A. SIMPLIFIED CIRCUIT

B. LOGIC DIAGRAM

NEO13-5

Figure 2-32. NOT function.

over an expression is used to indicate the NOT function. For example, $\overline{0}$ means NOT 0 and has a value of 1, since 1 is the complement of 0. For the same reason, $\overline{1}$ has a value of 0. So, when A is 1, $\overline{A}$ is 0, and when A is 0, $\overline{A}$ is 1.

4-17. Figure 2-32,A, is a simplified light switching circuit that illustrates a use of the NOT function. In this case, the NOT function is used to label alternate switch positions so that switch action may be indicated by a Boolean equation. This is the common switching circuit used to turn the same light on or off from two different switches. It is often used for a stairway light that can be turned on or off from either upstairs or downstairs. The logic diagram for the circuit is shown in figure 2-32,B.

4-18. Switch 1 has two positions labeled A and $\overline{A}$. When switch 1 is in the UP position, it makes contact at A, and since a closed circuit is represented by a 1, A = 1 and $\overline{A}$ = 0. When switch 1 is in the DOWN position, it makes contact with $\overline{A}$, and since a closed circuit represents 1, $\overline{A}$ = 1 and A = 0. The same can be applied to switch 2. When B equals 1, $\overline{B}$ equals 0. When B equals 0, $\overline{B}$ equals 1.

TABLE 2-2
TRUTH TABLE FOR CIRCUIT IN FIGURE 2-32

A	$\overline{A}$	B	$\overline{B}$	$A\overline{B}$	$\overline{A}B$	$A\overline{B} + \overline{A}B$
0	1	0	1	0	0	0
1	0	0	1	1	0	1
0	1	1	0	0	1	1
1	0	1	0	0	0	0

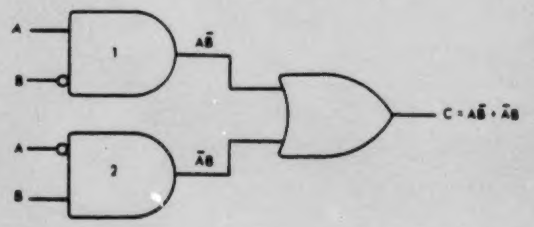
NDA6-39

4-19. There are two possible combinations of switch positions that turn the light on and two that turn it off, as follows:

Light on	A and $\overline{B}$
	$\overline{A}$ and B
Light off	A and B
	$\overline{A}$ and $\overline{B}$

4-20. Therefore, if switch 1 is in the A position and switch 2 is in the $\overline{B}$ position or if switch 1 is in the $\overline{A}$ position and switch 2 is in the B position, light C is on. The equation for this AND-OR combination is $A\overline{B} + \overline{A}B = C$.

4-21. To show all possible combinations of values for A and B that may be placed into the equation, it is helpful to construct a table



NEO13-6

Figure 2-33. Logic diagram illustrating state indicators.

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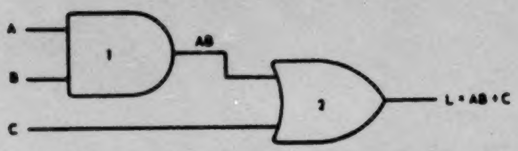


Figure 2-34. Logic diagram.

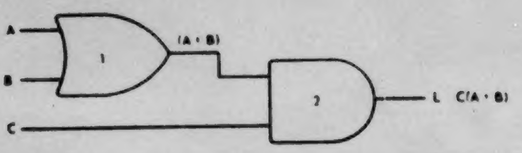


Figure 2-35. Logic diagram.

of possible values for the variables. This table is called a *truth table*. The truth table for the equation for the circuit in figure 2-32 is shown in table 2-2. Study figure 2-32 and table 2-2 to verify the information in the truth table.

4-22. The NOT function is important in computer logic, because it is sometimes necessary to indicate that a circuit has an output of 1 only when a certain expression is *not* present, as in the equation $C = A\overline{B}$. This is the equation for part of the circuit shown in figure 2-32,A, and states that C is 1 when A is 1 and NOT B is 1. In figure 2-33, the logic diagram is the same as in figure 2-32 except that small circles, called *state indicators*, are drawn at the inputs to the AND circuits and $\overline{B}$ is changed to B. The state indicator in figure 2-33 shows that AND circuit 1 is inhibited when B is present and activated when the NOT function of B is present along with the presence of A. Read this paragraph and study figure 2-33 again.

4-23. **Equivalent Expressions.** Refer again to figure 2-28. The equation that represents this OR circuit when light C is on is $A + B = C$. This equation states that C is present when A is present OR when B is present. When light C is off, the equation which represents the circuit is $\overline{(A + B)} = \overline{C}$. This equation indicates that C is not present when the quantity (A + B) is not present and is read: NOT the quantity of A OR B equals NOT C. Looking again at figure 2-28, you can see that C is not present when both A and B are not present. From this, you can develop the equation $\overline{A} \cdot \overline{B} = \overline{C}$ to represent the circuit. You now have two expressions which are equal to the same quantity. This makes these two expressions equal to each other. That is, $\overline{A} \cdot \overline{B} = \overline{(A + B)}$.

4-24. Refer to the AND circuit in figure 2-29. The equation which represents this circuit when light C is on is $A \cdot B = C$. The equation states that C is on when A is present and B is present. When light C is off, the equation for the circuit is $\overline{A \cdot B} = \overline{C}$ and is read: NOT the quantity of A AND B equals NOT C. Looking again at figure 2-29, note that C will not be present when either A or B is not present. From this, the equation $\overline{A} + \overline{B} = \overline{C}$ represents the circuit. Again, we have two expressions which are equal to the same quantity. This makes these two quantities equal to each other. That is, $\overline{A \cdot B} = \overline{A} + \overline{B}$.

4-25. **Application of Boolean Algebra.** To write the equation for a logic diagram, begin by writing the equation for the gate *farthest* from the final or output gate. Then, in a step-by-step manner, write the equation for each gate, proceeding toward the final or output gate. For example, look at the logic diagram in figure 2-34. To write an equation for the output (OR-gate 2), first write the equation for AND-gate 1. This equation is

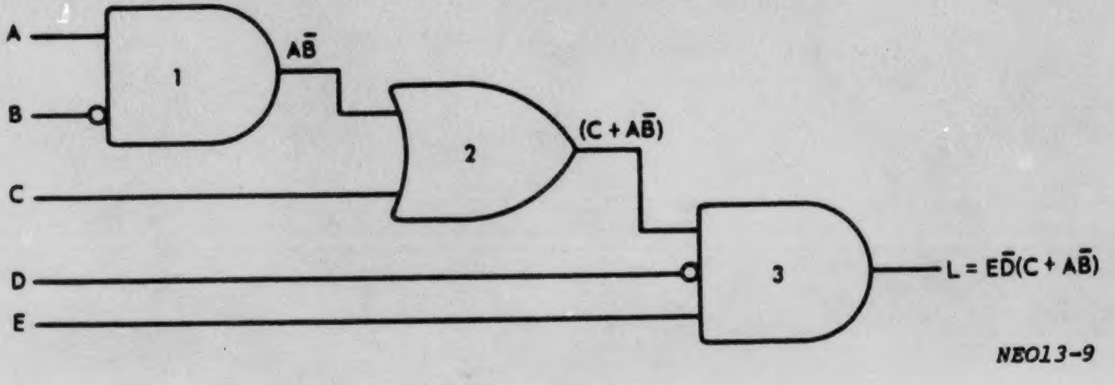


Figure 2-36. Logic diagram.

213

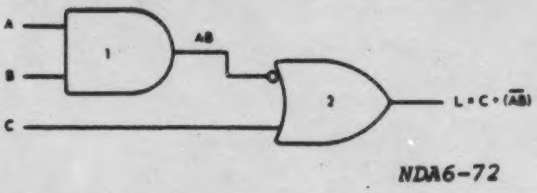


Figure 2-37. Logic diagram.

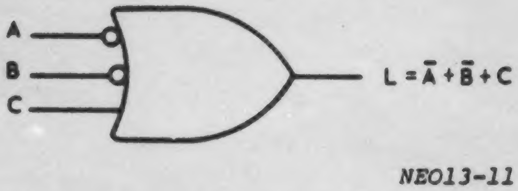


Figure 2-38. Logic diagram.

AB. The output of AND-gate 1 (AB) and C are inputs to OR-gate 2. The output of AND-gate 1 is OR'ed with input C in OR-gate 2. Then the output, L, is present when A AND B are present OR when C is present. The equation then is L = AB + C.

4-26. Figure 2-35 shows the output of an OR-gate (1) as an input to an AND-gate (2). The output from OR-gate 1 is AND'ed with input C to AND-gate 2. The equation for the output of OR-gate 1 is A + B. Then the output of AND-gate 2, L, is present when A OR B is present AND when C is present. The equation then is L = C (A + B).

4-27. Figure 2-36 illustrates how the NOT function is used. When gate 1 is activated, the equation for the output is $A\bar{B}$. The inputs needed to activate gate 2 are the output of gate 1 OR C; therefore, the equation for the output of gate 2 is C + $A\bar{B}$. The inputs needed to activate gate 3 are the output of gate 2 AND $\bar{D}$ AND E; therefore, the equation for the output of gate 3 is L = $E\bar{D}$ (C + $A\bar{B}$).

4-28. In figure 2-37, the state indicator at gate 2 shows that the output of AND-gate 1, AB, inhibits OR-gate 2. Therefore, for OR-gate 2 to be activated, C must be present OR the NOT function from AND-gate 1 must be present. Thus, the equation for the output of OR-gate 2 is L = $\overline{AB}$ + C. Substituting $\bar{A} + \bar{B}$ for $\overline{AB}$, the equation becomes L = $\bar{A} + \bar{B}$ + C. This equation can be represented by a different logic diagram which is shown in figure 2-38.

4-29. **Drawing Logic Diagrams.** To draw a logic diagram to represent a given Boolean equation, reverse the steps for writing the equation for the logic diagram. That is, start with the diagram of the output gate and proceed to draw the logic diagram for each input.

4-30. For example, the first gate to be drawn for the Boolean expression F + [$\bar{D}$E ($A\bar{B}$ + C)] is the OR-gate shown in figure 2-39. Now draw the OR-gate input $E\bar{D}$ ($A\bar{B}$ + C) shown in figure 2-39 as the output of the three-input AND-gate shown in figure 2-40. Next, draw the AND-gate input $A\bar{B}$ + C shown in figure 2-40 as the output of the two-input OR-gate shown in figure 2-41. Draw the OR-gate input $A\bar{B}$ shown in figure 2-41 as the output of the two-input AND-gate shown in figure 2-42. Combine the gates shown in figures 2-39 through 2-42, and you have the complete logic diagram for the Boolean expression F + [$E\bar{D}$ ($A\bar{B}$ + C)] as shown in figure 2-43.

4-31. **Simplifying Boolean Equations.** Sometimes, simplifying a Boolean equation results in the use of fewer gates in its logic diagram. For example, the logic diagram for the Boolean equation X = AC + AD + BC + BD is shown in figure 2-44. Here you see that 12 signal paths and five gates are required for this equation. However, the equation X = AC + AD + BC + BD can be factored as in ordinary algebra, thus:

$$\begin{aligned} X &= AC + AD + BC + BD \\ &= A(C + D) + B(C + D) \\ &= (A + B)\ (C + D) \end{aligned}$$

The simplified equation is X = (A + B) (C +

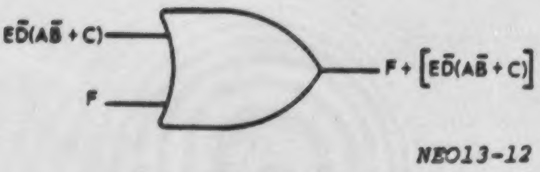


Figure 2-39. Logic diagram.

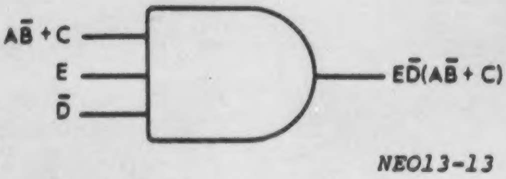


Figure 2-40. Logic diagram.

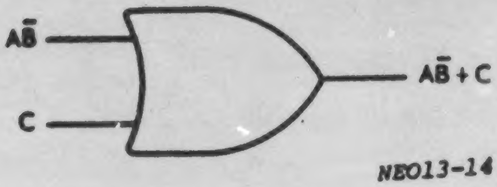


Figure 2-41. Logic diagram.

D). The logic diagram for this equation is shown in figure 2-45. Now there are six signal paths and three gates. Compare figures 2-44 and 2-45 and note that they are equivalent. You can use simplification of Boolean equations to determine the most practical circuit.

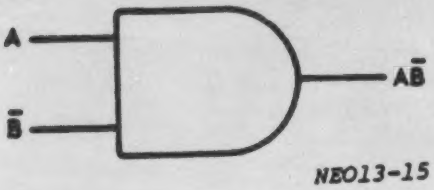


Figure 2-42. Logic diagram.

4-32. In the example just explained, we simplified the Boolean equation by factoring as in ordinary algebra. Also, just as in ordinary algebra, terms may be expanded in Boolean algebra. For example, expand the Boolean expression $(A + B)(\overline{A} + \overline{B})$:

$$(A + B)(\overline{A} + \overline{B}) = A\overline{A} + A\overline{B} + B\overline{A} + B\overline{B} =$$
$$A\overline{B} + B\overline{A} \; (\overline{A}A = 0 \text{ and } B\overline{B} = 0)$$

4-33. Now, let's see how to NOT an equation to simplify it. We have already proved that $\overline{AB} = \overline{A} + \overline{B}$. Study this equation,

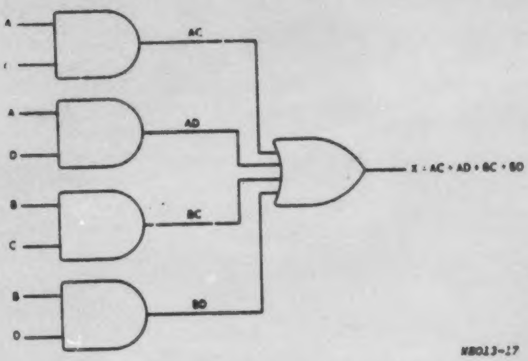


Figure 2-44. Logic diagram.

and you can see that to NOT or complement a Booleen equation or expression, change the sign of operation and NOT or complement each term. For example, to NOT the expression $\overline{A + B}$, change the operation (+) to (·) and NOT each term. This gives $\overline{A} + \overline{B} = \overline{A} \cdot B$. Remember that $\overline{AB}$ and $\overline{A}\,\overline{B}$ are not the same. The bar over an equation or expression means to NOT or complement the entire expression. Let's take another example. Simplify $L = A + \overline{(B + C)(D)}$:

$$L = A + (\overline{B + C}) + \overline{D}$$
$$L = A + \overline{B}\,\overline{C} + \overline{D}$$

5. Logic Gates

5-1. In Boolean algebra, you studied basic logical functions in terms of information only. The logic blocks used to diagram the functions actually represent physical circuits. Now, let's see how physical (computer) circuits operate according to the rules of these functions. As inputs of these computer circuits, we use electrical signals which represent the facts that must be logically

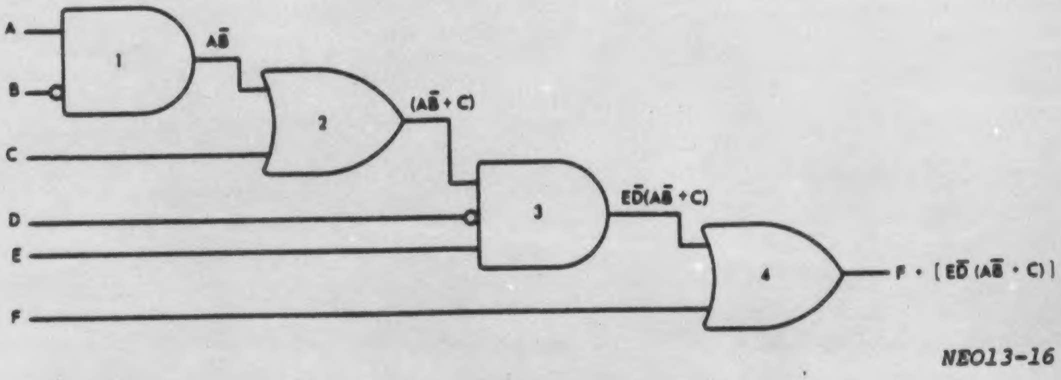


Figure 2-43. Logic diagram.

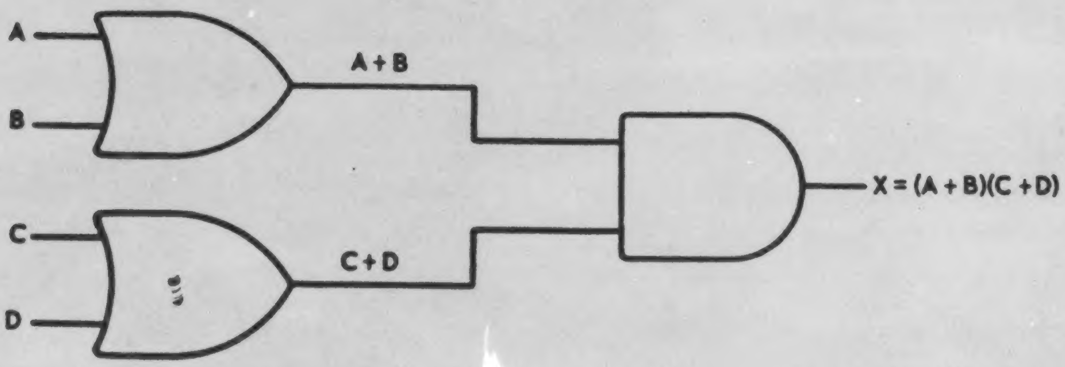


Figure 2-45. Logic diagram.

processed. Each output is an electrical signal which represents the result of applying the rules of a particular logical function to a set of inputs. In other words, each output is a logical conclusion.

5-2. The switching devices commonly used in logic circuits are determined by the state of the art and the job. Relays, semiconductor diodes, vacuum tubes, transistors, and magnetic cores are used today. Tomorrow's devices may be different, for research is constantly seeking smaller, faster, more efficient, and more reliable switching devices.

5-3. First, let's discuss the operation of logic switching circuits called *gates*. A gating circuit operates in very much the same manner as its name implies. It acts as a valve or a swinging door that determines whether a pulse is passed or stopped. Gates can perform AND, OR, and NOT functions.

5-4. **Diode Logic Gates.** Many computers use *diode logic*; that is, they perform most logical operations in circuits made up of diodes (usually semiconductor). Vacuum tube or transistor circuits are used primarily for building up weak or attenuated pulses.

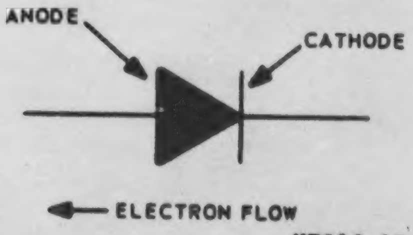


Figure 2-46. Solid-state diode symbol.

5-5. The solid-state diode, like the vacuum-tube diode, has an anode and a cathode, as shown in figure 2-46. It offers practically no forward resistance to the flow of electrons from the cathode to the anode; in other words, it conducts easily when the anode is made more positive than the cathode. However, when the cathode is more positive than the anode, the diode offers a very high resistance and practically no current can flow.

5-6. *Diode positive AND-gate or negative OR-gate.* Figure 2-47 shows a diode logic gate that may perform either the positive AND or the negative OR function. The inputs are connected in parallel, each through a separate

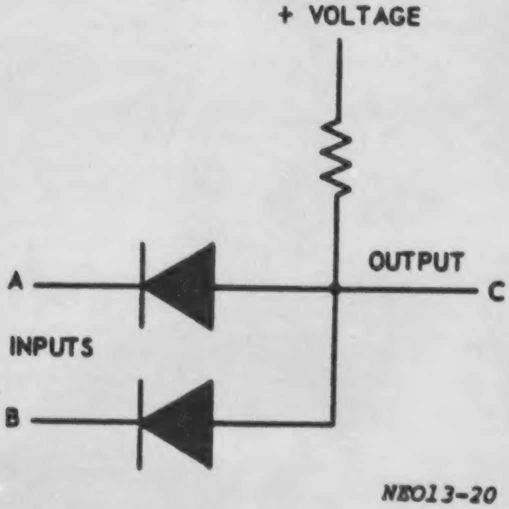


Figure 2-47. Diode positive AND- or negative OR-gate.

212

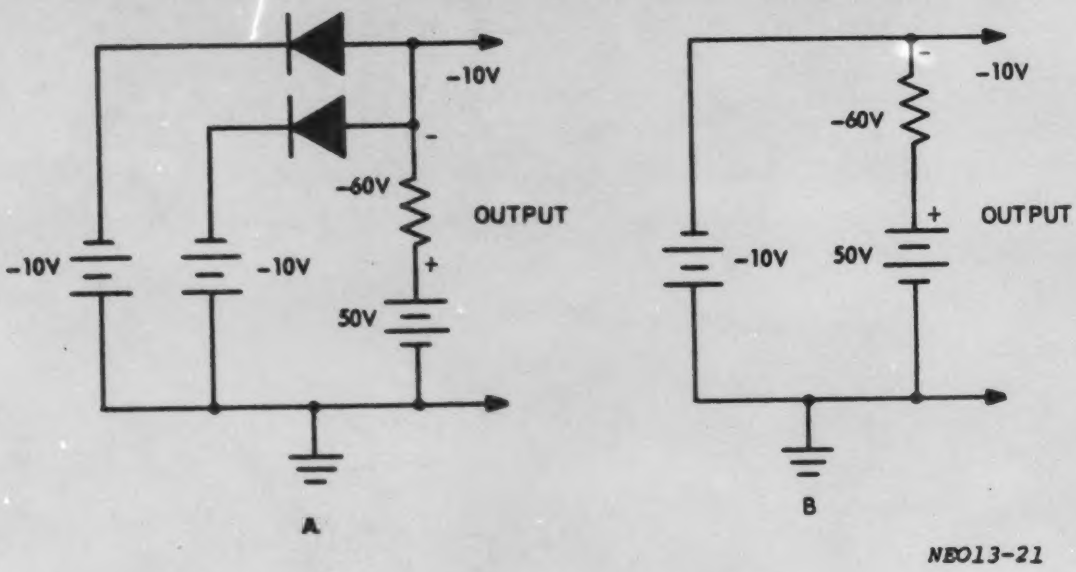

-10V
-60V
OUTPUT
-10V
-10V
50V
A
-10V
-60V
OUTPUT
-10V
50V
B
NEO13-21

Figure 2-48. Diode gate with both inputs - 10 volts.

diode to the output. The operation of the circuit depends upon the voltage drop across load resistor RL which, in this case, is connected to a positive voltage source. More inputs can be added, although only two are shown.

5-7. Let us assume, for the explanation of the circuit shown in figure 2-47, that the logic levels are 0 volts and - 10 volts. It should be remembered that different computers use different logic level voltages to represent information.

5-8. The circuit in figure 2-48,A, shows - 10 volts being applied to both inputs. In this circuit, both diodes are conducting; thus, both act as a short circuit for current. The output is therefore - 10 volts with respect to ground for this condition. Figure 2-48,B,

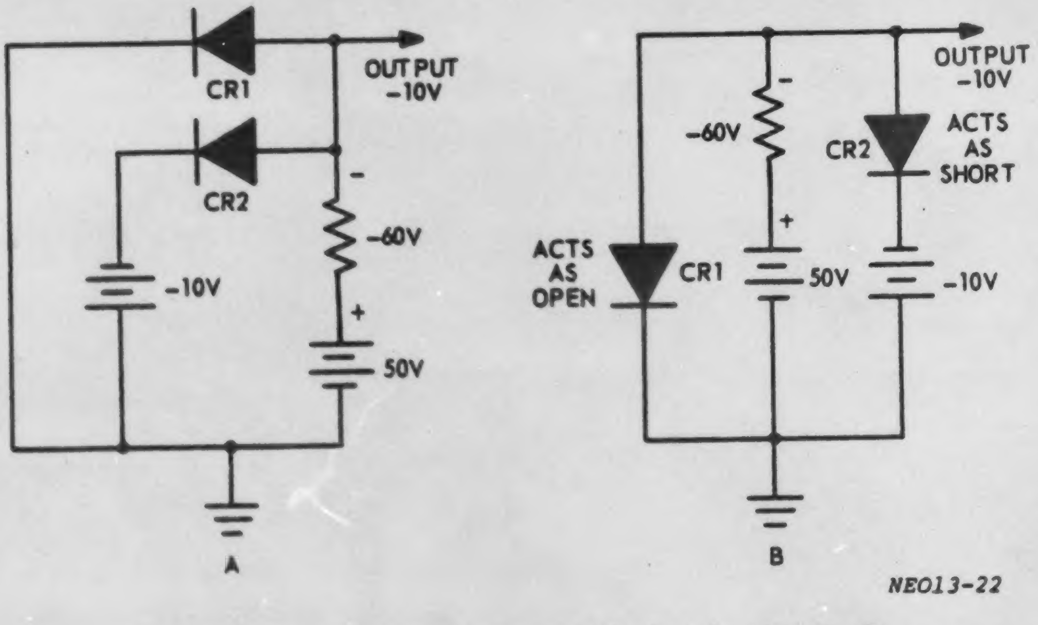
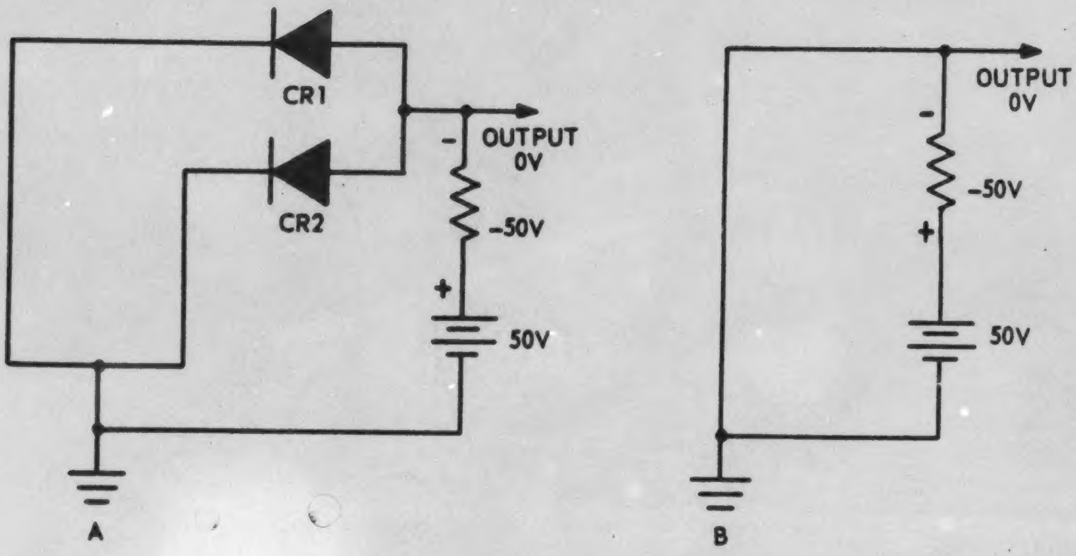

CR1
OUTPUT
-10V
CR2
-60V
-10V
50V
A
OUTPUT
-10V
-60V
ACTS
AS
SHORT
CR2
ACTS
AS
OPEN
CR1
50V
-10V
B
NEO13-22

Figure 2-49. Diode circuit with one input - 10 volts and one input 0 volts.



NEO13-23

Figure 2-50. Diode circuit with both inputs 0 volts.

shows the equivalent circuit with both diodes acting as shorts and both batteries replaced by one - 10-volt battery.

5-9. Figure 2-49,A, shows the same circuit with one input at 0 volts and the other at - 10 volts. The initial difference in potential across CR2 is 60 volts, since the 50-volt source and the 10-volt source are now connected in series aiding. Thus, CR2 conducts and puts the anode of CR1 at - 10 volts with respect to ground. This causes CR1 to act as an open, and the output is - 10 volts for this condition. Figure 2-49,B, shows the circuit in simplified form.

5-10. If the - 10-volt input is applied to CR1 and the 0-volt input is applied to CR2, the conditions are reversed. That is, CR1 conducts and puts the anode of CR2 at - 10 volts. This causes CR2 to act as an open. The output is - 10 volts for this condition also.

5-11. When the - 10 volts is applied to either input and 0 volts applied to the other, the conducting diode shorts out the open circuit. The result is an output of - 10 volts in either case.

5-12. Figure 2-50,A, shows the same circuit used in figure 2-49 with both inputs at 0 volts. Both diodes are conducting, thus acting as short circuits. For this condition, the output is 0 volts.

5-13. From the preceding discussion, it is possible to set up the *device activity states* or

TABLE 2-3
DEVICE ACTIVITIES STATES FOR CIRCUIT IN FIGURE 2-47

Inputs		Outputs
A	B	C
-10v	-10v	-10v
-10v	0v	-10v
0v	-10v	-10v
0v	0v	0v

NDA6-40

TABLE 2-4
ACTIVITY COMBINATIONS FOR CIRCUIT IN FIGURE 2-47

Inputs		Outputs
A	B	C
L	L	L
L	H	L
H	L	L
H	H	H

NDA6-38

TABLE 2-5
TRUTH TABLE FOR CIRCUIT IN FIGURE 2-47 USING POSITIVE LOGIC

Inputs		Outputs
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

NDA6-37

electrical truth table for the circuit in figure 2-47. This is shown in table 2-3. Refer to figure 2-47 to verify the truth table.

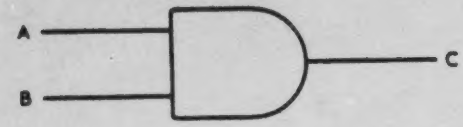
14. In computer terminology, a high (H) is the less negative, or more positive, logic level. A low (L) is the more negative, or less positive, logic level. For example, in the preceding discussion of the diode logic gate, 0 volts is the high (H) and - 10 volts is the low (L). In table 2-3, substitute H for the high (0 volts) and L for the low (- 10 volts); then the activity combinations table for the circuit will be shown in table 2-4.

5-15. Remember, in the discussion of information signals, that a computer may use either extreme of the logic levels to represent a binary 1 or a binary 0. The voltage level which represents one of the digits may become reversed in some of the circuits during the handling operation. This is not objectionable as long as the operation remains logical and consistent, and the desired end result is obtained. If a relatively high-voltage level represents a binary 1, the logic is referred to as *positive logic*. If a relatively low-voltage level represents a binary 1, the logic is referred to as *negative logic*.

TABLE 2-6
TRUTH TABLE FOR CIRCUIT IN FIGURE 2-47 USING NEGATIVE LOGIC

Inputs		Outputs
A	B	C
1	1	1
1	0	1
0	1	1
0	0	0

NDA6-42



NEO13-24

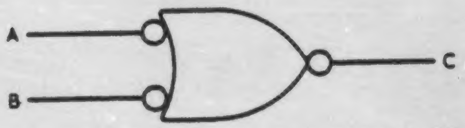
Figure 2-51. Symbol for positive AND-gate.

5-16. For the diode logic gate in figure 2-47, the 0-volt level is assigned the binary value 1, and the - 10-volt level is assigned the binary value 0. The circuit is using positive logic, and it is now possible to write a truth table for the circuit by substituting 1 for 0 volts and 0 for - 10 volts. Table 2-5 shows this truth table.

5-17. From truth table 2-5, you can see that the circuit in figure 2-47 performs the AND function. That is, all of the inputs must be 1 to obtain an output of 1. Since the high-voltage level represents a binary 1, the function performed is called the positive AND function, and the circuit is a positive AND-gate. The gate in figure 2-47 is symbolized by the standard logic symbol for the positive AND function, as shown in figure 2-51. The Boolean equation for this gate is AB = C.

5-18. Consider the same circuit when a - 10-volt level is assigned the binary value 1 and a 0-volt level is assigned the binary value 0, i.e., negative logic. The truth table for this condition is shown in table 2-6.

5-19. From truth table 2-6, you can see that the circuit now performs the OR function. That is, the output is 1 if any input or all outputs are 1. Since the low-voltage level represents binary 1, the function performed is called the negative OR function



NEO13-25

Figure 2-52. Symbol for negative OR-gate.

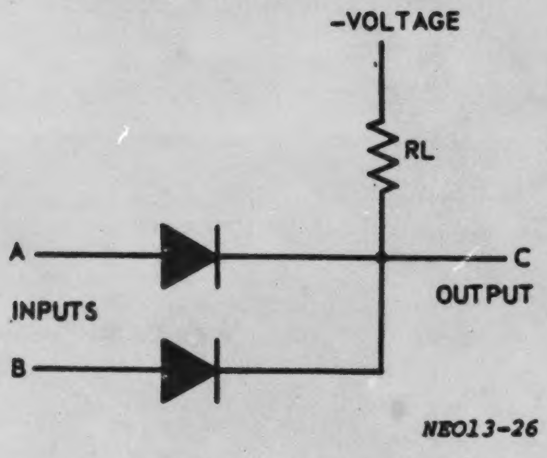


Figure 2-53. Diode positive OR-gate or negative AND-gate.

and the circuit is a negative OR-gate. The gate is symbolized by the standard logic symbol shown in figure 2-52. The Boolean equation for the gate is A + B = C.

5-20. The small circle(s) at the input to any symbol element (logical or nonlogical) indicate(s) that the relatively low (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively high (H) input signal activates the function. A small circle at the symbol output side indicates that the output terminal of the activated function is relatively low (L).

5-21. From the foregoing discussion, you can see that a single circuit may be caused to perform either the AND function or the OR function. The function that it performs depends upon the assignment of the logic levels. The circuit that you have just studied may be used as a positive AND-gate or a negative OR-gate.

5-22. *Diode positive OR-gate or negative AND-gate.* We have discussed a diode logic gate that is capable of performing both the positive AND and the negative OR function. In contrast, the gate shown in figure 2-53 performs both the positive OR and the negative AND functions.

5-23. How does the circuit in figure 2-53 differ from the circuit in figure 2-47? First, in figure 2-53, load resistor RL is connected to a negative power source, and, second, the cathodes of the diodes are connected to the load resistor.

5-24. Again, for explanation of the circuit in figure 2-53, we assume that the logic levels are 0 volts and -10 volts. Figure 2-54,A, shows the circuit with -10 volts applied to both inputs. Both diodes are conducting, thus acting as short circuits for current. Therefore, the output is -10 volts for this condition.

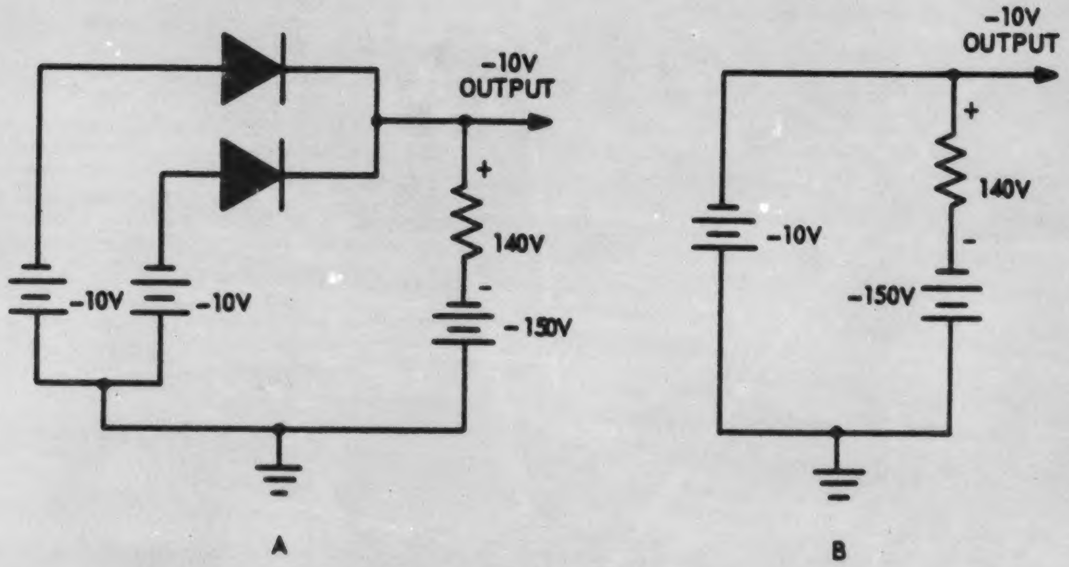
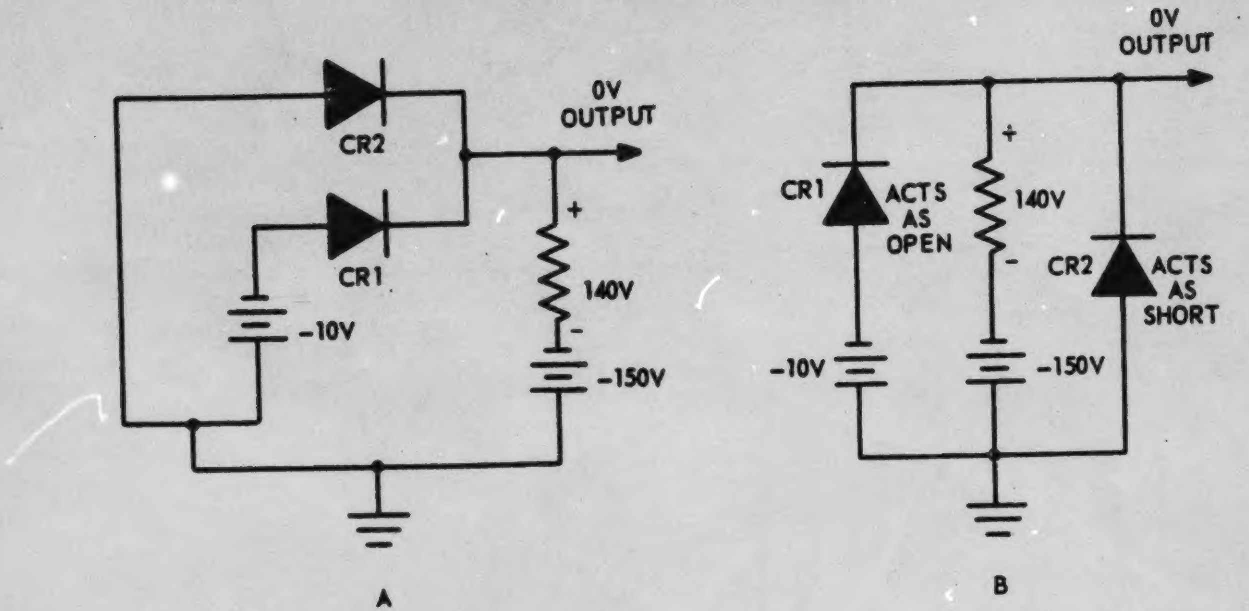
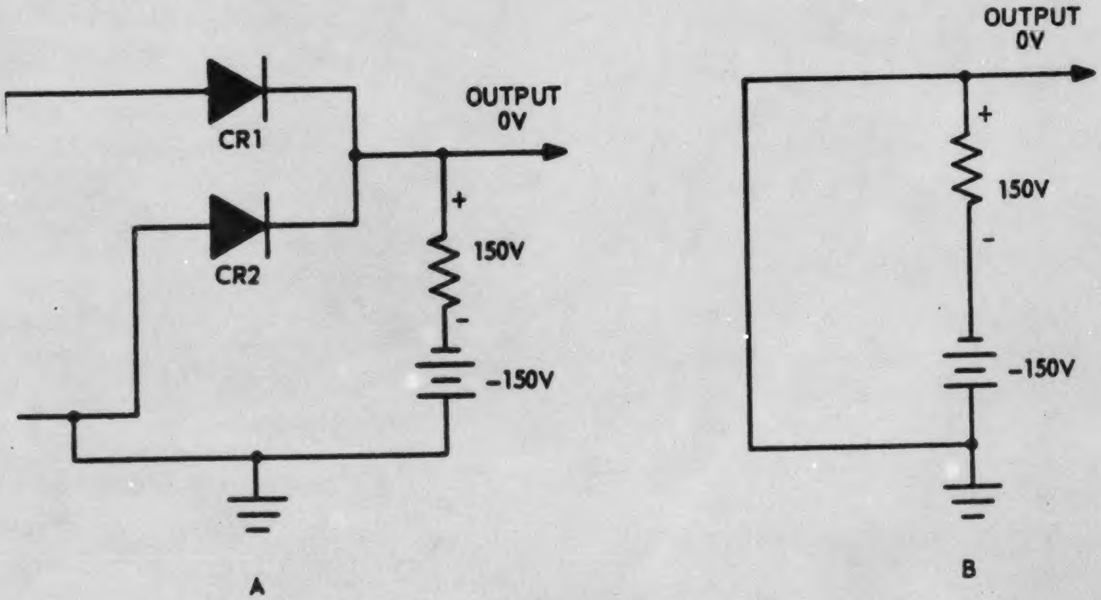


Figure 2-54. Positive OR/negative AND circuit with both inputs -10 volts.


CR2
CR1
-10V
0V
OUTPUT
+
140V
-
-150V
A
0V
OUTPUT
+
CR1
ACTS
AS
OPEN
140V
-
CR2
ACTS
AS
SHORT
-10V
-150V
B

NDA6-59

Figure 2-55. Positive OR/negative AND circuit with one input 0 volts and one input -10 volts.


CR1
CR2
OUTPUT
0V
+
150V
-
-150V
A
OUTPUT
0V
+
150V
-
-150V
B

NEO13-29

Figure 2-56. Positive OR/negative AND circuit with both inputs 0 volts.

TABLE 2-7
DEVICE ACTIVITY STATES FOR CIRCUIT IN FIGURE 2-53

Inputs		Outputs
A	B	C
-10v	-10v	-10v
-10v	0v	0v
0v	-10v	0v
0v	0v	0v

NDA6-43

Figure 2-54,B, shows the equivalent circuit with both diodes acting as shorts and both input batteries replaced by one -10-volt battery.

5-25. Figure 2-55,A, shows the same circuit with one input at 0 volts and the other at -10 volts. The anode of CR1 has -10 volts applied to it, and the anode of CR2 has 0 volts applied to it. This means that initially, across CR2, there is a 150-volt difference, while across CR1 there is a 140-volt difference. CR2 conducts and shorts the output to 0 volts. This shorting action causes 0 volts to be felt on the cathode of CR1. The -10 volts in series with CR1 causes it to be biased in its high-impedance direction. Since the cathode of CR1 is positive with respect to the anode, it does not conduct. Thus, CR1 acts as an open circuit and the output of the circuit remains at 0 volts. This condition is shown in figure 2-55,B.

TABLE 2-8
ACTIVITY COMBINATIONS FOR CIRCUITS IN FIGURE 2-53

Inputs		Outputs
A	B	C
L	L	L
L	H	H
H	L	H
H	H	H

NDA6-33

TABLE 2-9
TRUTH TABLE FOR CIRCUIT IN FIGURE 2-53 USING POSITIVE LOGIC

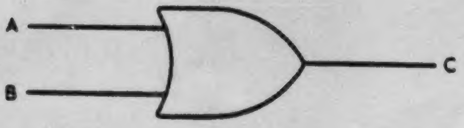
Inputs		Outputs
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

NDA6-34

5-26. If the -10-volt input is applied to CR2 and the 0-volt input is applied to CR1, the conditions are reversed. That is, CR1 conducts and puts the cathode of CR2 at 0 volts, and again the output of the circuit is 0 volts. Figure 2-56,A and B, shows the same circuit with both input levels at 0 volts. Both diodes conduct, and the output is 0 volts.

5-27. From the preceding discussion, it is possible to set up the device activity states or electrical truth table for the circuit in figure 2-53. This information is shown in table 2-7. Substituting the high (H) for 0 volts and the low (L) for the -10 volts results in the activity combinations for this diode logic circuit shown in table 2-8.

5-28. Consider the diode circuit in figure 2-53 when the 0-volt level is assigned the logic value 1 and activates the circuit, and the -10-volt level is assigned the logic value 0 and is the inactive level; i.e., positive logic. Substitution of these values in table 2-8 results in the truth table shown in table 2-9.



NEO13-30

Figure 2-57. Symbol for positive OR-gate.

TABLE 2-10

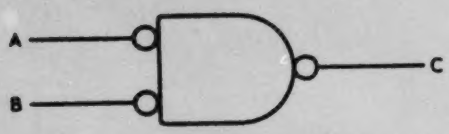
TRUTH TABLE FOR CIRCUIT IN FIGURE 2-53 USING NEGATIVE LOGIC

Inputs		Outputs
A	B	C
1	1	1
1	0	0
0	1	0
0	0	0

NDA6-41

5-29. From truth table 2-9, you can see that the circuit performs the OR function. That is, the output is 1 if any or all of the inputs are 1. Since the high-voltage level represents binary 1, the circuit performs the positive OR function and is called a positive OR-gate. The gate is symbolized by the standard logic symbol for the positive OR function, as shown in figure 2-57. The Boolean equation for the gate is A + B = C.

5-30. Consider the same circuit when the -10-volt level is assigned the logic value of 1 and is the activating signal, and the 0-volt level is assigned the logic value of 0 and is the inactive level. The truth table for this condition is shown in table 2-10.



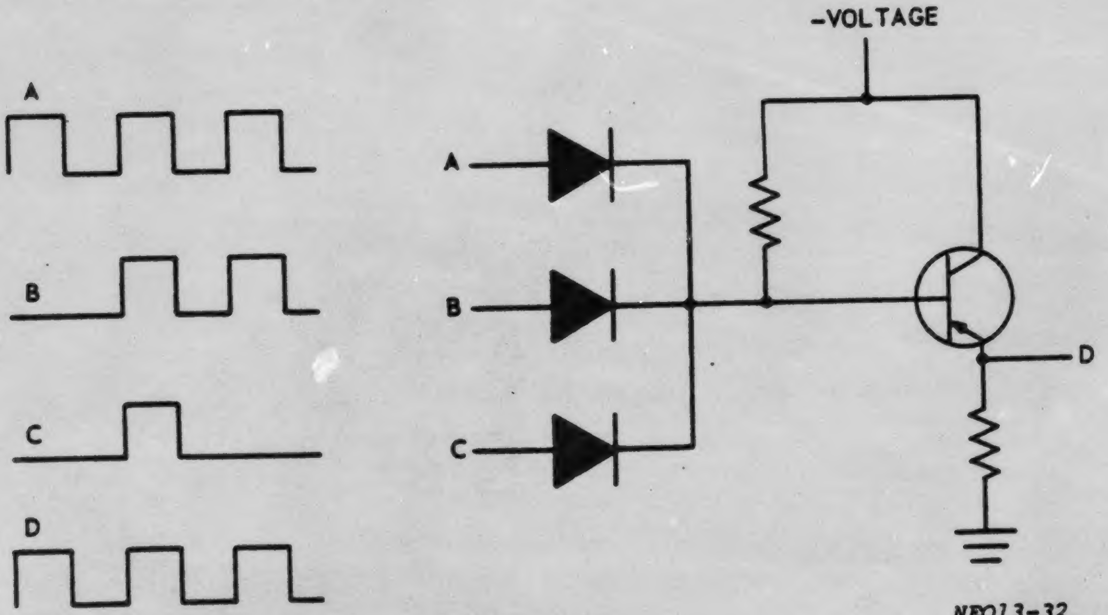
NEO13-31

Figure 2-58. Symbol for negative AND-gate.

5-31. From table 2-10, you can see that the circuit now performs the AND function. That is, all the inputs must be 1 to obtain an output of 1. Since the low-voltage level represents binary 1, the function performed is called the *negative AND function* and the circuit is a negative AND-gate. A negative AND-gate is symbolized by the standard logic symbol shown in figure 2-58. The Boolean equation for the gate is AB = C.

5-32. Again, a single circuit may perform either the OR function or the AND function. The function that it performs depends upon the assignment of logic levels. The circuit that you have just studied may be used as a positive OR-gate or a negative AND-gate.

5-33. *Transistor Logic Gates.* Computers also use transistor gate circuits to perform



NEO13-32

Figure 2-59. Diode-and-transistor logic (DTL) circuit.

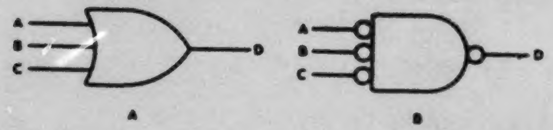


Figure 2-60. Logic symbols for circuit in figure 2-59.

logical functions. Transistors have the ability to amplify and are used to keep a signal constant through several gates. Transistors may be connected in series, parallel, or series-parallel to provide the logical functions of a computer.

5-34. There are several types of transistor logic circuits which are used for logic gates. The type used will depend upon the power requirements, switching speeds, and cost. These are the basic transistor logic circuits:

- Diode-and-transistor combination logic (DTL).
- Resistor-transistor logic (RTL).
- Direct-couples transistor logic (DCTL).

5-35. *Diode-and-transistor logic gates.* As we stated before, the diode logic gate does not amplify the signal; therefore, to keep the amplitude constant, a transistor is added to the output of the diode gate. Figure 2-59 shows a transistor used for this purpose. The diode gate and the transistor circuit (an emitter-follower) make up the logic network. From the input and output waveforms, you can see that the output of the logic network is low only when all of the inputs are low and is high when one or all of the inputs are high. Therefore, it is a positive OR-gate or a negative AND-gate. Figure 2-60,A, is the symbol for the positive OR-gate, and figure 2-60,B, is the symbol for the negative AND-gate. Figure 2-61 illustrates the same type circuit used as a positive AND-gate or negative OR-gate. The logic symbols for this circuit are shown in figure 2-62. Figure 2-62,A, is the symbol for the positive AND-gate, and figure 2-62,B, is the symbol for the negative OR-gate.

5-36. Instead of using the emitter-follower as the output stage, a common-emitter or inverter circuit may be used. This circuit is shown in figure 2-63. The circuit is an inverted positive OR-gate or an inverted negative AND-gate. The logic symbols for this gate are shown in figure 2-64. Figure 2-64,A, is the symbol for the inverted positive OR-gate, and figure 2-64,B, is the symbol for the inverted negative AND-gate.

5-37. Figure 2-65 shows the same type circuit used as an inverted positive AND-gate or an inverted negative OR-gate. The logic symbols for this gate are shown in figure 2-66. Figure 2-66,A, is the symbol for the inverted positive AND-gate, and figure 2-66,B, is the symbol for the inverted negative OR-gate.

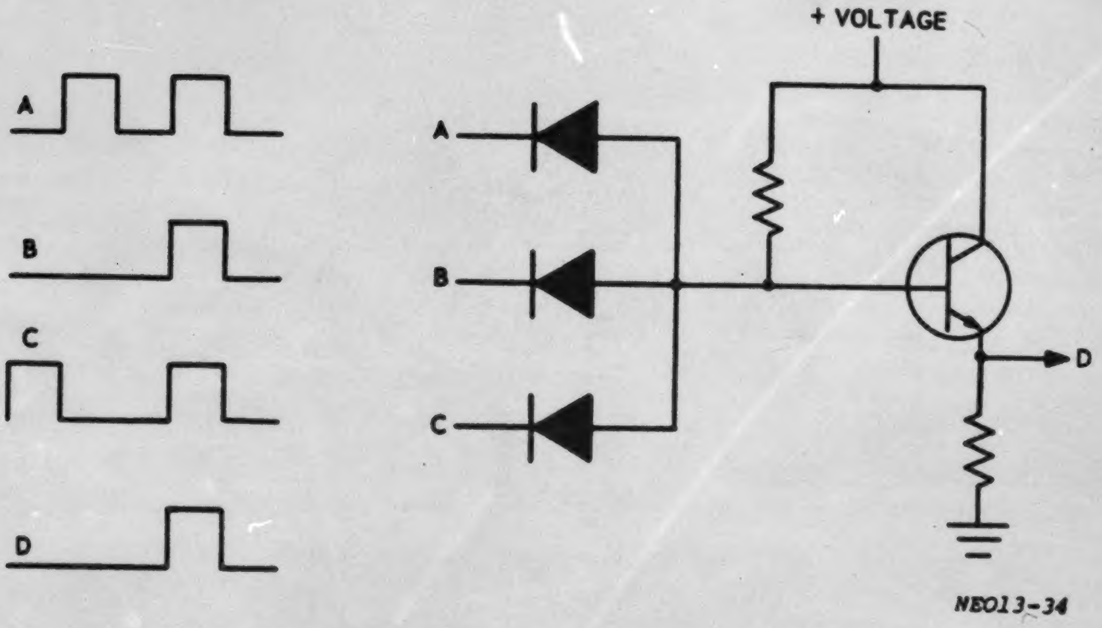
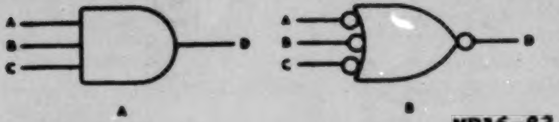


Figure 2-61. Positive AND-gate or negative OR-gate circuit (DTL).



NDA6-83

Figure 2-62. Logic symbols for circuits in figure 2-61.

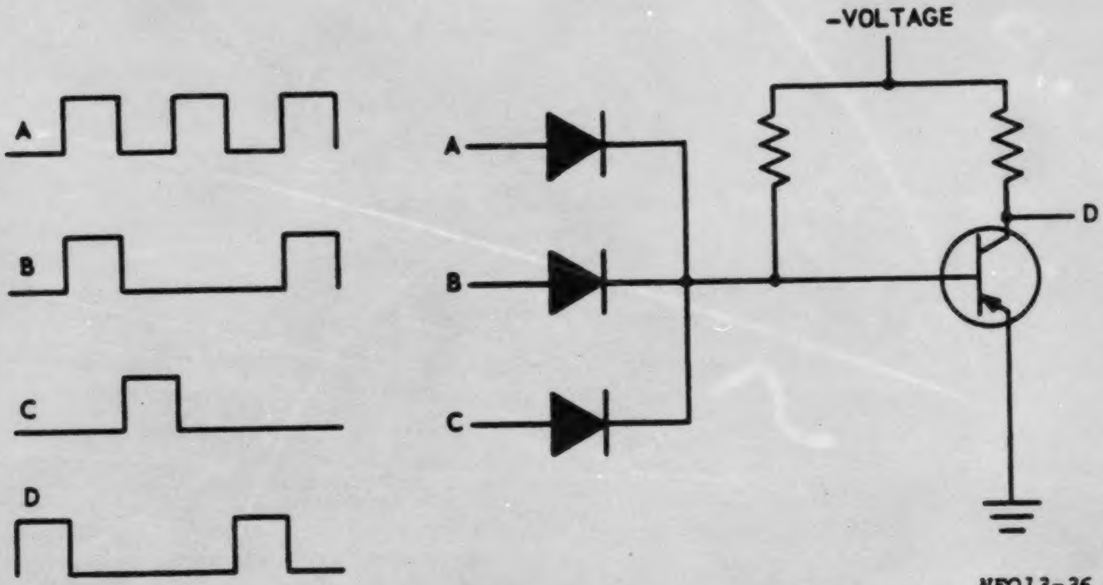
5-38. An AND-gate whose output signal is inverted with respect to the input signals is called a *NOT-AND-gate* or *NAND-gate*. The circuits shown in figures 2-63 and 2-65 are examples of NAND-gates. The logic symbols for the NAND-gates are the same as those shown in figures 2-64,B, and 2-66,A.

5-39. An OR-gate whose output signal is inverted with respect to the input signal is called a *NOT-OR-gate* or *NOR-gate*. The circuits shown in figures 2-63 and 2-65 are examples of NOR-gates. Notice that these are the same circuits as the NAND-gates. The function the circuit performs depends upon the logic level used to represent 1. The logic symbols for the NOR-gates are the same as those shown in figures 2-64,A, and 2-66,B.

5-40. *Resistor-transistor logic (RTL) gates.* A resistor-transistor logic circuit is made up of a resistor gate and an inverting amplifier. Figure 2-67 shows this type of circuit. Resistors R1, R2, and R3 are of equal value. The logic levels are assumed to be 0 volts and -2 volts. If all the inputs are at the upper level, or 0 volts, the transistor will not conduct. The resistor values are such that, if one input is at the lower level of -2 volts, the transistor is driven into the saturation region. If more than one input is at the lower level, the transistor is driven more into saturation. The output is inverted through the transistor. This circuit performs the negative OR function or the positive AND function with an inverted output. The logic symbols for the gate are shown in figure 2-66. Note that the logic symbols are the same for this circuit as for the circuit in figure 2-65.

5-41. To perform the positive OR function or negative AND function with inversion, the circuit shown in figure 2-68 may be used. If any of the inputs are at the upper level, the transistor conducts. The resistors perform the OR function, while the transistor amplifies and inverts. The logic symbols for the circuit are shown in figure 2-64. Here again, we have two different circuits, shown in figures 2-63 and 2-68, with the same symbols.

5-42. Some resistor-transistor logic circuits require the addition of RL networks, speedup



NEO13-36

Figure 2-63. Common-emitter diode-and-transistor circuit.

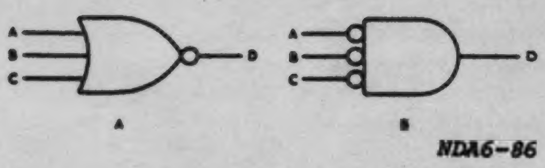


Figure 2-64. Logic symbols for circuits in figures 2-63, 2-65, and 2-72.

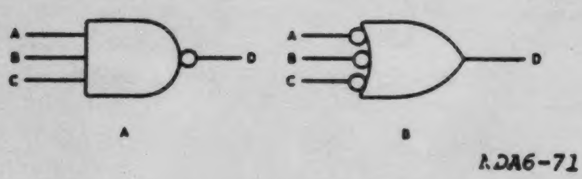


Figure 2-66. Logic symbols for circuits in figures 2-65, 2-67, and 2-69.

capacitors, and diodes to make them work at high frequencies. Therefore, they are more complicated, less economical, and less efficient than diode logic circuits at these frequencies. However, when used with good high-frequency transistors, they are useful in high-speed computers.

5-43. *Direct-coupled transistor logic (DCTL) gates.* Direct-coupled transistor logic, as its name implies, uses direct coupling to transfer a logic voltage level from one transistor to another. Since these circuits use only transistors and resistors, their frequency response is excellent. Logical functions can be performed with small voltage changes when DCTL circuits are used. The voltage swings may be as low as 0.2 or 0.3 volt. No level-restoring circuitry, such as diode limiters, is needed since the DCTL circuit sets the upper and lower voltage levels.

5-44. A parallel DCTL gate is illustrated in figure 2-69. This gate has three transistors connected in parallel in a common-emitter configuration. If all three inputs (A, B, and C) are high, the output at D is low. However, if any one of the three inputs is low, the output becomes high. From these facts, you can see that the gate is either a positive input AND-gate with inversion or a negative input OR-gate with inversion. The logic symbols for this gate are shown in figure 2-66.

5-45. If inversion is not desired, an inverter-amplifier may be added to the circuit. More transistors can be placed in parallel to provide more inputs, but there is a limit to the number because the sum of the leakage currents, I_{CO}, will increase to a point where the output voltage remains too close to the high-logic level.

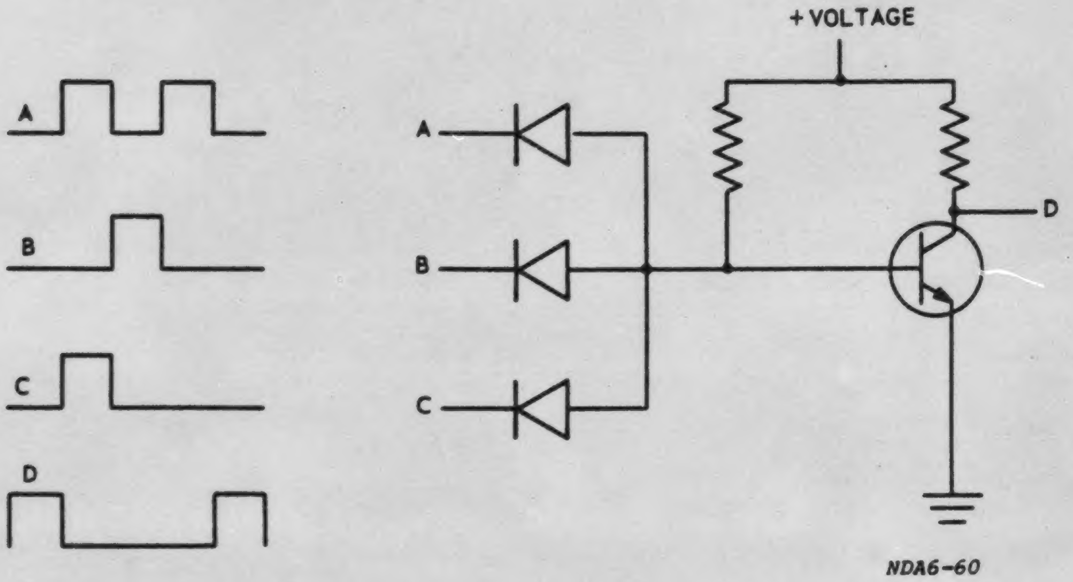


Figure 2-65. Inverted positive AND or negative OR logic circuit.

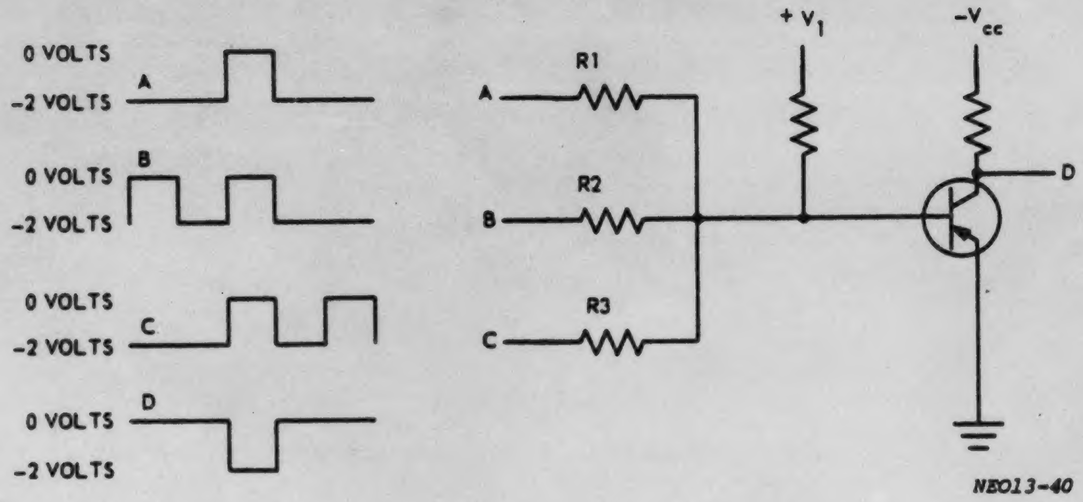

0 VOLTS
-2 VOLTS
A
B
C
D
R1
R2
R3
+V1
-Vcc
NE013-40

Figure 2-67. Resistor-transistor logic (RTL) circuit.

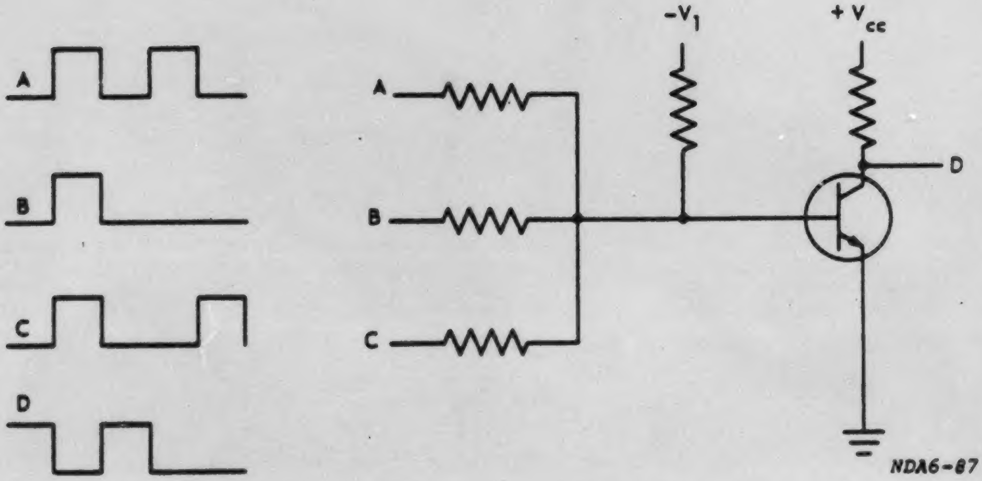

A
B
C
D
-V1
+Vcc
NDA6-87

Figure 2-68. Positive OR/negative AND circuit with inversion.

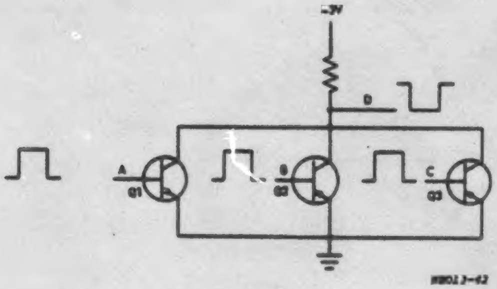


Figure 2-69. Parallel DCTL gate.

5-46. A series DCTL gate consisting of two transistors in series is illustrated in figure 2-70. If the inputs (A and B) are relatively high, the output is low. If either input is low, the output is still low. If both inputs are low, the output is high. From these facts, you can see that the series gate is either a positive input OR-gate with inversion or a negative input AND-gate with inversion. The logic symbols for this gate are shown in figure 2-71. Figure 2-71,A, is the symbol for the positive input OR-gate with inversion, and figure 2-71,B, is the symbol for the negative input AND-gate with inversion.

5-47. Again, if inversion is not desired, an inverter-amplifier may be added to the circuit. More transistors may be placed in series, but there is a limit to the number because the voltage drops across the transistors add together and reduce the voltage swing of the output.

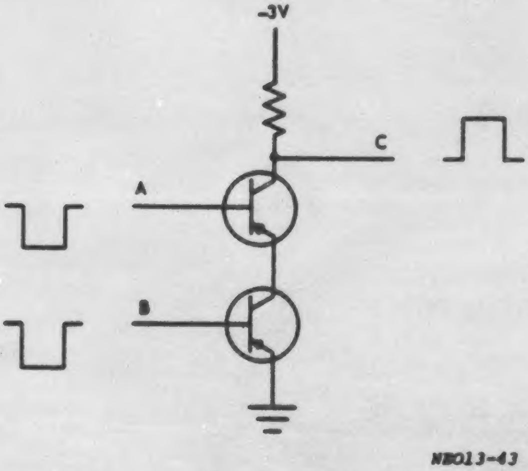


Figure 2-70. Series DCTL gate.

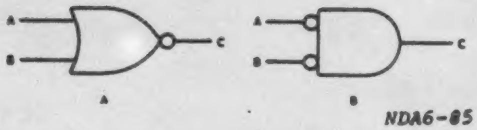


Figure 2-71. Logic symbols for series DCTL gate shown in figure 2-70.

5-48. The direct-coupled transistor logic circuit is simple and has low-power consumption. It also has disadvantages. The transistors and resistors must be kept within close tolerances. Noise voltages increase as the number of transistors increases. If many transistors are used, noise voltages are a problem. Since the transistors are operated at saturation, the switching speed is limited.

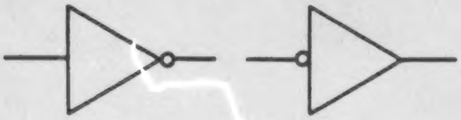


Figure 2-72. Logic symbols for an inverter or NOT circuit.

5-49. *NOT Circuits.* A circuit that inverts the logic of a pulse or group of pulses is called a NOT circuit and is usually a simple inverter. A plate-loaded triode or a grounded emitter transistor amplifier constitutes a NOT circuit. A NOT circuit is frequently used to advantage in conjunction with other switching gates to change the polarity of the signal.

5-50. Refer to figures 2-63 and 2-65. These circuits use grounded emitter transistor amplifiers to invert the outputs of the diode gates. In these cases, the amplifier part of the circuit is the NOT circuit. The logic symbols for an inverter or NOT circuit are shown in figure 2-72.

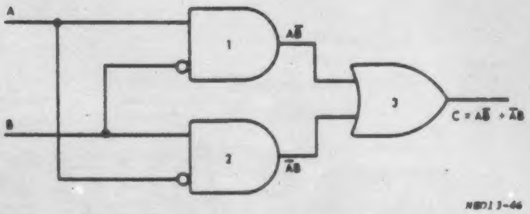


Figure 2-73. Exclusive OR circuit.

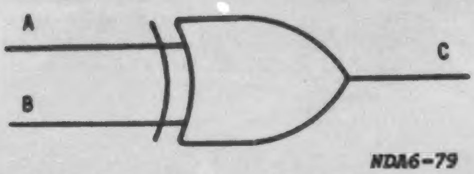


Figure 2-74. Logic symbol for exclusive OR-gate.

TABLE 2-11

TRUTH TABLE FOR EXCLUSIVE OR CIRCUIT

Inputs		Outputs
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

NDA6-32

5-51. Exclusive OR. The OR function produces a specified result when any one or all of the input conditions are satisfied. Since the OR includes all combinations as well as one-at-a-time inputs, it is called an *inclusive OR*. All of the circuits that have been discussed which perform the OR function have been inclusive OR-gates. In digital computer logic circuits, the OR function is always "inclusive" unless otherwise specified.

5-52. A logical operation that produces an output when either input is present, but not when both inputs are present, is called an exclusive OR. A combination of AND- and OR-gates may be arranged to perform this logical function. Such an arrangement is shown in figure 2-73. The logic symbol for an exclusive OR-gate is shown in figure 2-74.

5-53. The Boolean equation for an exclusive OR-gate is $A\overline{B} + \overline{A}B = C$. This says that C is present when A or B is present, but not when both are present. A truth table for this gate is shown in table 2-11.

CHAPTER 3

Computer Components

AS A COMPUTER repairman, you can expect to be exposed to several types of computer components—such as counters, storage registers, shift registers, decoders, converters, encoders, and comparators. A review of these components is presented in this chapter. The circuits that make up the computer components discussed here are not necessarily the same as those used in the computer system you are presently maintaining. However, you shouldn't have any problem in understanding their functional operation, because the majority of these circuits are similar to those you studied during your formal electronic and computer fundamental training.

NOTE: In our discussion of computer components, the figures presented are drawn with the least significant digit (LSD) component on either the left or right. You can easily determine its location by identifying the component in the figure that is activated by the input first. However, the binary number represented by a specific figure will always have the LSD written to the extreme right of the number.

1. Counters

1-1. The basic circuit used in most counters is a modified Eccles-Jordan bistable multivibrator. Recall in your previous studies of multivibrators that they were referred to as flip-flops (F/Fs). By connecting several F/Fs together and controlling the input signals with gates, we can design a circuit that performs a counting operation in the binary number system. As such, they are referred to as binary counters. A binary counter is a device capable of counting according to the binary system and recording the number of events which have occurred. They are used to facilitate converting pulse information into a usable form within digital data processors and computers. Some of their many uses include:

- Counting and keeping track of program steps.
- Counting time (seconds, minutes, and hours).
- Providing a means of timing various units such as a memory or arithmetic unit.

1-2. Classification of Counters. Counters are classified by both *circuit design and function*. The two classifications of circuit design are *serial* and *parallel*. The two functional classifications are *up-counters* and *down-counters*. Counters are composed of F/Fs and gates connected so that each F/F represents one place position in a binary number (2^0, 2^1, 2^2, etc.). Refer to figure 3-1 for a basic counter comprised of three F/Fs. The number of pulses required to recycle a counter is referred to as its *modulus* and is normally determined by the number of stages (flip-flops) in the counter. This number is 2^N, where N is equal to the number of stages in the counter. In our basic counter shown in figure 3-1, its modulus is eight because 2^3 (2^N) is equal to eight. In other words, if this three-stage counter were cleared (each F/F in its cleared state), it would take eight pulses to recycle the counter from 0 back to 0. Also, the maximum count of a counter is equal to $2^N - 1$. In the case of a three-stage binary counter, its maximum count is equal to $2^3 - 1$ or 7. These facts hold true for both parallel and serial counters.

1-3. Serial Counters. These are the simplest of counter configurations, and they are further designated as serial up-counters or serial down-counters. Each time the input is triggered (clocked) in a serial up-counter, the count in the counter is raised by one. Each time the input is triggered in a serial down-counter, the count is lowered by one. The advantage of serial counters is that minimum circuitry is required. The disadvantage is that they are slow when compared to parallel counters.

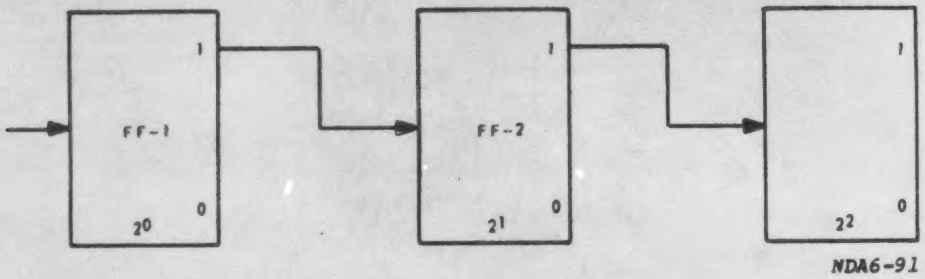


Figure 3-1. Basic counter.

1-4. The type of F/F used in the construction of a counter is one of the factors that determines the use of the leading (up-clock) or the lagging (down-clock) edge of the trigger input to the F/F. As each pulse is applied to the counter, the stage of one or more F/Fs is changed in such a way that the binary configuration represented by the counter indicates the number of input pulses received. Refer to figure 3-2 for an illustration of input clock pulses.

1-5. *Serial up-counter.* In a basic four-stage serial up-counter as shown in figure 3-3, each F/F represents a power of two. The counter has 16 different states, and with the application of each input pulse it makes a progressive transition from state to state. The sixteenth input pulse resets the counter to its original starting state. These features are easily recognized from the waveforms shown in the figure. Note that the F/Fs in this particular counter are triggered with a down-clock.

1-6. The output from each F/F in figure 3-3 is taken from the ONE side and fed to the trigger input of each succeeding F/F. Before the application of the first input, we'll assume that the counter is cleared (reset) to ZERO. When a down-clock is applied to F/F-A, it causes a transition from the ZERO to the ONE state. F/F-B is not affected, because it has felt an up-clock from F/F-A. The overall result is F/F-A has changed to the ONE state while all other F/Fs remain in the ZERO state. The binary count in the counter at this time is 0001 or 1. The second input pulse causes F/F-A to return to the ZERO state. F/F-B receives a down-clock from A and changes from the ZERO to the ONE state. The overall result of the application of the second pulse is F/F-B transitions to the ONE state, and all other F/Fs are in the ZERO state. The count in the counter is now 0010 or 2.

1-7. Table 3-1 shows the state of each F/F after a given number of input pulses. Note that the count in the counter corresponds to the number of input pulses. Thus, when seven pulses are inputted to the counter, F/Fs-A, -B, and -C are in the ONE state, while F/F-D remains in the ZERO state. This is the binary representation of 0111 or 7.

1-8. *Serial down-counter.* Normally, a serial down-counter is preset to a specific count, and as it is triggered the counter counts down from this preset configuration. Refer to figure 3-4 and note how the down-counter is wired as compared to the up-counter. That is, the output is taken off of the ZERO side instead of the ONE side. The waveforms (representing the SET-side output

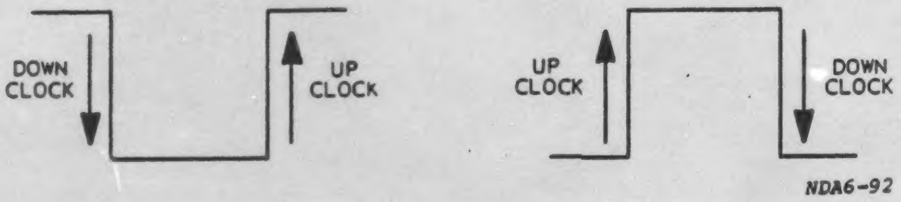
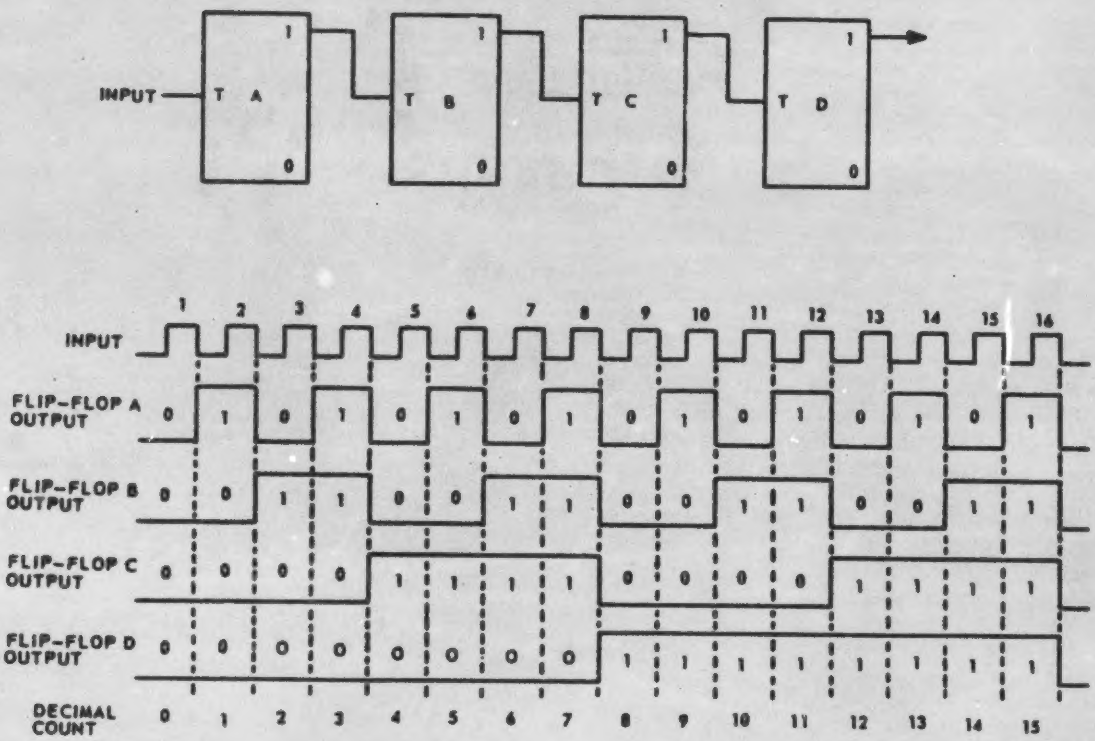


Figure 3-2. Up-clocks and down-clocks.



NDA6-93

Figure 3-3. Serial up-counter and waveshapes.

of the counter's F/Fs) indicate that when a F/F makes a transition from the ZERO state to the ONE state, the ONE-side output up-clocks and the ZERO-side output down-clocks. In our down-counter, the down-clock from the ZERO-side output of a F/F causes a transition in the F/F to which it is connected.

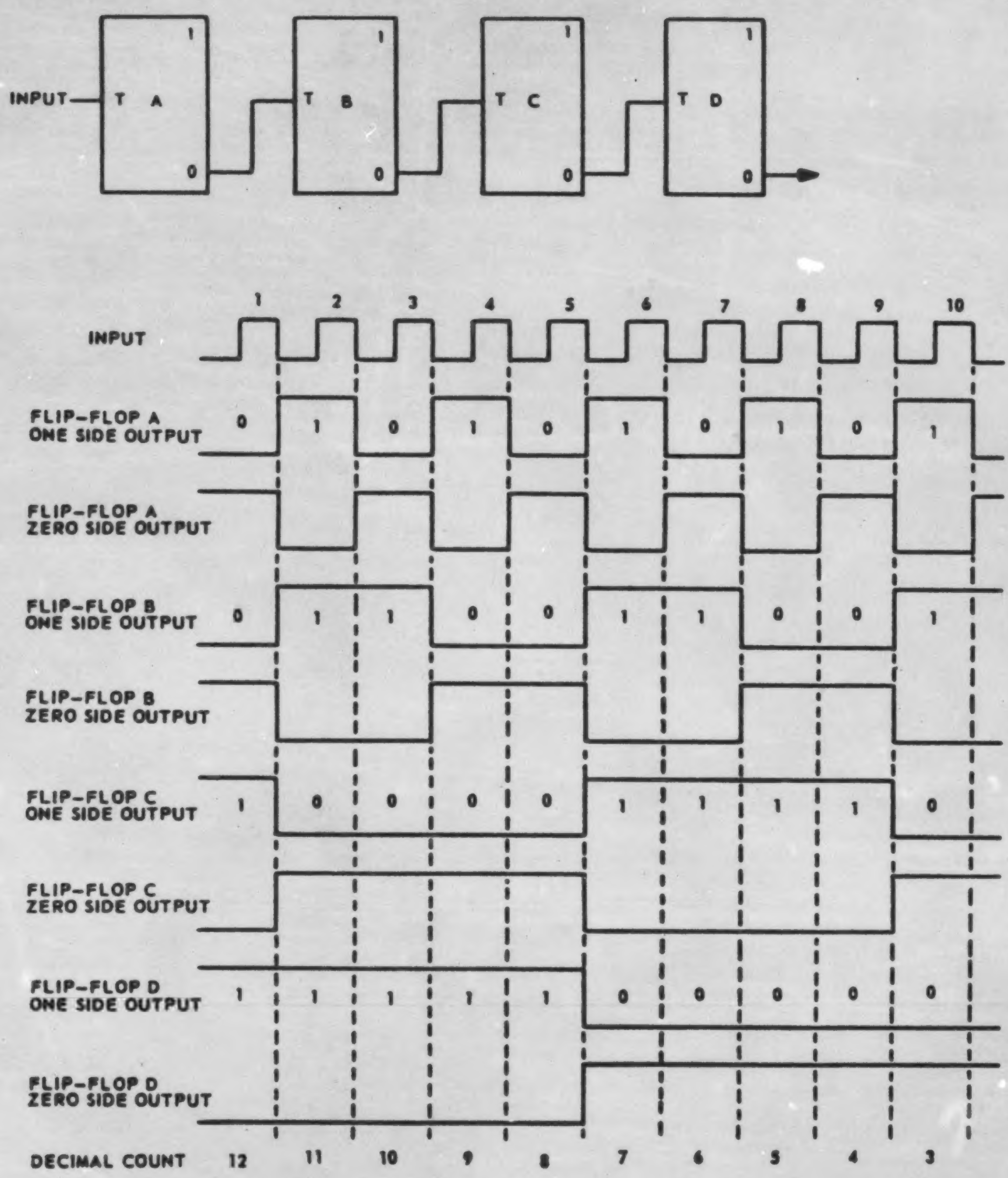
TABLE 3-1
EQUIVALENT NUMBERS IN DECIMAL AND BINARY NOTATION

NUMBER OF INPUT PULSES	STATE OF FLIP-FLOP			
	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1 = MAXIMUM COUNT
16	0	0	0	0 = RESET
17	1	0	0	0 = COUNT STARTS OVER

NDA6-88

1-9. Consider our down-counter in figure 3-4 as being preset to a binary count of 1100 (12 decimal). The waveforms indicate F/Fs-A and -B are in the ZERO state, and F/Fs-C and -D are in the ONE state. On the down-clock of the first input pulse, F/F-A transitions to the ONE state, B transitions to the ONE state, C transitions to the ZERO state, and F/F-D remains in the ONE state. The counter now contains the binary count of 1011 (11 decimal). Since the original number was equal to 12 decimal, it is obvious that the counter down-counted by ONE. Check the waveforms for our down-counter and note that the counter reaches a count of ZERO with the reception of the twelfth trigger's down-clock.

1-10. *Speed limitation of serial counters.* You will find many serial counters used in equipment in your career ladder. For the most part, they are used when a clock-pulse rate is relatively low. To count high-clock rates, the parallel counter is used, since the parallel counter eliminates the problem of *propagation time* (time delay through a series of stages).


INPUT
T A
T B
T C
T D
1
0
1 2 3 4 5 6 7 8 9 10
INPUT
FLIP-FLOP A ONE SIDE OUTPUT
0 1 0 1 0 1 0 1 0 1
FLIP-FLOP A ZERO SIDE OUTPUT
FLIP-FLOP B ONE SIDE OUTPUT
0 1 1 0 0 1 1 0 0 1
FLIP-FLOP B ZERO SIDE OUTPUT
FLIP-FLOP C ONE SIDE OUTPUT
1 0 0 0 0 1 1 1 1 0
FLIP-FLOP C ZERO SIDE OUTPUT
FLIP-FLOP D ONE SIDE OUTPUT
1 1 1 1 1 0 0 0 0 0
FLIP-FLOP D ZERO SIDE OUTPUT
DECIMAL COUNT
12 11 10 9 8 7 6 5 4 3

NDA6-94

Figure 3-4. Serial down-counter.

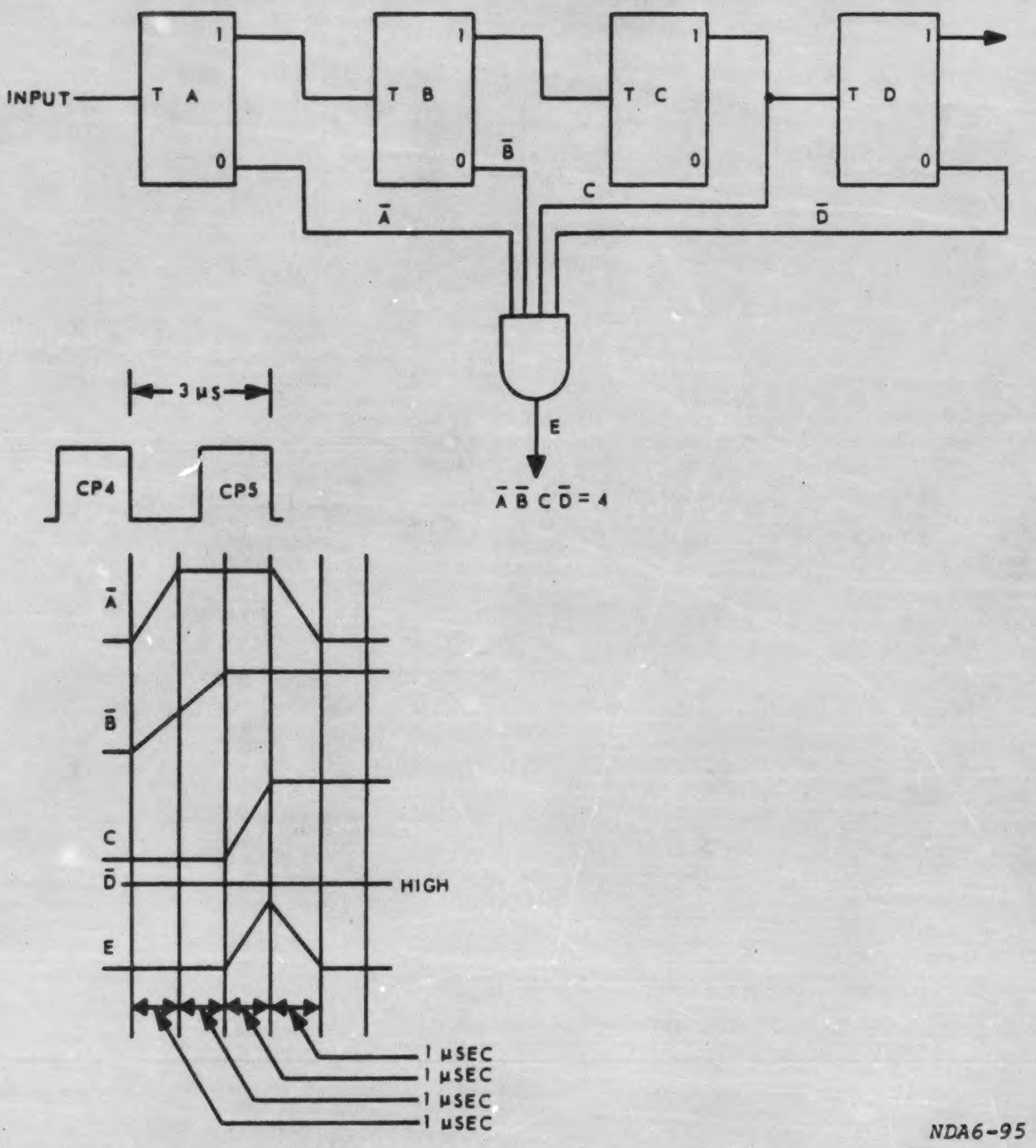

INPUT
T A
1
0
T B
1
0
T C
1
0
T D
1
0
$\overline{B}$
C
$\overline{A}$
$\overline{D}$
E
$\overline{A}\,\overline{B}\,C\,\overline{D} = 4$
3 μS
CP4
CP5
$\overline{A}$
$\overline{B}$
C
$\overline{D}$
HIGH
E
1 μSEC
1 μSEC
1 μSEC
1 μSEC
NDA6-95

Figure 3-5. Count detection.

1-11. To understand why the serial counter is too slow, look at figures 3-3 and 3-5. In figure 3-3, the waveforms are idealized; that is, the F/Fs are shown changing state instantaneously. This is not true, since some measurable time is required to flip a stage from one state to another. For explanation purposes, assume that the time between down-clocks of the input pulses is 3 μsec, and that it takes 1 μsec to change the state of a F/F. Locate input pulse 4 in figure 3-3. The down-clock of this pulse changes the count from 3 to 4, causing F/Fs-A, -B, and -C to change state. Since it requires 1 μsec to change the state of F/F-A and 1 μsec to change the state of F/F-B, F/F-C will receive the down-clock from F/F-B 1 μsec prior to the arrival of the next clock pulse (3 μsec - 2 μsec = 1 μsec). These facts are illustrated by the hypothetical waveforms shown in figure 3-5.

1-12. The computer component illustrated in figure 3-5 shows how a count of 4 ($\overline{AB}\,\overline{CD}$) could be detected by a positive AND-gate.

The waveforms in the figure also show that the HIGH output (E) from the AND-gate at the count of 4 is extremely narrow. This is caused by the propagation time established for our explanation. Note that the HIGH output from the AND-gate occurs just as the fifth input pulse down-clocks, and this same down-clock sets F/F-A which completely disables the AND-gate 1 μsec later. The short-time duration of the AND-gate's HIGH output is not normally a desirable feature.

1-13. Continuing our discussion of propagation time, refer to the waveforms in figure 3-3 again. At a count of 8, all F/Fs change state. Since F/F-D does not receive a down-clock until 3 μsec after the clock pulse, F/F-A could be triggered for count 9 (1001) before count 8 (1000) could be performed by the counter. As a result, count 8 would be missed. Again, this is caused by the propagation time. At the clock rate used in this explanation, and with F/Fs that require 1 μsec to change state, it is apparent that a limited number of F/F stages can be serially connected. The solution to this problem of propagation time is the use of a parallel counter.

1-14. **Parallel Counters.** An advantage of parallel counters over serial counters is speed in operation. This speed is a direct result of applying input trigger pulses, through gates, to each stage of the counter simultaneously. Consequently, more circuitry is required and more power is consumed in a parallel counter than in a serial counter. Parallel counters are also used as up-counters or down-counters.

1-15. *Parallel up-counter.* A basic three-stage parallel up-counter is illustrated in figure 3-6. For our discussion of its operation, we'll assume the counter is cleared and each

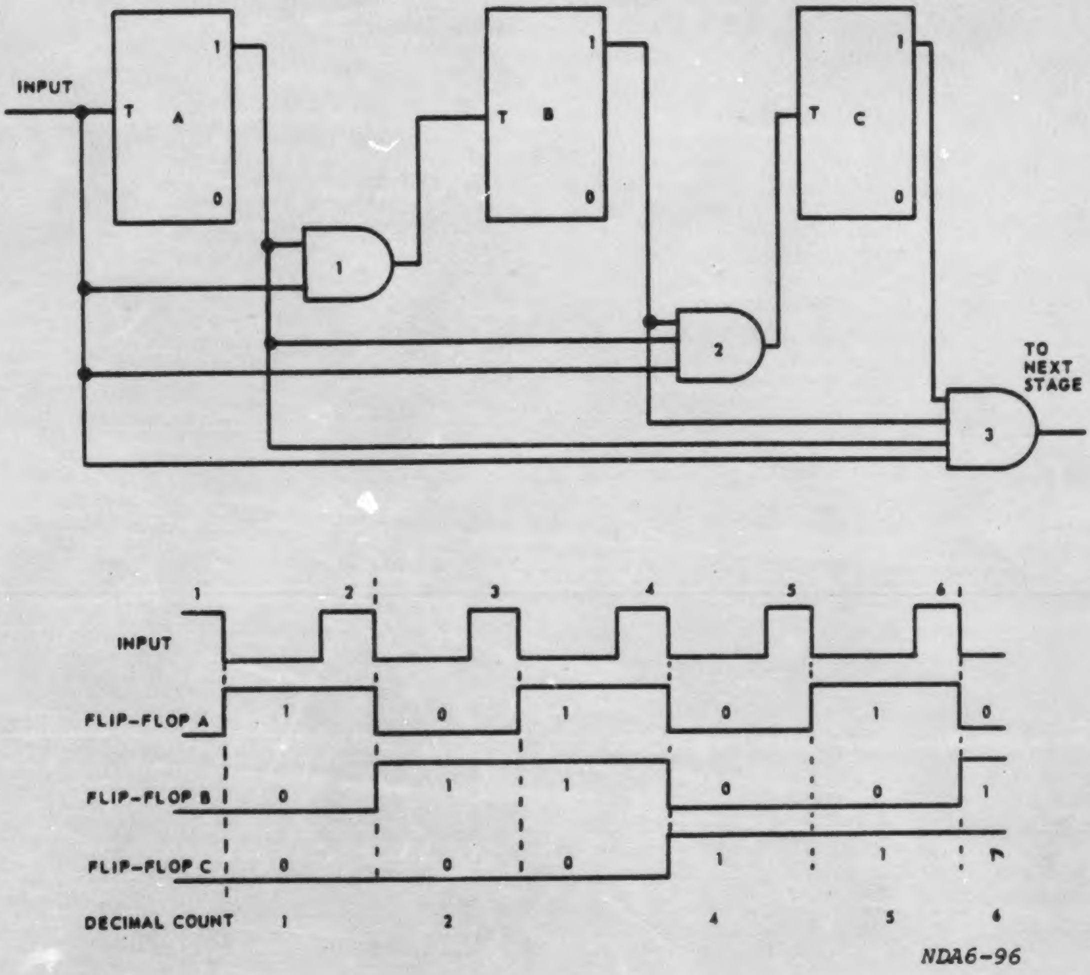


Figure 3-6. Parallel up-counter.

F/F is triggered on the down-clock. The first input pulse is applied to the input of F/F-A and to one leg (input) of positive AND-gates 1, 2, and 3. The other inputs to these gates are from the SET side of the counter's F/Fs. The end result of this first input pulse is that F/F-A gets set (ONE state), which, in turn, places a HIGH on one leg of the three AND-gates. The up-clock of the second input pulse conditions AND-gate 1 and causes its output to up-clock. The down-clock of this same pulse clears F/F-A (ZERO state) and deconditions AND-gate 1, causing its output to down-clock; and this down-clock causes F/F-B to get set. The binary count in the counter is now 010 or 2. The down-clock of the third input pulse sets F/F-A. The binary count in the counter is now 011 or 3. The up-clock of the fourth input pulse provides the final conditioning level for AND-gate 2, causing its output to up-clock. The down-clock of this fourth input pulse clears F/F-A, deconditions AND-gates 1 and 2, causing their output to down-clock which, in turn, clears F/F-B and sets F/F-C. The binary count in the counter is now 100 or 4.

1-16. As the number of input pulses increases, the count in the counter progresses until a maximum count of seven (111) is reached. The next pulse (the 8th) causes the counter to clear all ZEROS.

1-17. *Parallel down-counter.* The function of this counter is the same as the serial down-counter. That is, the count in the counter is decreased by one each time an input pulse is applied. However, the parallel down-counter operates at a faster speed than the serial down-counter, but it uses more circuitry to do so. Figure 3-7 illustrates a

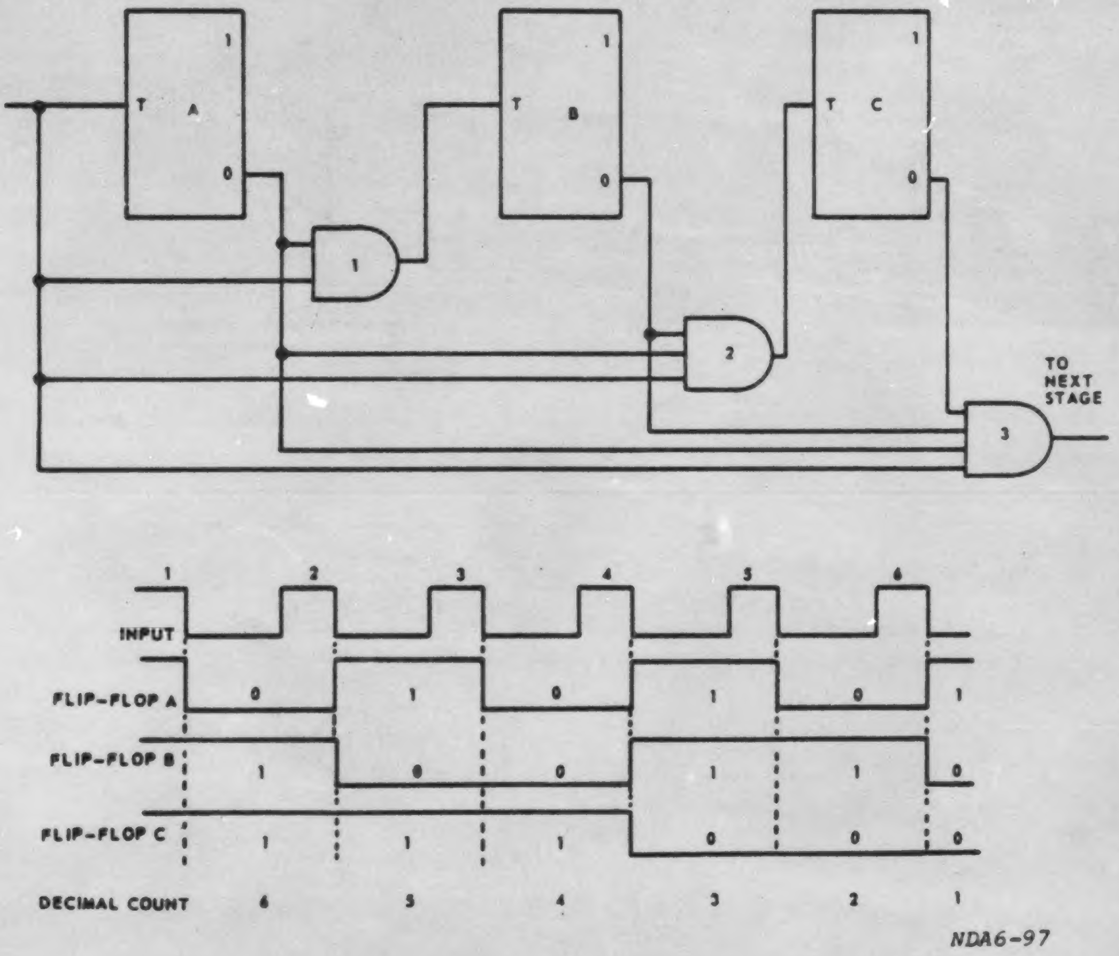


Figure 3-7. Parallel down-counter.

parallel down-counter with the associated waveforms for the input pulses and the SET-side outputs of the flip-flops. Notice that the difference between this counter and the up-counter in figure 3-5 is that the AND-gates are conditioned by the CLEAR-side output of the F/Fs.

1-18. **Advantages and Disadvantages of Serial and Parallel Counters.** Table 3-2 summarizes a comparison of serial and parallel counters from the standpoint of their advantages and disadvantages. Basically, this table brings out the fact that the reaction time from one count to another is much faster in a parallel counter than in a serial counter. However, this advantage is at the expense of more circuitry and high power requirements. Another advantage of the parallel counter is that propagation time is equal to the transient time of one F/F; whereas, in a serial counter, this time is equal to the sum of the transient time of all F/Fs that change state with a given input pulse.

1-19. **Determining Count in Counter.** There may be times on your job when it will become necessary for you to determine the count in an up-counter or a down-counter after a given number of input pulses are applied. Use of the formulas below should help you to perform this task.

1-20. *Up-counters:*

$\frac{P + C_c}{2^N}$ = number of counter cycles + R (remainder).

P = number of pulses to be applied.

C_c = the original count in the counter.

2^N = the modulus of the counter. Recall this is equal to the number of pulses required to recycle the counter (N = number of stages in the counter).

R = the new count in the counter.

- Example: A five-stage up-counter contains a *binary* count of 10100 or $20_{(10)}$. After 20 input pulses are applied, what is the new count in the counter, and how many times has it cycled completely through all counts?
- Solution: $\frac{P + C_c}{2^N} = \frac{20 + 20}{2^5} = \frac{40}{32}$ = 1 cycle and R of 8.
- Result: The new binary configuration in the counter is equal to 01000 which is $8_{(10)}$.

1-21. *Down-counters:*

$\frac{P - C_c}{2^N}$ = number of counter cycles + R.

$2^N - R$ = the new count in the counter.

TABLE 3-2
ADVANTAGES AND DISADVANTAGES OF SERIAL AND PARALLEL COUNTERS

	TYPES OF COUNTERS	
	SERIAL	PARALLEL
SPEED	SLOW	FAST
PROPAGATION TIME	LONG	SHORT
CIRCUITRY	SIMPLE	COMPLEX
COST	LOW	HIGH
ACCURACY	POOR	GOOD
POWER	LOW	HIGH

NDA6-89

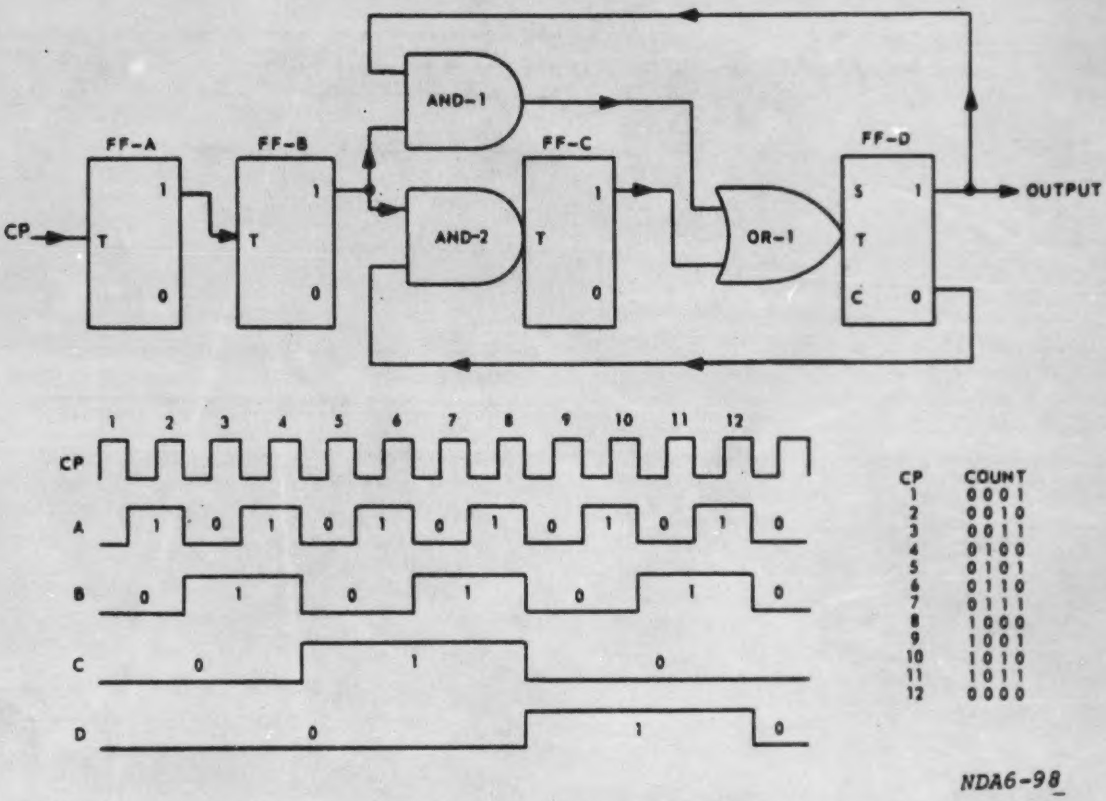
- Example: A six-stage down-counter contains a binary configuration of 0001000 or $4_{(10)}$. After 75 input pulses are applied, what is the new count in the counter, and how many times has it cycled completely through all counts?
- Solution: $\frac{P - C_c}{2^N} = \frac{75 - 4}{2^6} = \frac{71}{64}$ = 1 cycle and R of 7.

  $2^N - R = 2^6 - 7 = 64 - 7 = 57.$
- Result: The new binary configuration in the counter is equal to 111001 which is $57_{(10)}$.

1-22. **Modulus Counters.** Binary counters that are modified to have a modulus that is not a power of 2 are called modulus counters, or simply referred to as *mod counters*. In this section, we will discuss two mod counters: the mod 12 and the mod 10.

1-23. *Mod-12 counter.* Figure 3-8 illustrates a mod-12 counter. It is a four-stage series up-counter which has been modified to block F/F-C from receiving counts after the count of 8. Since this F/F represents $2^2 = 4$, disabling it removes four counts from the maximum count capability of the counter. We know a four-stage binary counter has a modulus of $2^4 = 16$. Therefore, this modified counter has a modulus of 16 - 4 = 12. Thus, it is named *mod-12 counter*.

1-24. AND-gate 2 is the blocking gate. AND-gate 1 permits F/F-C to be bypassed when it is no longer functioning as a counter stage, thereby removing four counts from the maximum capability of the counter. Until the count of 8 is reached, F/F-D is in the ZERO state and its ZERO output conditions one leg of AND-gate 2; thus, all down-clocks from



CP	COUNT
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	0000

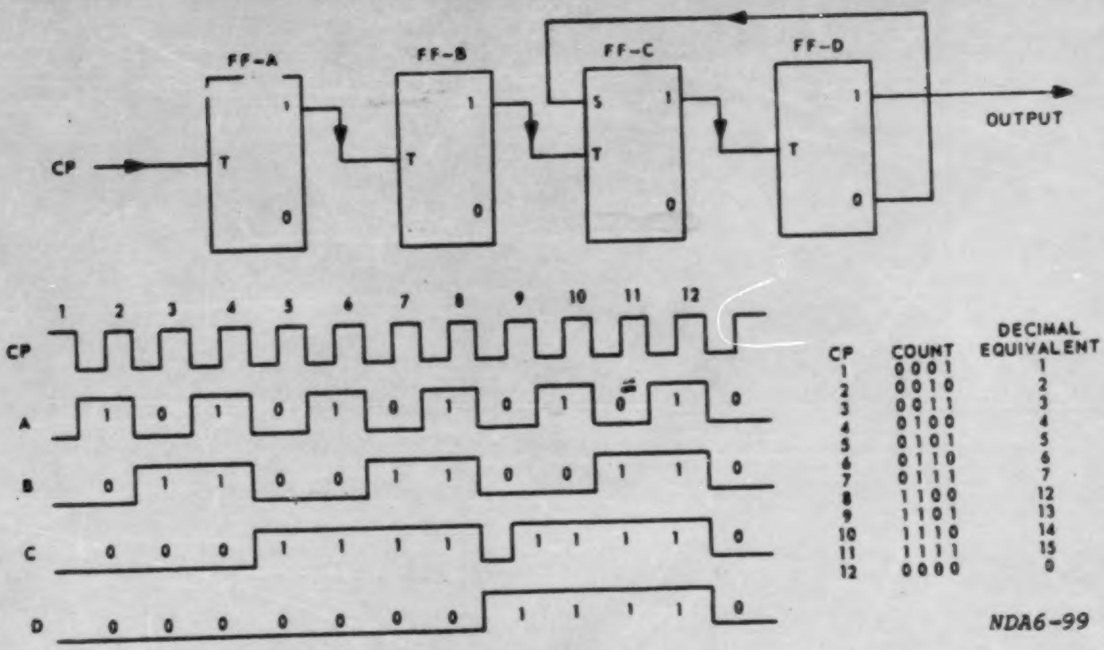
Figure 3-8. Mod-12 counter (count blocking).

F/F-B are permitted to pass through the gate and trigger F/F-C. Also, up to the count of 8, the ONE side of F/F-D is LOW, keeping AND-gate 1 deconditioned. From the waveforms and the table shown in figure 3-8, you can see that the counter functions as a normal serial up-counter, up to count 8. Clock pulse (CP) 8 sets F/F-D to the ONE state, deconditioning AND-gate 2 and conditioning AND-gate 1. F/F-C is now blocked and cannot count. F/F-A and F/F-B change state to provide the counts of 9, 10, and 11. Upon receipt of CP-12, F/F-A down-clocks, triggering F/F-B to the ZERO state. The down-clock from F/F-B passes through AND-gate 1 and triggers F/F-D to the ZERO state. Therefore, the counter is reset to 0000 upon receipt of the 12th clock pulse. The down-clock from the ONE side of F/F-D could be fed to other circuits in the equipment to indicate that 12 pulses were counted.

1-25. Another method of modifying a binary counter for a modulus of 12 is shown in figure 3-9. Instead of blocking four counts, this counter adds four counts. Notice that the counter counts seven pulses exactly like a serial up-counter. At the count of 7, it holds the binary configuration 0111. When the 8th clock pulse arrives, the counter jumps to the 1100 binary configuration, which is equal to decimal 12. Thus, only four more pulses are required to reset the counter to ZERO. With the reception of the 8th CP, the following actions take place:

- F/F-A flips to the ZERO state, sending a down-clock to F/F-B.
- F/F-B flips to the ZERO state, sending a down-clock to F/F-C.
- F/F-C flips to the ZERO state, sending a down-clock to F/F-D.
- F/F-D flips to the ONE state, sending a down-clock from its ZERO side to the SET input of F/F-C. This resets F/F-C to the ONE state.

1-26. From this discussion, you can see that the counter actually reaches the count of 8 momentarily, but before another CP arrives, the counter is set to a count of 12. Thus, count 8 becomes 12; count 9 becomes 13; count 10, 14; count 11, 15; and count 12



CP	COUNT	DECIMAL EQUIVALENT
1	0 0 0 1	1
2	0 0 1 0	2
3	0 0 1 1	3
4	0 1 0 0	4
5	0 1 0 1	5
6	0 1 1 0	6
7	0 1 1 1	7
8	1 1 0 0	12
9	1 1 0 1	13
10	1 1 1 0	14
11	1 1 1 1	15
12	0 0 0 0	0

NDA6-99

Figure 3-9. Mod-12 counter (count adding).

resets the counter to ZERO. When the counter resets to ZERO, the ONE-side output of F/F-D down-clocks. This down-clock could be fed to other circuits in the equipment to indicate that 12 pulses have been counted.

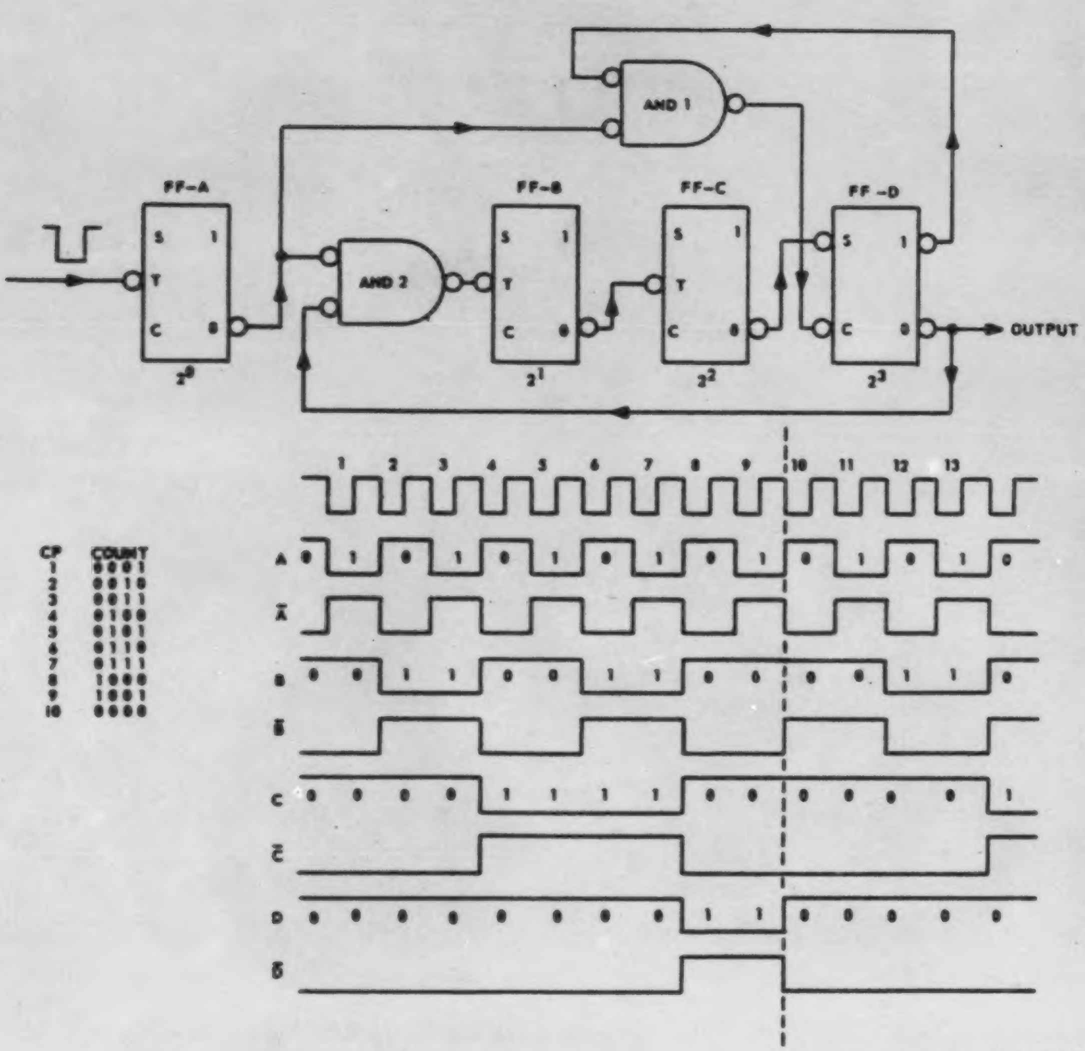
1-27. *Mod-10 (decimal) counter.* A mod-10 counter is normally called a decimal counter since it counts to 9 and resets on the 10th count. The method of developing a mod-10 counter is similar to that described for a mod-12 counter. In the mod-10 counter, either six counts must be blocked or six counts must be added. This is true because the basic counter itself is a four-stage binary counter which has a modulus of 16.

1-28. Figure 3-10 shows a simple mod-10 counter using the pulse blocking method. In this counter, F/F-B and F/F-C are blocked from receiving counts after the count of 8 is reached. This counter is drawn in negative logic. Before discussing how it counts, let us establish several pertinent facts about the circuit operation.

- The counter flip-flops trigger on the down-clock of the applied pulse.
- A LOW voltage represents a ONE; a HIGH voltage represents a ZERO. Therefore, when a flip-flop switches to the ONE state, the voltage from the ONE side down-clocks, and the voltage from the ZERO side up-clocks. Conversely, when a flip-flop switches to the ZERO state, the voltage from the ONE side up-clocks and the voltage from the ZERO side down-clocks.
- To make this circuit function as an up-counter, the trigger for each F/F is obtained from the ZERO side of the preceding F/F.

1-29. To clarify these facts, the waveforms for both outputs of each stage are shown. The waveforms A, B, C, and D represent the ONE-side output of the F/Fs. AND-gate 2 is the blocking gate. It passes the trigger pulses from F/F-A as long as F/F-D remains in the ZERO state. However, when F/F-D is triggered to the ONE state (with CP-8), its ZERO-side output goes HIGH, which deconditions AND-gate 2. With AND-gate 2 deconditioned, F/F-B and F/F-C are blocked from further counting. AND-gate 1 is a bypass gate that enables F/F-B and F/F-C to be bypassed when they are blocked by AND-gate 2.

1-30. The counter counts the first seven clock pulses as a simple serial up-counter. CP-8 triggers F/F-D to the ONE state, which deconditions one leg of AND-gate 2 and conditions one leg of AND-gate 1. F/F-B and F/F-C are now blocked and cannot count. CP-9 triggers F/F-A to the ONE state. The binary configuration in the counter is now 1001 or $9_{(10)}$. CP-10 triggers F/F-A to the ZERO state, and its output down-clocks.



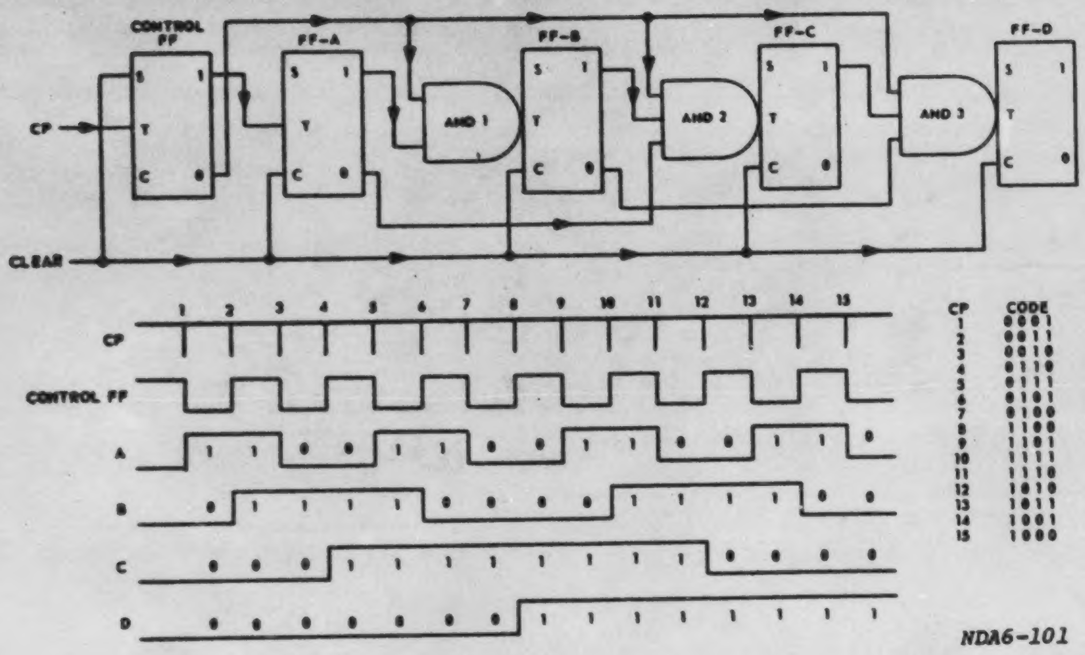
CP	COUNT
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	0000

Figure 3-10. Mod-10 counter (count blocking).

Now, this LOW from the ZERO side of F/F-A conditions the other leg of AND-gate 1, and its output down-clocks which, in turn, triggers F/F-D to the ZERO state. Since F/Fs-A, -B, and -C are also in the ZERO state, the count in the counter is now equal to zero. Therefore, the counter is a mod-10 counter.

1-31. Gray Counter. This type of counter counts pulses and provides outputs that are coded in gray code. Figure 3-11 illustrates a gray counter, its associated waveforms, and a code table. The right-hand column of this table represents the pattern followed by F/F-A. Note that F/F-A is in the ONE state for two counts, then the ZERO state for two counts, then returns to the ONE state for two counts. This pattern is continued for as many counts as the counter holds. Let's look at F/F-A and see how it is designed to follow this pattern.

1-32. In order to make F/F-A change state every two counts, the basic CP is fed to the control flip-flop, and that F/F develops the CP for F/F-A. Since a F/F divides by two, the control F/F triggers F/F-A every two pulses. This means that F/F-A is forced to follow the pattern indicated by the least significant column of the code table in figure 3-11. F/F-A changes state each time a down-clock is received from the control flip-flop. The control F/F is initially set to the ONE state by a clear pulse. The first CP triggers the control F/F to the ZERO state; it down-clocks, which, in turn, triggers F/F-A to the ONE state. This means F/F-A is set to the count of 1 with the first CP.



CP	CODE
1	0 0 0 1
2	0 0 1 1
3	0 0 1 0
4	0 1 1 0
5	0 1 1 1
6	0 1 0 1
7	0 1 0 0
8	1 1 0 0
9	1 1 0 1
10	1 1 1 1
11	1 1 1 0
12	1 0 1 0
13	1 0 1 1
14	1 0 0 1
15	1 0 0 0

Figure 3-11. Basic gray counter.

1-33. Now look at the next column to the left of the LSD column. It represents the pattern followed by F/F-B. Notice that F/F-B goes to the ONE state on the second count and remains in that state for four counts. Then it goes to the ZERO state for four counts, then to the ONE state for four counts, and continues to repeat this pattern. Let us see how this F/F is designed to follow this pattern.

1-34. F/F-B cannot change state until F/F-A is in the ONE state. Therefore, it cannot be set to the ONE state until the first pulse has been counted by F/F-A. Since F/F-B is clocked by the ZERO-side output of the control F/F, it cannot change state at the same time F/F-A changes state. Now look at the timing waveforms and notice that F/F-B changes state in the center of F/F-A's positive-going waveform.

1-35. Now look at the second column to the left of the LSD column. This represents the pattern followed by F/F-C. Notice that F/F-C goes to the ONE state at the count of four and remains in the ONE state for eight counts. Then it goes to the ZERO state for eight counts, and continues to repeat this pattern. Let us see how this flip-flop is designed to follow this pattern.

1-36. F/F-C cannot change state until F/F-A is in the ZERO state and F/F-B is in the ONE state; therefore, AND-gate 2 doesn't permit a clock pulse (from the control flip-flop) to pass through until the count of 3. At the count of 3, the pulse from the ZERO side of the control F/F is up-clocking. At the count of 4, the conditions to this AND-gate do not change, but the pulse from the control F/F is a down-clock and F/F-C is set to the ONE state. The condition that satisfies AND-gate 2 occurs every eight counts; therefore, F/F-C changes state every eight counts. Now look at the timing waveforms and note that F/F-C cannot change state at the same time F/F-A or F/F-B is changing state.

1-37. You should be able to figure out F/F-D's pattern and see how that pattern is accomplished by the counter. Look at the waveforms; notice that only one stage of the counter (disregarding the control F/F) changes state from one count to the next. This, of course, is the primary advantage of gray code over binary. That is, from one count to another only one digit changes.

1-38. **Ring Counters.** A type of counter in which only one stage of the counter is in the ONE state at any one time is called a *ring counter*. This type of counter does not provide an output that is identifiable as a particular code, such as is provided by a binary counter or a gray counter. Instead, a ring counter provides a "one-shot" indication. That is, only one output line from the counter is energized at any one time.

1-39. Figure 3-12 shows a simple ring counter. It is designed in the form of a closed loop; that is, F/F-D (the last stage) feeds back to the input stage to automatically start the count over. Not all ring counters function in this manner. Some ring counters count from a preset point and must be reset before starting over again.

1-40. Assume that F/F-D is in the ONE state; thus, its output is HIGH, indicating that four pulses have been counted. The next CP, CP-1, on the start of a new count, passes through AND-gate 4 and sets F/F-A to the ONE state and F/F-D to the ZERO state. Line A is now HIGH, indicating that the counter holds a count of one. The next clock pulse, CP-2, passes through AND-gate 1 to set F/F-A to the ZERO state and F/F-B to the ONE state. Line B is now HIGH, indicating that the counter holds a count of two. The next clock pulse, CP-3, passes through AND-gate 2 to set F/F-B to the ZERO state and F/F-C to the ONE state. Line C is now HIGH, indicating that the counter holds a count of three. The next clock pulse, CP-4, passes through AND-gate 3 to set F/F-C to the ZERO state and F/F-D to the ONE state. Line D is now HIGH, indicating that the counter holds a count of four.

1-41. The counter has now progressed through a complete cycle. Only one stage was in the ONE state at any one time. This four-stage counter has the capability of counting only four pulses. Consequently, the counter stages do not represent the place position of any number system; instead, each stage represents a number.

2. Storage Registers

2-1. In all computer systems, there is a need to temporarily store information derived from one functional block until it can be used by another functional block. This function is performed by storage registers. A storage register is capable of storing one assembled unit of information. This unit of information is known as a word, message, or character, depending upon the vocabulary used with a particular equipment. The ability of a storage register to store one unit of data is in contrast to bulk storage systems. These systems are normally referred to as memories and are covered in Chapter 4 of this volume.

2-2. **Functions of Storage Registers.** The functions performed by storage registers are as follows:

- Temporary storage of one unit of information.
- Conversion of serial binary data to parallel binary data.
- Conversion of parallel binary data to serial binary data.
- Time buffering between two devices operating at different speeds.

2-3. **Devices Used as Storage Registers.** Any two-stage device can be used to store one bit of information. Thus, any storage register can be constructed simply by assembling the number of two-state devices needed to store the number of bits in the unit of data. Two types of these two-state devices discussed here are the flip-flop (F/F) and the bimag core. Our discussion will be confined to flip-flop and bimag core registers.

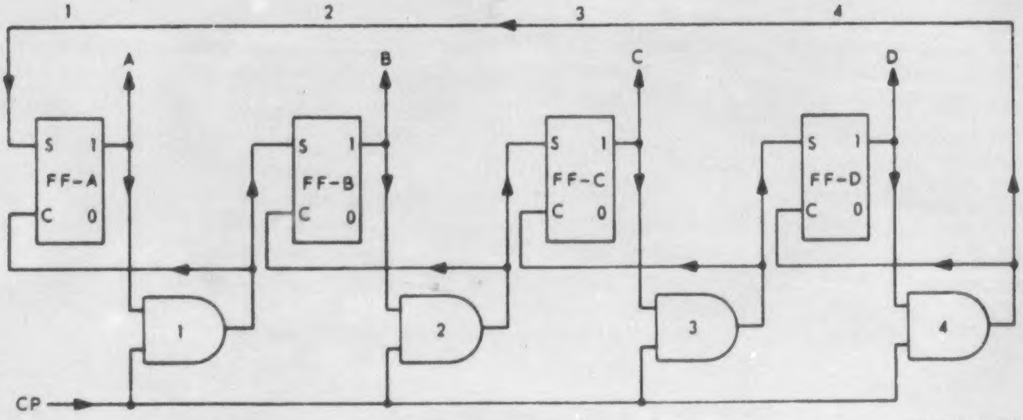


Figure 3-12. Closed ring counter.

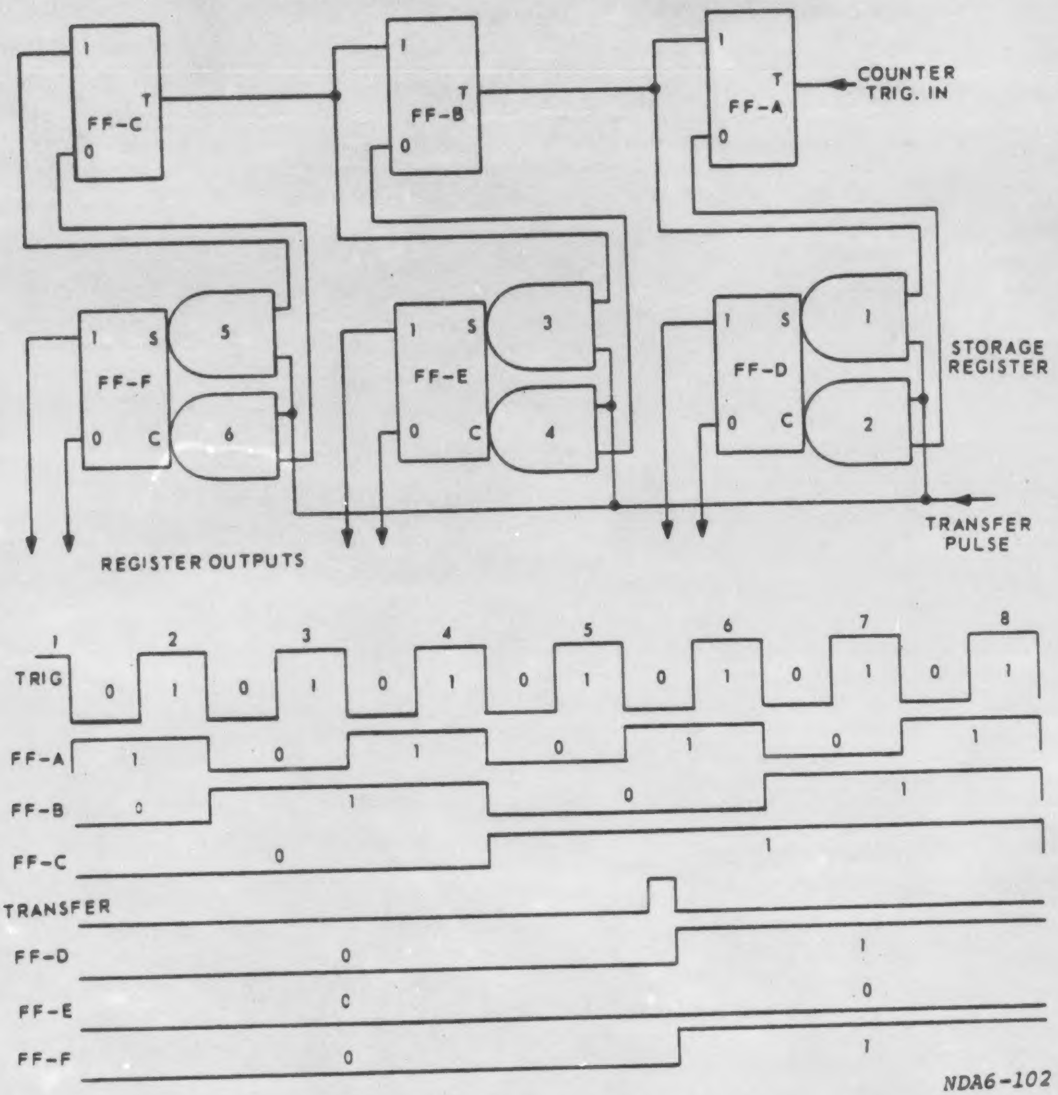
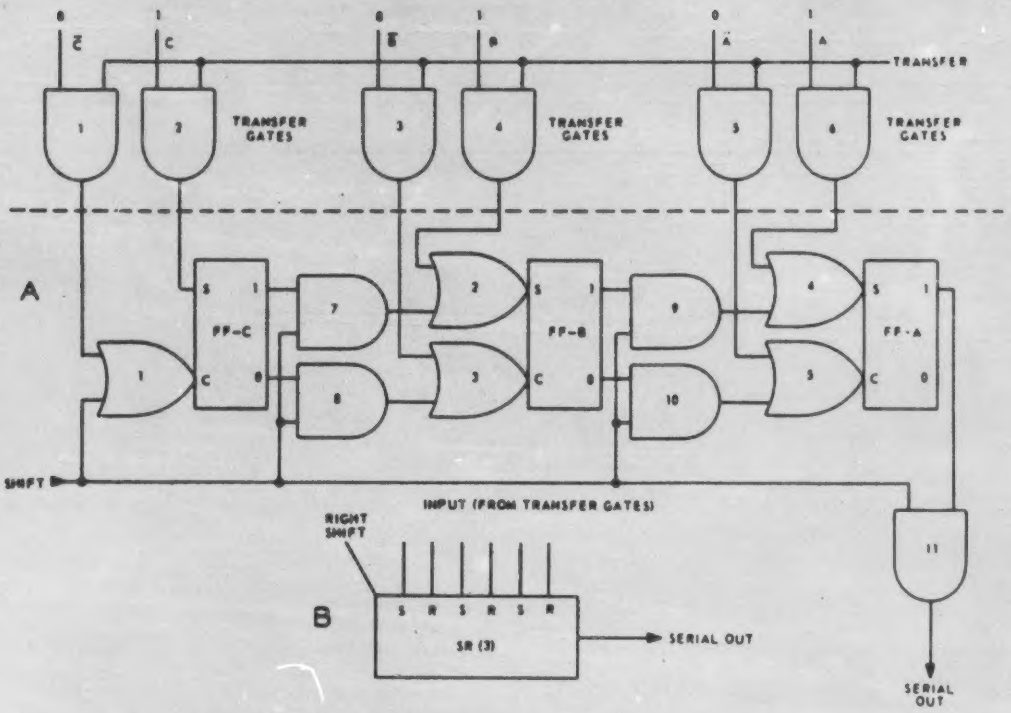

FF-C
FF-B
FF-A
T
1
0
COUNTER TRIG. IN
FF-F
FF-E
FF-D
S
C
1
2
3
4
5
6
STORAGE REGISTER
TRANSFER PULSE
REGISTER OUTPUTS
TRIG
FF-A
FF-B
FF-C
TRANSFER
FF-D
FF-E
FF-F
1
2
3
4
5
6
7
8
NDA6-102

Figure 3-13. Parallel-in/parallel-out register.

2-4. **Parallel-In/Parallel-Out Register.** This is a register that provides temporary storage between two functional blocks that use parallel data and accepts data in parallel and transfers data out in parallel. A typical use of this type of register is shown in figure 3-13. In this logic circuit, the content of the counter is sampled at the time the equipment generates a transfer pulse. The register stores the count and transfers it to using circuits when needed.

2-5. There are many configurations of F/Fs and gates that are used to make up this same type of register. The exact configuration used depends to a large extent upon the amount of interchangeability provided between the register and counter F/Fs within a particular equipment. The register F/Fs in figure 3-13 have an AND-gate at each input. This is typical of most multiuse F/Fs. In our illustration, the counter consists of F/F-A, F/F-B, and F/F-C; the storage register consists of F/F-D, F/F-E, and F/F-F. Notice that the ONE and ZERO side of each counter F/F is connected to the SET and CLEAR input of their respective register F/F through AND-gates 1 through 6. The second input to each of these gates is the transfer pulse.

2-6. If a transfer pulse occurs just after the



NDA6-103

Figure 3-14. Parallel-in/serial-out register.

counter reaches a binary count of 101, the outputs of the ONE side of F/F-A and F/F-C are HIGH, which conditions one leg of transfer AND-gates 1 and 5, respectively. When the transfer pulse occurs, it passes through these transfer gates and sets F/F-D and F/F-F to the ONE state. Transfer AND-gate 4 is conditioned by the HIGH output from the ZERO side of F/F-B; therefore, the transfer pulse passes through this gate to set F/F-E to the ZERO state. The binary count of 101 has now been transferred to the storage register without affecting the counting of the counter. The count stored in the storage register is now available for use by other circuits within a computer system. That is, the voltage levels available at the ONE and ZERO outputs of the storage register could be fed to count detection matrices, digital-to-analog converters, or any circuit that needs this particular count to perform a specific function. Note from the waveforms in the figure that this count remains in the storage register until another transfer pulse is generated to read in a new count.

2-7. When another transfer pulse reads in a new count from the counter, it changes the state of the register F/Fs to represent the new count. Since the transfer gates sample both sides of the counter F/Fs, no clear pulse is needed to clear the register of old data prior to the transfer in of new data. Note one other feature of this circuit: The transfer pulse is delayed slightly with respect to the pulses counted by the counter. This allows the counter F/Fs to assume a stable state between count states prior to transfer.

2-8. Parallel-In/Serial-Out Register. Most digital operations are carried out in parallel circuits. Therefore, when all necessary operations result in an answer that is in binary form, that binary number of configuration is normally in a parallel register awaiting use. If this number is to be used to actuate print hammers to print out the information it represents, or if it is used to position the beam of a CRT to display the data as a radar picture, it is usually transferred in parallel to decoders or digital-to-analog converters. When the data must be transmitted over telephone lines or microwave links to another computer system, it must be converted from parallel to serial form. This conversion is made by parallel-in/serial-out registers.

2-9. Figure 3-14,A, illustrates a register that accepts data in parallel through AND-gates 1 through 6, and shifts it out serially, bit by bit, through AND-gate 11. The actual storage register is composed of three F/Fs—A, B, and C—AND-gates 7 through 10, and OR-gates 1 through 5. Normally, in practical circuits, these OR-gates are part of the flip-flop and are not shown on functional diagrams. By showing them as separate functional circuits, we hope to give you a clear picture of the operation of the register. Figure 3-14,B, depicts the register as it is shown in simplified MIL-STD 806B logic.

2-10. *Transfer operation.* For an explanation of the transfer action, let's assume that the binary configuration 011 is transferred to the storage register. This means the transfer gate input lines A, B, and C are HIGH. When the transfer pulse is applied to AND-gates 1 through 6, the output of AND-gates 1, 4, and 6 goes HIGH. These HIGH levels are, in turn, applied to OR-gates 1, 2, and 4. When the transfer pulse is removed, a down-clock is felt at the CLEAR (C) input of F/F-C and the SET (S) input of F/Fs-A and -B. Therefore, the storage register now contains the binary configuration 011. Now let's shift this data out of the storage register.

2-11. *Shifting operation.* Three shift pulses are required to shift the binary configuration 011 out of our example register. The action that occurs as a result of each shift pulse will be discussed separately.

a. First shift pulse:
- Passes through AND-gate 11 as the first ONE bit in the serial data.
- Passes through AND-gate 9 and OR-gate 4 to keep F/F-A in the ONE state.
- Passes through AND-gate 8 and OR-gate 3, which flips F/F-B to the ZERO state.
- Passes through OR-gate 1 to insure F/F-C is in the ZERO state. The shift register now contains the binary number 001, and a ONE has been shifted out of AND-gate 11 onto the serial output line.

b. Second shift pulse:
- Passes through AND-gate 11, as F/F-A is still in the ONE state, and becomes the second ONE bit on the serial output line.
- Passes through AND-gate 10 and OR-gate 5 which flips F/F-B to the ZERO state.
- The shift register now contains the binary number 000.

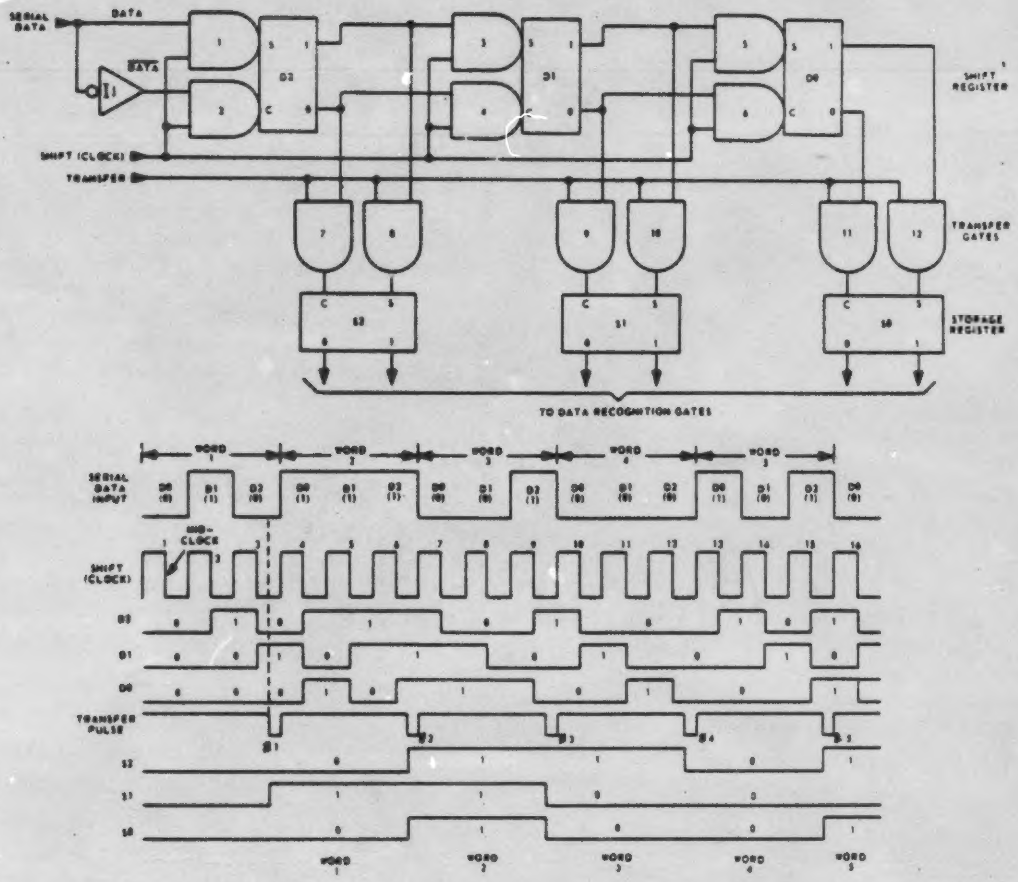
c. The third shift pulse finds AND-gate 11 disabled (F/F-A is now cleared) and the output becomes ZERO for this third time period.

2-12. The application of the three shift pulses has placed the binary configuration 011 onto the serial line. Note that the shifting process cleared the register to all ZEROS.

2-13. **Serial In/Parallel-Out Register.** When data is to be transmitted over relatively long distances, it is uneconomical to use a line for each bit in a binary configuration as is required for parallel transfer of data. Therefore, data being sent away from a facility is normally transferred serially in a manner similar to that described in paragraph 2-11. The equipment that receives this serially transmitted data must accept it bit by bit as it comes in on the serial line, and, once received, this serial data must be converted to parallel data for use in parallel operations. To perform this serial-to-parallel conversion, a serial-in/parallel-out register is normally used. A typical register of this type is illustrated in figure 3-15. it is designed to accept a three-bit word in serial form and, when the total word is in the register, transfer it to the parallel storage register. Circuits of this type normally have more than three stages; however, if you understand how three stages work, you'll understand the operation of registers with many stages.

2-14. Look at the waveforms in our figure, and notice that the serial data input consists of five three-bit words, with each word containing bits D0, D1, and D2. Serial data is applied to F/F-D2 via AND-gates 1 and 2. The input to AND-gate 2 is inverted by inverter I1; thus, the output of the inverter is referred to as $\overline{\text{DATA}}$. DATA provides a conditioning level to AND-gate 1 when the data bit is a ONE, and $\overline{\text{DATA}}$ provides a condition-level to AND-gate 2 when the data bit is a ZERO. A shift pulse is applied simultaneously to all register input gates. The down-clock of the shift pulse occurs in the middle of the data pulse which causes shift-in to occur. A transfer pulse occurs following the down-clock of *every third shift pulse.* Now let's shift each bit of word 1 in serially and then transfer the word to the storage register in parallel.

2-15. *Shift-in operation.* The first bit applied is D0 which is a logic ZERO. AND-gate 2 is conditioned by D0 and the SHIFT PULSE. At mid-clock time, the shift pulse down-clocks, the output of AND-gate 2 goes negative, and F/F-D2 is cleared (set to


SERIAL DATA
DATA
DATA
SHIFT (CLOCK)
TRANSFER
SHIFT REGISTER
TRANSFER GATES
STORAGE REGISTER
TO DATA RECOGNITION GATES
WORD 1
WORD 2
WORD 3
WORD 4
WORD 5
SERIAL DATA INPUT
MID-CLOCK
SHIFT (CLOCK)
D2
D1
D0
TRANSFER PULSE
S2
S1
S0

NDA6-104

Figure 3-15. Serial-in/parallel-out register.

the ZERO state). Bit D0, a logic ZERO, is now stored in F/F-D2. AND-gate 4 is conditioned by the ZERO-side output of F/F-D2 and the second shift pulse. At the down-clock of this second shift pulse, the output of AND-gate 4 goes negative which clears F/F-D1 to the ZERO state. AND-gate 1 is conditioned by D1 which is a logical ONE and the SHIFT PULSE. At the down-clock of the second shift pulse, the output of AND-gate 1 also goes negative, setting F/F-D2 to the ONE state. The first two data bits (D0 = 0, D1 = 1) are now stored in shift register F/Fs-D2 and D1, respectively.

2-16. AND-gate 6 is conditioned by the ZERO side output of F/F-D1 and SHIFT PULSE. At the down-clock of the third shift pulse, the output of AND-gate 6 goes negative which clears F/F-D0 to the ZERO state. AND-gate 3 is conditioned by the ONE-side output of F/F-D2 and the third shift pulse. AND-gate 3's output also goes negative with the down-clock of the third shift pulse which sets F/F-D1 to the ONE state. The third data bit, D2, is a logic ZERO; therefore, F/F-D2 is cleared to the ZERO state by the output of AND-gate 2. The first word, 010, is now stored in the shift register.

2-17. *Transfer operation.* Transfer pulse number 1 is now applied to transfer AND-gates 7 through 12. Since the shift register contains the binary configuration 010, AND-gates 7, 10, and 11 are conditioned. At the down-clock of the shift pulse, these gates are deconditioned, their output goes negative, and the word is transferred to the storage register. F/F-S2 is cleared, F/F-S1 is set, and F/F-S0 is cleared. Word number 1 is now in the storage register where it is available for use until the next transfer pulse transfers in a new word. Circuit

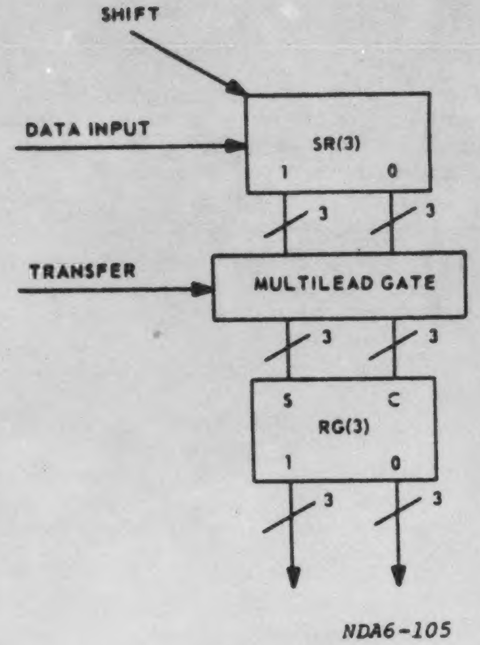

SHIFT
DATA INPUT
SR(3)
1
0
3
3
TRANSFER
MULTILEAD GATE
3
3
S
C
RG(3)
1
0
3
3
NDA6-105

Figure 3-16. Simplified representations, shift/storage register (serial-in/parallel-out).

operation for serial input words 2, 3, 4, and 5 is similar to that just explained for word 1. The waveforms for these remaining four words are shown in the figure.

2-18. *Simplified representation of serial-in/parallel-out register.* The shift register, transfer gates, and the storage register of a serial-in/parallel-out register are represented in simplified form as shown in figure 3-16. This form of logic representation is normally used where detail is not needed and only basic logic functions need to be shown. Data input is shown coming into the left side of the block labeled SR. The SR (3) inside this block identifies it as a three-stage shift register. The shift arrow shows that shifting is to the right. The slash marks with the number 3 at each output of the SR indicate three ONE-side outputs, and three ZERO-side outputs from the shift register are applied to the multilead gates. Presence of the transfer line indicates that all gates transfer when this pulse is applied. The remainder of the drawing is self-explanatory. Compare it with the drawing in figure 3-15, and note how simple functions can be expressed when there is no interest in the detail of how these functions are accomplished.

2-19. Serial-In/Serial-Out Magnetic Storage Register Considerations. In the output section of many computer systems, it is often necessary to change from the fast data rate of the equipment to a slower rate acceptable by various devices such as landlines (telephone

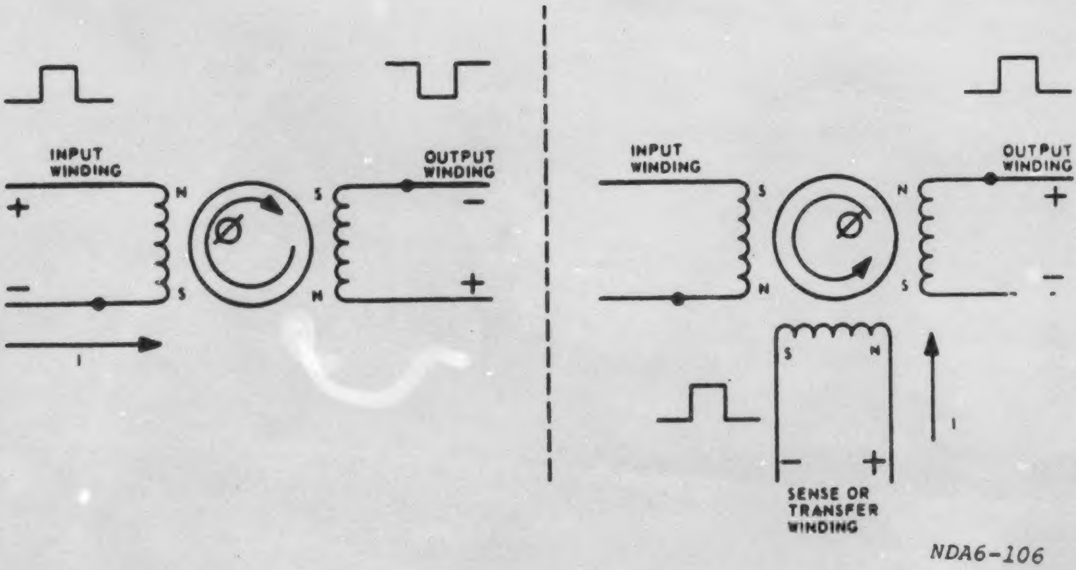

INPUT WINDING
OUTPUT WINDING
+
−
N
S
S
N
Ø
−
+
I
INPUT WINDING
OUTPUT WINDING
S
N
N
S
Ø
+
−
S
N
−
+
I
SENSE OR TRANSFER WINDING
NDA6-106

Figure 3-17. Bimag core.

lines). In these instances, a magnetic shift register (MSR) consisting of bimagnetic cores (referred to as *bimag cores*) is often used. The purpose of a magnetic shift register is to accept and store binary information. This information is shifted in serially, stored, and shifted out serially. A magnetic shift register consists of a series of bimag cores that are connected to transfer information in sequence from one core to another. The bimag cores used in circuits of this type consist of a ferromagnetic core and three or more windings. These windings are the input winding, the transfer or sense winding, and the output winding. Figure 3-17 shows a typical bimag core. The core is represented by the circle, and the windings are represented by the coil symbols. The dot denotes the polarity of the windings. When current flows into the dot side of the winding, the core is set to the ONE state; when current flows into the nondot side of the winding, the core is set to the ZERO state.

2-20. *Bimag core read-in process.* With a pulse causing current to flow into the dot side of the input winding (refer to fig. 3-17), the core flux increases rapidly to saturation, thus causing a voltage of opposite polarity to be induced into the output winding. When the input pulse drops to ZERO, the core remains magnetized: No current is flowing and no voltage is induced in the output winding; however, the core remains magnetized to the ONE state.

2-21. *Bimag core read-out process.* In order to read a ONE out of a core, it must be changed to its other stable state (opposite polarity): ZERO. To do this, a pulse is applied that causes current to flow into the nondot side of the transfer winding. This current causes the core to become polarized in the opposite direction. As the core switches rapidly from the ONE to the ZERO state, a large flux change takes place. This change induces a positive polarity pulse into the output winding. This positive pulse represents a binary ONE. The read-out process described here is also referred to as the transfer process.

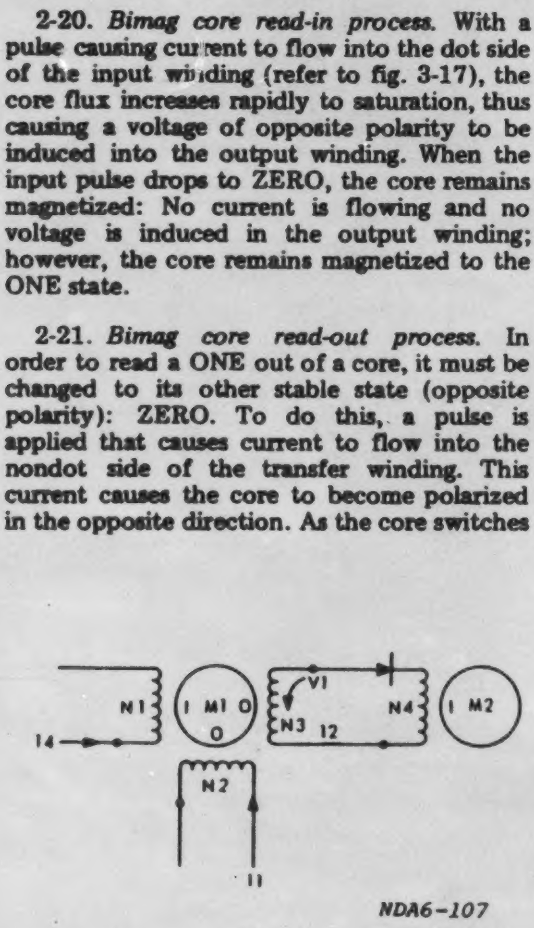


Figure 3-18. Single-diode transfer loop.

2-22. *Bimag core shifting process.* The basic circuit for connecting two cores within a magnetic shift register is called a *single-diode transfer loop.* Figure 3-18 shows a typical transfer loop consisting of two bimags and a crystal diode. The cores, M1 and M2, are represented by a circle. The three windings on the core are represented by the coil symbols placed around the circle. Assume that M1 and M2 are in the ZERO state. A pulse representing a binary ONE is applied to the input winding of M1. The current flowing into the dot side of winding N1 causes the bimag core to change to the ONE state. The rapid change of flux caused by the core switching from the ZERO state to the ONE state induces a voltage of opposite polarity into the output and transfer windings. The current flow through winding N2 can be ignored; however, the current flow in winding N3 would flow through the input winding of the second core M2 and set it to the ZERO state, if it were not for the crystal diode. The voltage induced in the output winding of M1 is negative on the dot side and positive on the nondot side. This applies a negative potential to the cathode of the diode. Due to the large back resistance of the crystal diode, insufficient current flows through the diode transfer loop to have any effect on the input winding of bimag M2. Therefore, after the pulse to the input of M1 passes, M1 is in the ONE state and M2 is in the ZERO state. Before another bit of information can be read into M1, the ONE it holds must be transferred to M2; the next step is the transfer step.

2-23. To transfer information from one core to the next core, a transfer pulse is applied to the transfer winding. The polarity of this pulse is such that current flows into the nondot side of N2, causing the core to switch to the ZERO state. As core M1 is switched rapidly from the ONE state to the ZERO state, a large change of flux takes place. This change in flux induces a voltage into the output winding N3. The polarity of the voltage induced in N3 causes a current to flow into the dot side of N4 back through the diode to the dot side of N3. This current sets the core M2 to the ONE state. Thus, a binary ONE has been transferred from M1 to M2. M1 is in the ZERO state and can now accept another bit of information.

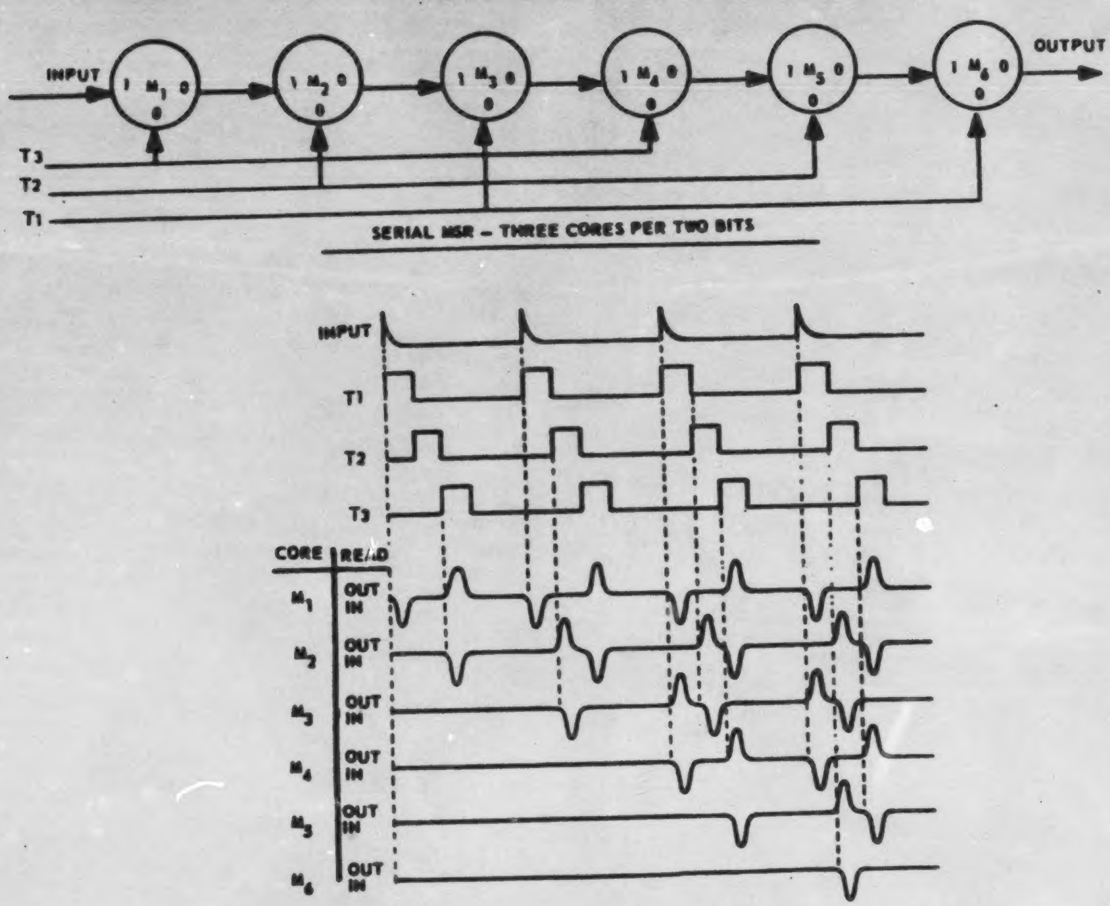


Figure 3-19. Magnetic shift register.

2-24. **Basic Magnetic Shift Register (MSR).** A magnetic shift register can be formed by connecting a series of bimag cores and their associated transfer loops together. Figure 3-19 shows a magnetic shift register which has a total of six cores. The circle represents the core. The arrows indicate the winding inputs and outputs. Each input winding is identified by the number 1 inside the circle. The sensing (transfer) and output windings are identified by a ZERO, since they are opposite in polarity to the input winding. This is a three-core-per-two-bit register; that is, it requires three cores to hold two bits of information. The operation of the MSR is divided into three steps: shift-in, storage, and shift-out. In our explanation of the MSR, we'll shift in four binary ONES and then shift them out serially.

2-25. *Shift-in.* Before shifting in new data, assume that all cores are in the ZERO state. Now refer to figure 3-19 and table 3-3. When the first data pulse which represents a binary ONE arrives at the input, the following circuit actions take place:

a. The first data pulse sets M1 to the ONE state. At the same time, a shift pulse, T1, is applied to the transfer windings of M3 and M6. Since cores M3 and M6 are in the ZERO state, the shift pulse has no effect.

b. At the trailing edge of shift pulse T1, the second shift pulse, T2, is applied to the transfer windings of cores M2 and M3. Since these cores are in the ZERO state, the shift pulse has no effect.

c. At the trailing edge of shift pulse T2, the third shift pulse, T3, arrives and is applied to the transfer windings of cores M1 and M4. The ONE in core M1 is transferred to core M2. Since M4 is in the ZERO state, the shift pulse has no effect on it.

d. The register now holds the binary configuration 010000, as shown in table 3-3.

TABLE 3-3
MAGNETIC SHIFT REGISTER ANALYSIS

	SHIFT PULSES	SHIFT-IN						SHIFT-OUT						OUT
		M1	M2	M3	M4	M5	M6	M1	M2	M3	M4	M5	M6	
First data pulse	T1	1	0	0	0	0	0	0	1	0	1	1	0	1
	T2	1	0	0	0	0	0	0	0	1	1	0	1	
	T3	0	1	0	0	0	0	0	0	1	0	1	1	
Second data pulse	T1	1	1	0	0	0	0	0	0	0	1	1	0	1
	T2	1	0	1	0	0	0	0	0	0	1	0	1	
	T3	0	1	1	0	0	0	0	0	0	0	1	1	
Third data pulse	T1	1	1	0	1	0	0	0	0	0	0	1	0	1
	T2	1	0	1	1	0	0	0	0	0	0	0	1	
	T3	0	1	1	0	1	0	0	0	0	0	0	1	
Fourth data pulse	T1	1	1	0	1	1	0	0	0	0	0	0	0	1
	T2	1	0	1	1	0	1	0	0	0	0	0	0	
	T3	0	1	1	0	1	1	0	0	0	0	0	0	

NDA6-90

2-26. When the second data pulse is applied to the input, the following circuit actions take place:

a. The data pulse sets M1 to the ONE state and the shift pulse, T1, senses M3 and M6. (The term "senses" is just another way of saying that a shift pulse is applied to the core to cause a transfer of information.) Cores M3 and M6 contain a ZERO; the shift pulse has no effect on them.

b. At the trailing edge of T1, the second shift pulse senses cores M2 and M5, thus transferring the ONE from M2 to M3. M5 remains in the ZERO state.

c. At the trailing edge of shift pulse T2, the third shift pulse, T3, senses cores M1 and M4, thus transferring the ONE from M1 to M2. M4 remains in the ZERO state.

d. The register now holds the binary configuration 011000, as shown in table 3-3.

2-27. When the third data pulse is applied to the input, the following circuit actions take place:

a. The data pulse sets M1 to the ONE state.

b. Shift pulse T1 transfers the ONE from M3 to M4.

c. Shift pulse T2 transfers the ONE from M2 to M3.

d. Shift pulse T3 transfers the ONE from M1 to M2 and also transfers the ONE from M4 to M5.

e. The register now holds the binary configuration 011010.

2-28. When the fourth data pulse is applied to the input, the following circuit actions take place:

a. The data pulse sets M1 to the ONE state.

b. Shift pulse T1 transfers the ONE from M3 to M4.

c. Shift pulse T2 transfers the ONE from M2 to M3 and also transfers the ONE from M5 to M6.

d. Shift pulse T3 transfers the ONE from M1 to M2 and also transfers the ONE from M4 to M5.

e. The register now holds the binary configuration 011011.

2-29. *Storage.* With the shift-in process complete, the binary configuration is considered to be *in storage*. That is, if the data is not shifted out, it will remain in the bimags indefinitely because of their *nonvolatile* characteristics. However, to complete our discussion of the bimag, we need to shift the binary configuration 011011 out.

2-30. *Shift-out.* When the information stored in the MSR is needed, a series of shift pulses are applied to the transfer windings of the bimag cores. Referring to figure 3-19 and table 3-3, note that the first T1 pulse causes a ONE to be shifted out of the MSR, while T2 and T3 shift the data bits toward the output. The next T1 pulse causes the second ONE to be shifted out, and T2 and T3 will shift the remaining data bits toward the output. This process continues until all data bits are shifted out. Upon completion of the shift-out process, each bimag of the MSR is in the ZERO state.

2-31. In our example of a basic MSR, three cores were necessary to store two bits of data. If one timing pulse were used per core, a three-core register could store three bits of data. However, as registers increased in size, the number of individual timing pulses would also increase, which would cause an increase in both the shift-in and shift-out time.

3. Decoders

3-1. A decoder is a combination of switching circuits used to translate two or more input signals in code form to a selected (discrete) output signal. Some of the devices used in decoder circuits include vacuum tubes, diodes, transistors, magnetic cores, and relays. Decoders are used for such functions as address, instruction, count, and character decoding. Our discussion of decoder circuits is concerned with those decoders that employ the use of diodes and relays. Decoders are known by many other names that express the type of data they decode. Some of the names associated with decoders include:

- Count decoder or detector—detects the presence or absence of a count or counts in a counter.
- Address decoder—decodes addresses of memory locations.
- Instruction decoder—decodes instructions that control circuit operations.
- Character decoders—decodes alphanumeric characters.

3-2. AND/OR-Gate Decoders. Figure 3-20 illustrates a serial up-counter with a simple AND-gate decoder which detects a specific count. Notice that this AND-gate produces a positive pulse output only when a count of 14 is present in the counter. This pulse output could be used for any control function that must occur at a specific time, such as when 14

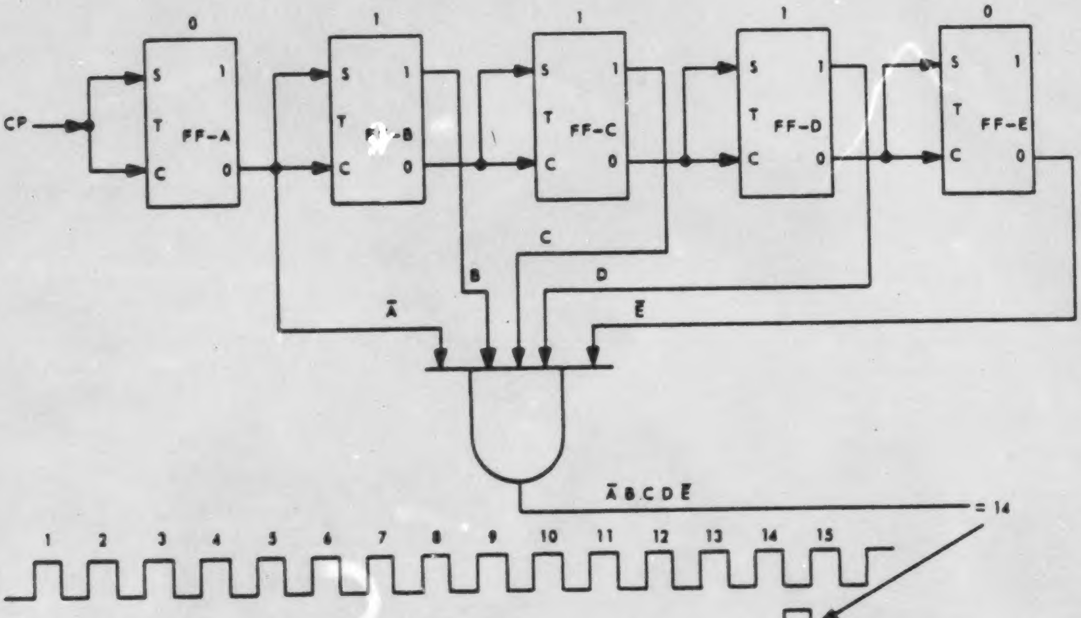


Figure 3-20. Count detection of 14.

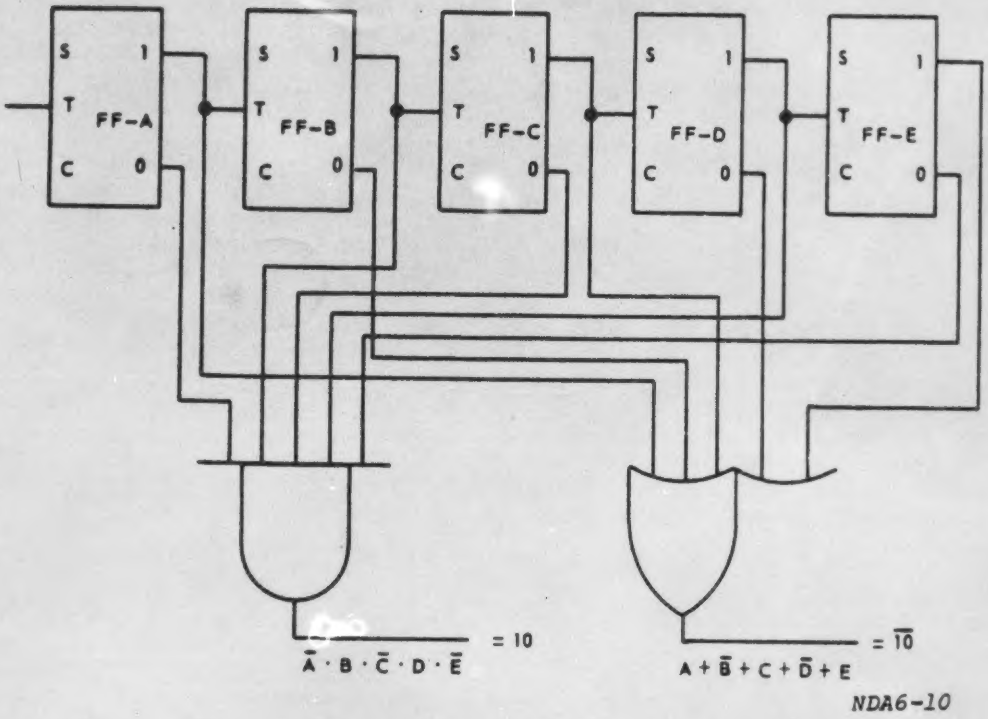

S
1
T
FF-A
C
0
FF-B
FF-C
FF-D
FF-E
= 10
$\bar{A} \cdot B \cdot \bar{C} \cdot D \cdot \bar{E}$
= $\overline{10}$
$A + \bar{B} + C + \bar{D} + E$
NDA6-10

Figure 3-21. Count detection of 10 or $\overline{10}$.

input pulses have been counted. Figure 3-21 shows a serial up-counter with an AND-gate and OR-gate being used to decode (or detect) specific counts. The AND-gate produces a positive output when the count of 10 is present in the counter; the OR-gate produces a positive output at all counts *except* the count of 10. Again, these outputs could be used for any control function that must occur at a specific time.

3-3. **Diode Matrix Decoders.** When a large number of AND- and OR-gates are used to detect a series of counts or a series of binary configurations, it is common practice to show them schematically as a diode matrix. This form of circuit is shown in figure 3-22. A three-stage serial up-counter is shown connected to eight AND-gates. Each AND-gate produces a pulse of one count width when a particular count is present in the counter.

3-4. Look at the first set of diodes. The anodes (plates) of the diodes are connected to the ZERO side of each F/F. This causes a positive output to appear on the first line when the binary count of 000 appears in the counter. Now look at the second set of diodes. They produce an output when the binary count of 001 is present in the counter. Recall that this count is expressed in Boolean notation as $A\bar{B}\bar{C}$. Notice that to decode the binary count 001, the plate of the diode connected to F/F-A is connected to its ONE side, and the plates of the other two diodes are connected to the ZERO side of their respective flip-flops. From this illustration, you should be able to recognize that the matrix represents eight separate 3-input AND-gates.

3-5. **Relay Decoders.** Circuits that require more current at the output than can be developed by diodes often use relays as decoders. Some of the circuits that make use of relay decoders are power controls, test function selectors, and print selectors.

3-6. Figure 3-23 shows a series of relays interconnected to form a decoder. A similar circuit is used in printers to select printer solenoids and, in turn, to determine what character is to be printed. Assume that the binary configuration 101 is present in the F/F register. The following circuit actions take place:

- The ONE in F/F-A causes relay A to energize, which switches its contacts and applies B+ to line A.
- The ZERO in F/F-B allows the B relay to remain in its deenergized state, leaving the B+ connected to the $\bar{B}$ line. The output is now $A\bar{B}$.

- The ONE in F/F-C energizes relay C. This switches relay contacts and connects B+ to the output line $A\bar{B}C$ which represents 101.

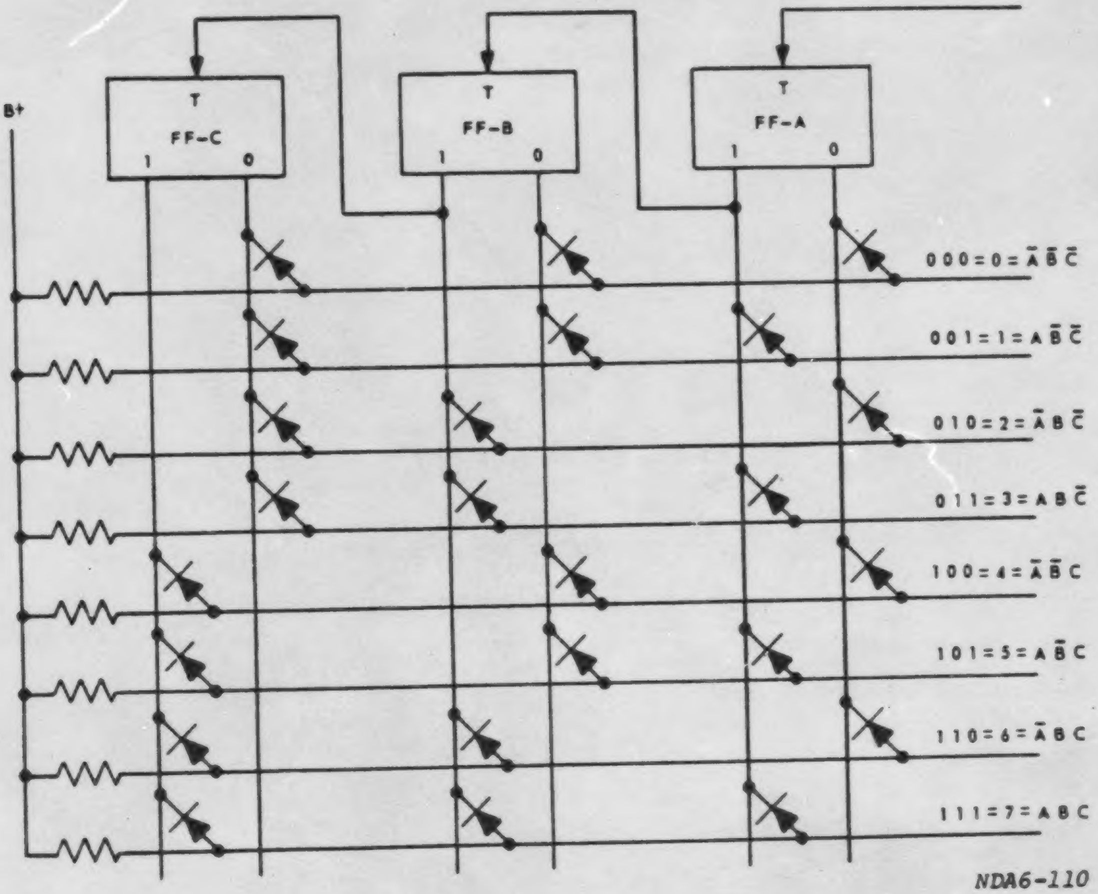
3-7. The end result is that the line selected by the relay contacts has a high voltage on it, representing a ONE. If a printer solenoid is connected to each line, the binary configuration 101 selects line 5 which would cause a specific character to be printed.

4. Digital and Analog Converters

4-1. There are many computer systems that must handle both digital and analog voltages. This requirement results in a need for circuits that are capable of converting these voltages from one to another. Digital-to-analog and analog-to-digital converters perform these functions.

4-2. **Digital-to-Analog Converter.** A computer output consisting of digital data may be sent to a digital-to-analog converter (called D to A) to change it from a digital form to an analog voltage. This analog voltage may be used to control some mechanism; for instance, it can drive an antenna or position the electron beam in a CRT.

4-3. There are several ways of converting digital data to analog. One of the most common ways is by the use of a resistor network. A typical digital-to-analog circuit is shown in figure 3-24. The converter is connected to a five-stage counter that holds a maximum decimal count of 31. The resistor ladder is made up of two sections which contain identical pairs of resistors in each leg. Notice that the value of each resistor is halved as the number increases from the LSD to the MSD. The output from the ONE side of each flip-flop is applied to a relay driver. When any one of the flip-flops is in the ONE state, the



NDA6-110

Figure 3-22. Diode matrix, decoder.

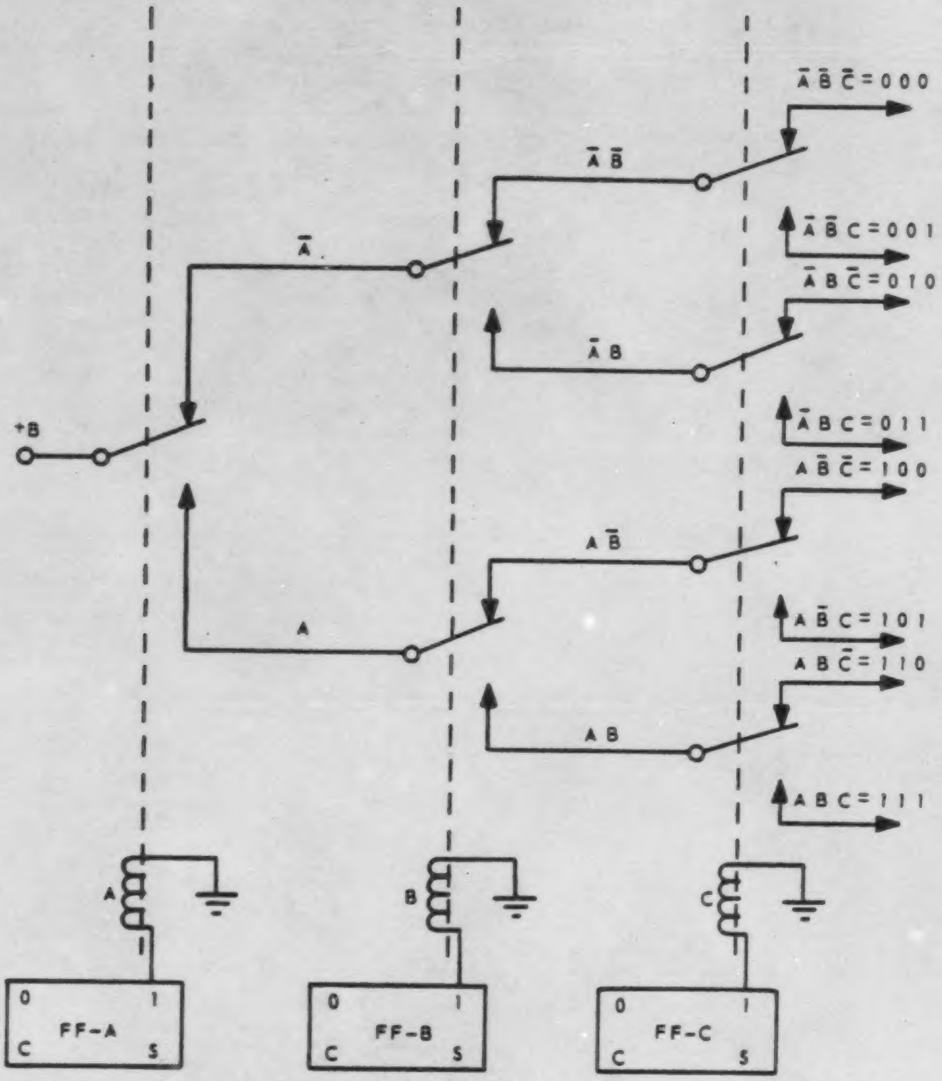

$\bar{A}\bar{B}\bar{C} = 000$
$\bar{A}\bar{B}$
$\bar{A}\bar{B}C = 001$
$\bar{A}$
$\bar{A}B\bar{C} = 010$
$\bar{A}B$
+B
$\bar{A}BC = 011$
$A\bar{B}\bar{C} = 100$
$A\bar{B}$
$A\bar{B}C = 101$
A
$AB\bar{C} = 110$
AB
$ABC = 111$
A
B
C
0
1
FF-A
C
S
0
1
FF-B
C
S
0
1
FF-C
C
S
NDA6-111

Figure 3-23. Count detection, relay pyramid.

corresponding relay is energized. With this arrangement, the count in the counter is converted from its digital form to a voltage that is proportional to that count. For example, if an output of 5 volts equals a count of 1, then an output of 10 volts equals a count of 2.

4-4. With a binary count of 11001 or decimal 25 in the counter in figure 3-24, relays K5, K4, and K1 are energized. This gives an equivalent network, as shown in figure 3-25. Resistance and voltage computations for the count are as follows:

- The total resistance, R_o, of the upper ladder is:

$$\frac{11}{R_o} = \frac{1}{R/16} + \frac{1}{R/8} + \frac{1}{R}$$

$$\frac{1}{R_o} = \frac{16}{R} + \frac{8}{R} + \frac{1}{R}$$

$$\frac{1}{R_o} = \frac{25}{R}$$

$$R_o = \frac{R}{25}$$

- The total resistance, R_f, of the lower ladder is:

$$\frac{1}{R_f} = \frac{1}{\frac{R}{4}} + \frac{1}{\frac{R}{2}}$$

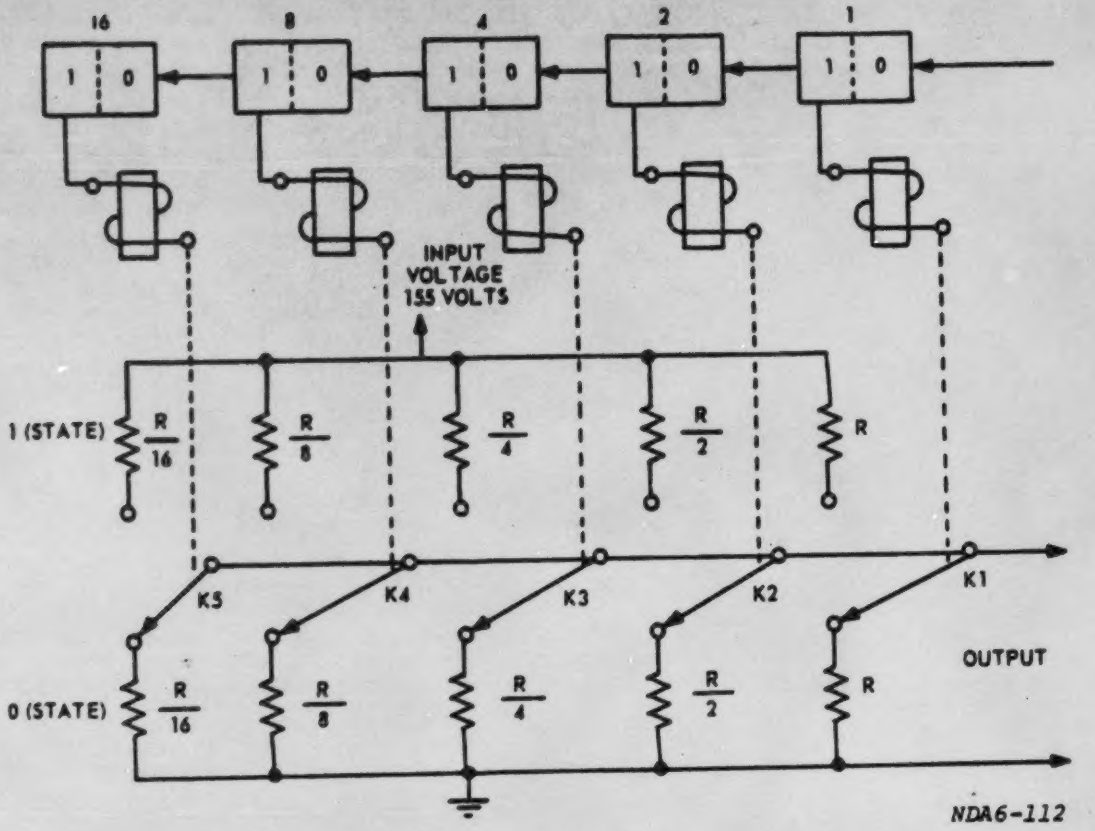

16
8
4
2
1
1 0
1 0
1 0
1 0
1 0
INPUT VOLTAGE 155 VOLTS
1 (STATE)
R/16
R/8
R/4
R/2
R
K5
K4
K3
K2
K1
OUTPUT
0 (STATE)
R/16
R/8
R/4
R/2
R
NDA6-112

Figure 3-24. Relay ladder, D to A converter.

$$\frac{1}{R_f} = \frac{6}{R}$$

$$R_f = \frac{R}{6}$$

- The total resistance, R_t, of the entire resistor network is:

$$R_t = \frac{R}{25} + \frac{R}{6}$$

$$R_t = \frac{6R + 25R}{150}$$

$$R_t = \frac{31R}{150}$$

- The voltage E_{out} is:

$$E_{out} = \frac{R_f}{R_t} \times 155V$$

$$E_{out} = \frac{\frac{R}{6}}{\frac{31R}{150}} \times 155$$

$$E_{out} = \frac{R}{6} \times \frac{150}{31R} \times 155$$

$$E_{out} = 125 \text{ volts}$$

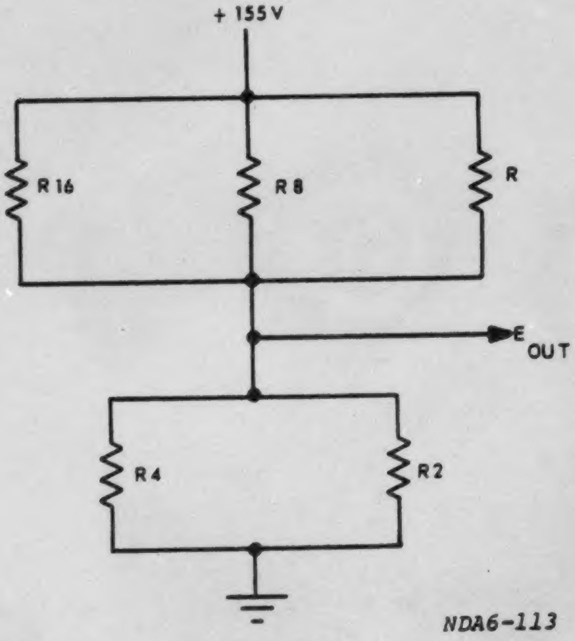

+ 155 V
R 16
R 8
R
E OUT
R 4
R 2
NDA6-113

Figure 3-25. Equivalent circuit for figure 3-24 with a count of 25.

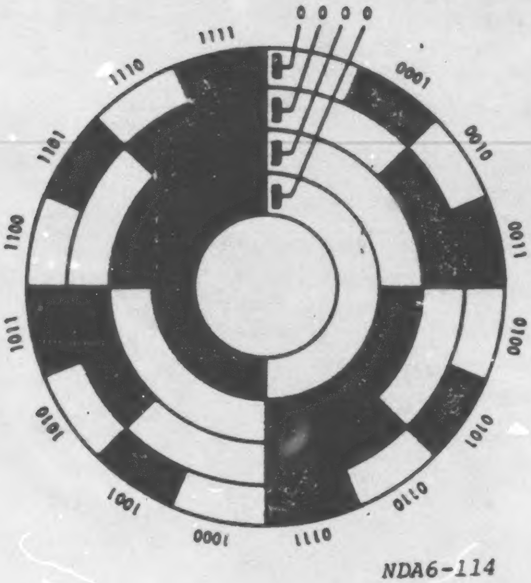


Figure 3-26. Analog-to-digital converter.

- The ratio between R_f and R_t is:

$$\frac{R_f}{R_t} = \frac{\frac{R}{6}}{\frac{31R}{150}}$$

$$\frac{R_f}{R_t} = \frac{R}{6} \times \frac{150}{31R}$$

$$\frac{R_f}{R_t} = \frac{25}{31}$$

4-5. The ratio of R_f and R_t should have pointed out one thing to us. That is, if we are only concerned with computing the voltage out of this D to A converter, all we have to do is the simple computation that follows:

$$E_{out} = Ea \frac{R_f}{R_t}$$

where

Ea = applied voltage
R_f = count in counter
R_t = maximum count of counter

Therefore, the problem just solved would be simplified as follows:

$$Ea = \frac{R_f}{R_t}$$

$$= 155 \times \frac{25}{31}$$

$$= 125 \text{ volts}$$

4-6. **Analog-to-Digital Converter.** Not all inputs to a computer are in digital form. Some of the inputs are in the form of analog voltages that represent quantities. Some analog quantities that are applied directly to a computer represent speed of movement, speed of rotation, position of a shaft, elevation, temperature, pressure, and humidity. Before this information can be used by a digital computer, it must be converted to digital form. An analog-to-digital converter (called A to D) does this job.

4-7. A type of converter that converts a shaft position (this position determined by an analog voltage) to a digital number is shown in figure 3-26. There are many different types of converters used for this purpose. The one explained is typical of some in use. The conducting material in the disk in figure 3-26 is shown in the dark areas, and the nonconducting material is shown in the light areas. Contacts are arranged into as many channels as there are digits in the largest binary number that is to be coded. A brush is in contact with each channel on the disk. A voltage source is used in the circuit so that if a brush is in contact with the conducting material, a binary 1 is detected. If the brush is in contact with the nonconducting material, a binary 0 is detected. The binary number detected in the position shown in the figure is 0000. As the shaft rotates counterclockwise, the brush in the outer channel makes contact with the conducting material. Now the binary count detected is 0001. The analog voltage is controlling the shaft (therefore the disk's) movement. As the converter continues to rotate, the binary count detected increases, as shown around the circumference of the disk. This digital information may now be fed into the computer.

5. Encoder

5-1. An encoder is a network in which one input produces a combination of outputs. It is commonly found at the input of a computer and is used to convert information to a form acceptable by the computer. Figure 3-27 illustrates an example of a simple encoder. The input to the encoder matrix is a keyboard. As the keys are depressed, the spring contact moves down and makes contact with a bar which has a positive potential applied. The spring contact passes this potential to the diode matrix. The matrix is made up of eight OR-gates, each having four diodes. The outputs are signals that represent a binary configuration for the

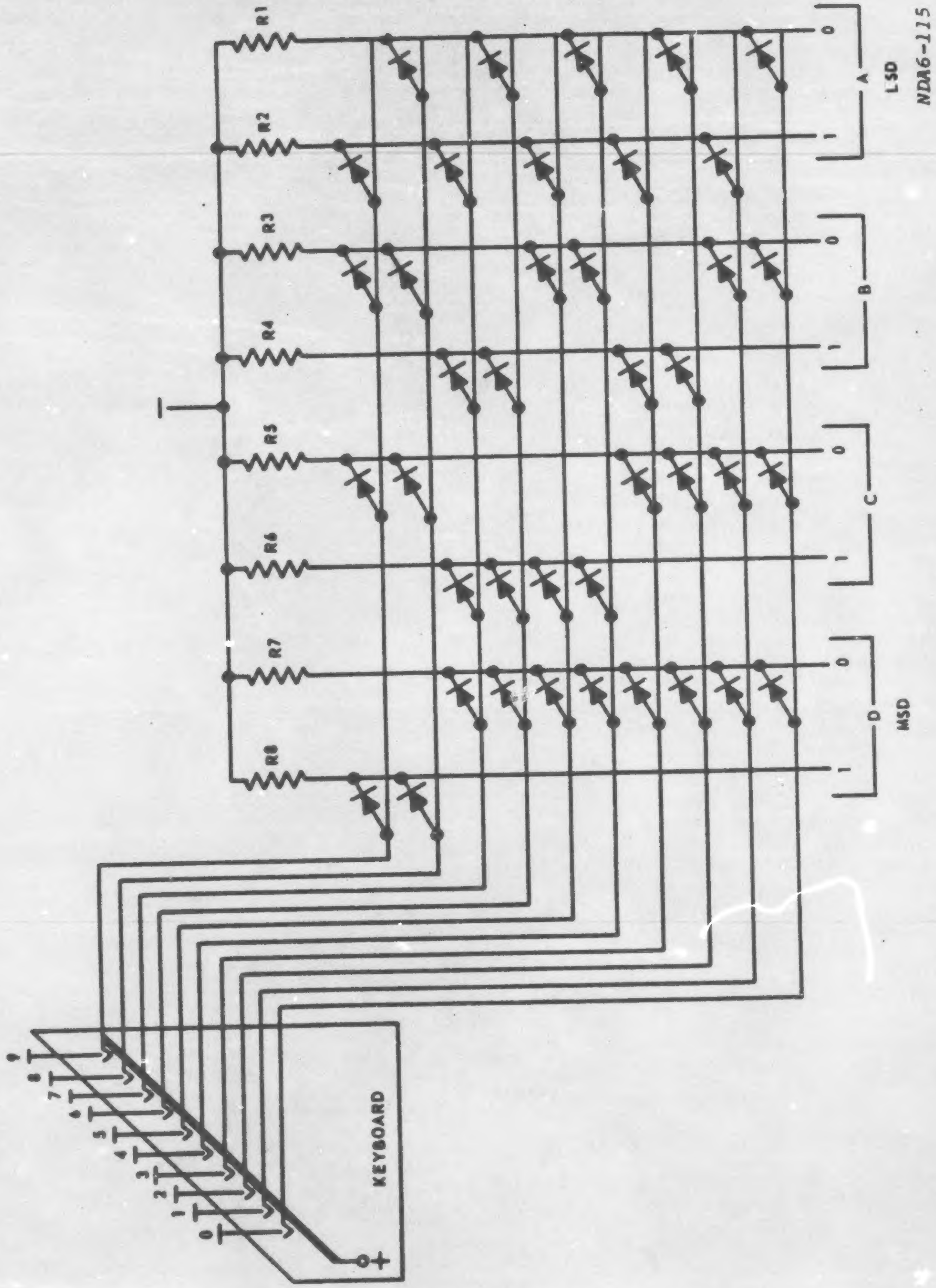
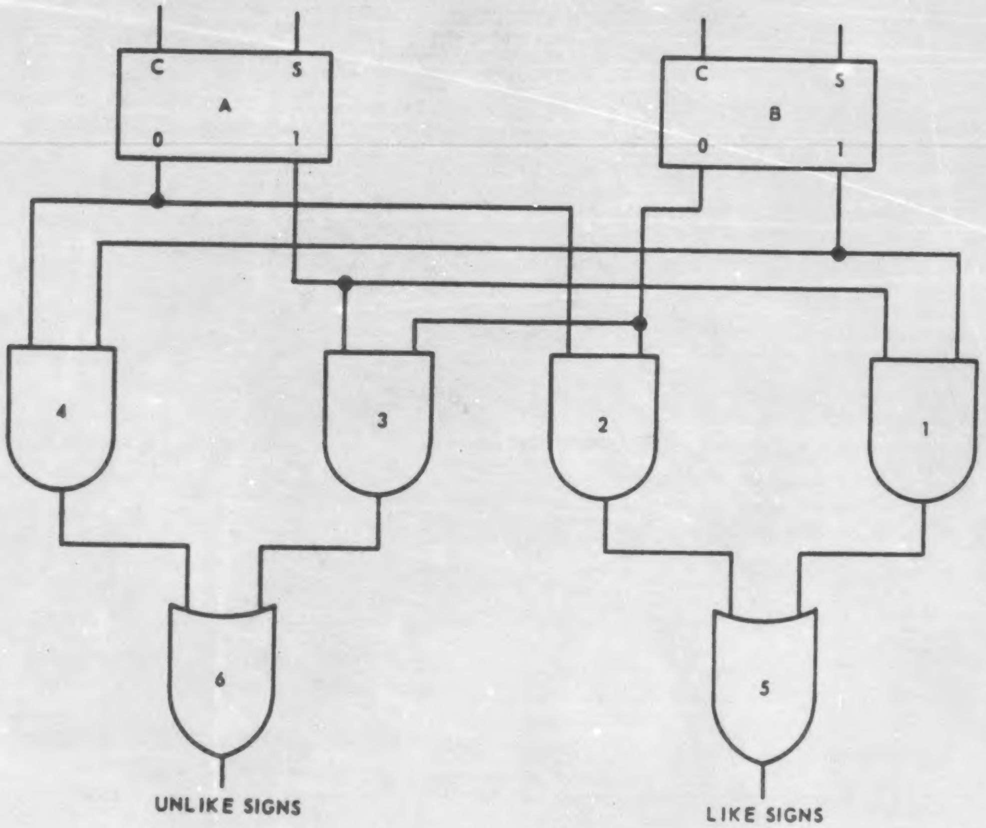

R1
R2
R3
R4
R5
R6
R7
R8
0
1
0
1
0
1
0
1
A
B
C
D
LSD
MSD
NDA6-115
KEYBOARD
0
1
2
3
4
5
6
7
8
9
+

Figure 3-27. Encoder.



NDA6-116

Figure 3-28. Sign comparator.

decimal number represented by a key. The output lines are grouped into four pairs, where each pair represents a binary digit. Pair A generates the LSD, pair B generates the 2^1 bits, pair C generates the 2^2 bits, and pair D generates 2^3 bits.

5-2. To see how an output is obtained, let's see what happens if the key that represents 5 is depressed. The positive potential of the bar is felt on the anodes of the four diodes tied to the 5 line (refer to fig. 3-27). With this potential applied, resistors R7, R6, R3, and R2 have current through them. This means that the activating potential will appear on the 0, 1, 0, and 1 of the D, C, B, and A pairs of the output line, respectively. This 0101 is the binary configuration for decimal 5. Any one of the input lines puts an activating potential on a combination of four diodes that is different from that of any other input line. Therefore, the encoder shown in figure 3-27 encodes 10 different inputs into binary combinations that represent 0 through 9.

6. Comparator

6-1. A comparator is a device that compares two or more signals and supplies an indication of agreement or disagreement. The arithmetic element of a computer needs such a device to compare the signs of numbers so that the numbers may be added algebraically. Also, in most computers, these devices are used in other decisionmaking circuits. An example of a sign comparator is shown in figure 3-28. The two signs to be compared are stored in F/Fs-A and -B. In this circuit, if the F/F holds a plus sign, its ONE-side output voltage is HIGH and its ZERO-side output voltage is LOW. If it holds a minus sign, its ONE-side output voltage is LOW and its ZERO-side output voltage is HIGH.

6-2. There are only four possible combinations of signs that can be stored in the two F/Fs. These are: (1) F/Fs-A and -B both storing plus signs; (2) F/Fs-A and -B both storing minus signs; (3) F/F-A storing a plus sign and F/F-B storing a minus sign; and

(4) F/F-A storing a minus sign and F/F-B storing a plus sign. These four possible combinations of outputs are applied to four AND-gates as shown in figure 3-28. AND-gate 1 has a HIGH output when F/Fs-A and -B store plus signs. AND-gate 2 has a HIGH output when F/Fs-A and -B store minus signs. AND-gate 3 has a HIGH output when F/F-A stores a plus sign and F/F-B stores a minus sign. AND-gate 4 has a HIGH output when F/F-A stores a minus sign and F/F-B stores a plus sign. OR-gates 5 and 6 provide the final output of this sign comparator. OR-gate 5's output is HIGH only when the signs are alike. OR-gate 6's output is HIGH only when the signs are *not* alike.

CHAPTER 4

Computer Units

COMPUTERS RANGE in size from small units consisting of a few circuits to large complex units involving thousands of circuits. In Chapters 2 and 3, you studied many of the computer circuits that are used to make up various computer units. These computer units are designed to perform a specific function or functions. Once made up, several computer units are interfaced (interconnected) to form a computer system. Regardless of its size, a computer system is made up of five basic units. Our main objective in this chapter is to discuss the function, operation, and characteristics of the three basic computer units which are normally located within the computer main frame. Our first discussion centers around a typical computer system comprised of five basic computer units.

1. Typical Computer Systems

1-1. A block diagram of a typical digital computer system is shown in figure 4-1. The five units (elements) that make up this system include the following:

- Memory.
- Arithmetic.
- Control.
- Input.
- Output.

1-2. Figure 4-2 shows the general organization of the above units within a typical computer system, along with the interfacing of each unit which indicates the flow of information and control signals. The heavy lines are information transfer lines. These lines indicate the information data flow within the system; note that all data flow is from and to the storage unit. The light lines are the system's control lines. Note in particular that all control signals originate in the control unit.

1-3. In the sections that follow, we will describe the function, operation, and characteristics of the three computer units—memory, arithmetic, and control—that are normally referred to as the computer main-frame units. The two remaining units—input and output—are discussed in greater detail in Chapter 5.

2. Memory

2-1. Instructions are required to direct the processing of the data feeding into and out of the computer. Some of the data, and all the instructions, must be stored for later use. Storing this data is the function of the memory. Let us now discuss the data to be stored in memory and some memories that are used.

2-2. Types of Data Stored. Operations in a digital computer are carried out in a step-by-step fashion utilizing information stored in the computer. For this reason, some of the information fed into the computer must be stored for indefinite periods prior to actual usage. The facilities required for storing information in a computer are included in the internal storage (memory) elements. The information normally fed into the computer is of three types:

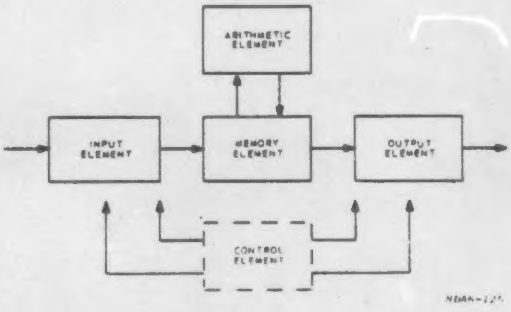


Figure 4-1. Block diagram, computer units.

256

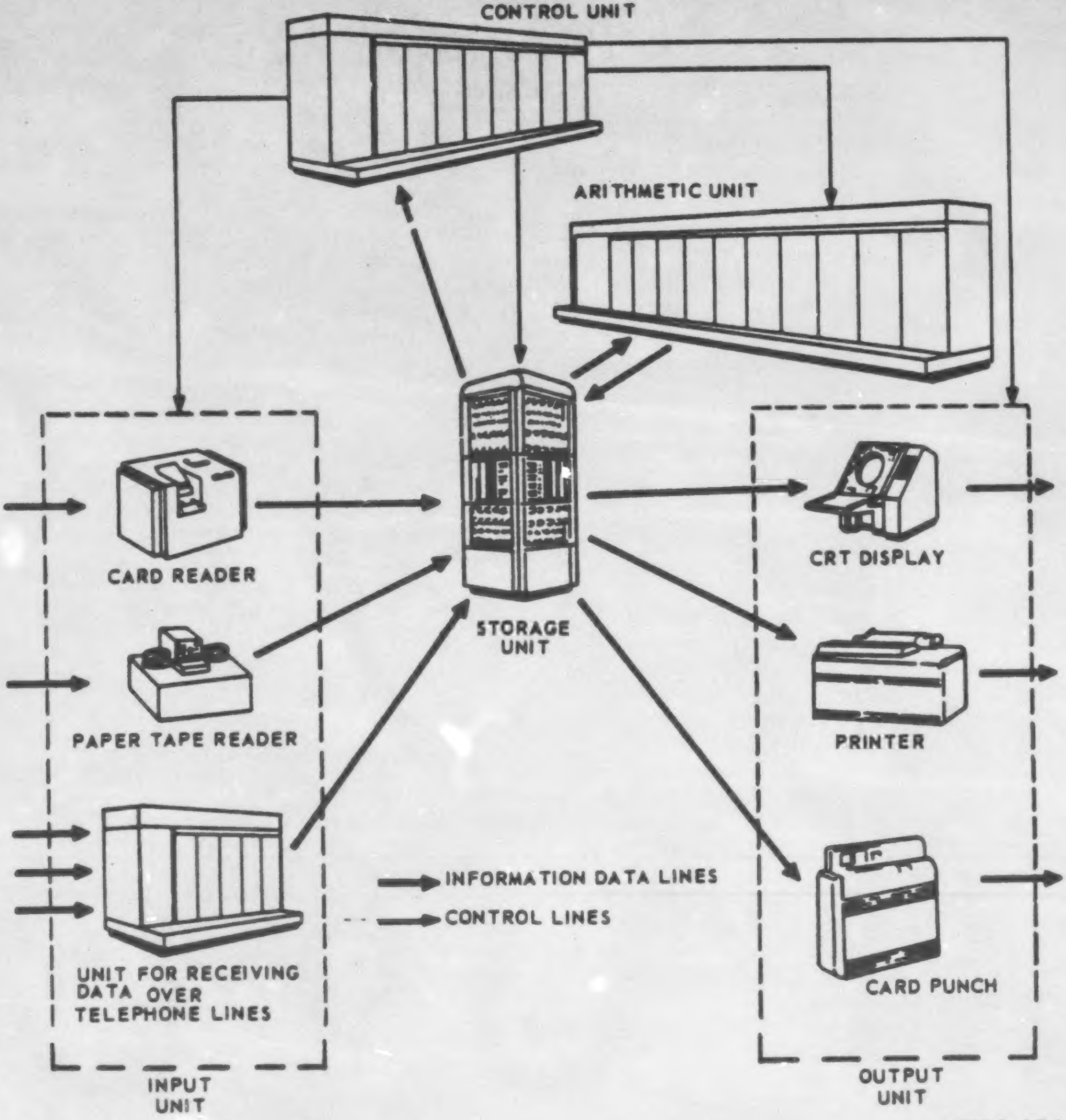

CONTROL UNIT
ARITHMETIC UNIT
STORAGE UNIT
CARD READER
PAPER TAPE READER
UNIT FOR RECEIVING DATA OVER TELEPHONE LINES
INPUT UNIT
CRT DISPLAY
PRINTER
CARD PUNCH
OUTPUT UNIT
INFORMATION DATA LINES
CONTROL LINES
NDA6-124

Figure 4-2. Organization of a typical digital computer.

(1) Reference data (constants).
(2) Instructions for performing the particular operations required (the program).
(3) Particular items to be processed (variable input data).

2-3. *Reference data.* This type of data is stored for future use. For example, if the computer is used in an air defense system, the reference data would probably include such items as radar site locations, aircraft locations, boundaries, and math tables. Such data is used over and over for successive computer calculations. It would be impractical to feed this same information into the computer for each new calculation. If the storage element of the computer retains such data indefinitely and quickly presents individual items each time they are needed, problems are solved much faster. A second example of a constant would be a supply system's custodian account number. This number is assigned to the

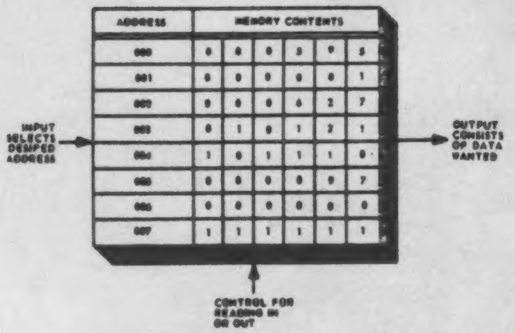


Figure 4-3. Storage unit.

supply custodian of a section, and it allows only that person or his representative to withdraw supplies for the section's account.

2-4. *Computer program.* Also stored in the memory is the computer's program. The program is the set of instructions (repertoire) for performing the particular computer system's tasks. With a common program, and common reference data in advance, the only additional data required to perform the computer's tasks are the variable data to be operated upon.

2-5. *Variable input data.* This is the data that is continuously changing. An example of this type of data is a jet fighter flying at 40,000 feet heading west at 1200 miles per hour. If the aircraft does not change its heading, only the speed changes the input data (the aircraft location will change at a rate of approximately 1 mile every 3 seconds). The program must use the reference data to set up an intercept point under these conditions; then it must check each new input to see if the point is still valid. Should the fighter change directions or reduce its speed, a new intercept point must be calculated. The input data may then be stored in the memory for a short time and also stored in some external storage device for later use as a record of the intercept.

2-6. Another example of variable input data would be the information for an account number in a supply system's computer. Each time a part is used, the computer must update all the information related to the part and the account number. For example, in a given work center, each section is allotted a given amount of money for parts, and the money is placed in the section's account (similar to a checking account). A particular section needs a 2N404 transistor, which is ordered by the supply custodian. The supply computer issues the part and charges it to the section's account by subtracting the cost of the part from the account. Also, it notes the number of transistors remaining in stock, and, if the supply is down to the reorder point, the computer initiates a reorder action.

2-7. Memory Unit Considerations. In order to store the three types of information discussed above, in binary form, the storage (memory) media must have at least two stable states. A memory unit must also be capable of "remembering" (storing) a great many program words and data words, and these words must be made available to the other computer components almost instantaneously. Indeed, without fast, automatic, and reliable processing of data into and out of the storage element, problem solving with a computer would be little more efficient than working with hand-operated calculators and reference tables. Let's consider some of these requirements individually.

2-8. *Addressable memory.* All storage elements have some basic characteristics that are similar. They always contain a number of storage locations, each of which stores a specific amount of data. Each of these locations is assigned a specific number called an "address," so that it may be selected by the computer either for insertion or extraction of data. For instance, in the diagram of the 8-location memory shown in figure 4-3, the addresses are shown on the left, opposite their actual contents. To refer to the number 10,121, the computer would select the location whose address is 003.

2-9. *Memory capacity.* Another important requirement of the memory is capacity. In large-scale computers, it may not be feasible to include all the required storage area in the main memory. Therefore, an auxiliary (additional) storage device is provided in addition to the main memory. This releases the main memory for storage of the most important program instructions and data required for specific computer tasks.

2-10. *Memory access time.* Another very important requirement of the memory unit is the speed (time) with which program instructions words and data words can be read

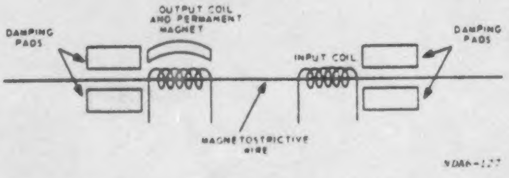


Figure 4-4. Magnetostrictive delay line.

from and written into the storage media. This time, called *access time*, limits the speed of operation that a computer system can perform its assigned tasks.

2-11. **Types of Memory Devices.** There are various types of memory devices that provide a reasonable access time and storage capacity. Because of the many types in use today, our discussion is limited to the four most common types used in Air Force computer systems. The four to be discussed include:

(1) Magnetostrictive Delay Lines.
(2) Ferrite Core Memory.
(3) Thin-Film Memory.
(4) Solid-State Memories.

2-21. **Magnetostrictive Delay Lines.** Magnetostrictive delay lines were one of the first devices used as a memory. It operates on the principle that certain materials change lengths when placed in a magnetic field. This phenomenon is called *magnetostriction*, and it is pronounced in nickel which becomes shorter in the presence of a magnetic field. Another material called *permalloy* gets longer when it is placed in a magnetic field.

2-13. *Construction.* The basic construction of a magnetostrictive delay line (MDL) is shown in figure 4-4. It is constructed by wrapping coils around the ends of a bar (wire) of ferrous material. The input coil (transmitter) creates a magnetic field that

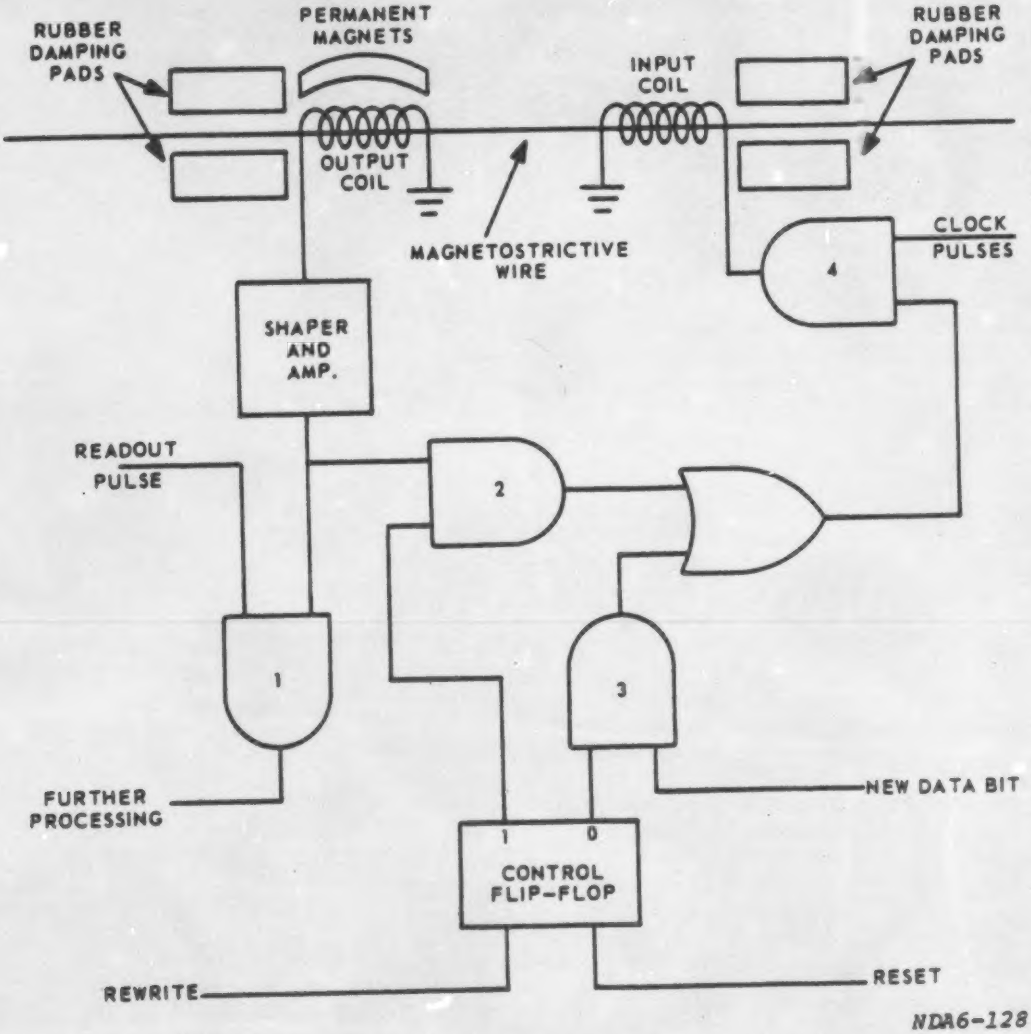

RUBBER DAMPING PADS
PERMANENT MAGNETS
INPUT COIL
RUBBER DAMPING PADS
OUTPUT COIL
MAGNETOSTRICTIVE WIRE
CLOCK PULSES
4
SHAPER AND AMP.
READOUT PULSE
2
1
3
FURTHER PROCESSING
NEW DATA BIT
1
0
CONTROL FLIP-FLOP
REWRITE
RESET
NDA6-128

Figure 4-5. Magnetostrictive delay line operation.

causes magnetostriction (shock waves) in the material. As this shock wave travels through the line, it is detected by the output coil. The MDL delay is determined by the location of the output coil assembly. The output coil assembly is moved along the length of the line to adjust the storage time. When the shock wave has been detected by the output coil, it is necessary to absorb the shock wave to prevent reflection. This is accomplished by clamping rubber pads to the ends of the line to absorb the waves, thus preventing reflection of the shock wave back down the line.

2-14. When the input coil is pulsed, it produces a magnetic field which causes the portion of the nickel wire within the coil to become shorter. This change in length is transmitted through the wire as a shock wave which travels the length of the delay line at the speed of sound. This shock wave is accompanied by a change in reluctance. Recall that reluctance is a measure of the opposition a material offers to magnetic lines of force. The permanent magnet at the output coil provides a magnetic field through the coil which is varied by the change in reluctance that accompanies the shock wave. As a result, a voltage is induced in the coil. This action produces an output pulse which is sent to a pulse amplifier and shaper.

2-15. *Clearing the loop.* Now that we have the basic construction of a MDL, let us see how it is put to practical use. Figure 4-5 shows a MDL and the representive external circuitry required to make it function as a recirculating memory device.

2-16. A data bit in the delay line continues to recirculate through the line for as long as it is desired to store this bit. The bit can be read out without destroying it; thus, the line has nondestructive readout characteristics. When new information is to be stored, or when it is desired to destroy the old information, the data in the line is prevented from recirculating and disappears. This action is referred to as "clearing the loop" or "resetting to ZERO." The circuit that controls this function is the control flip-flop.

2-17. Notice that the ONE-side output of the control F/F is fed to AND-gate 2, and the ZERO-side output is fed to AND-gate 3. When the control F/F is SET and a data bit is present in the delay line, the pulse from the output coil is fed back through the line again. This recirculation continues as long as the control F/F remains in the SET state. When the control F/F is reset (placed in the ZERO state), AND-gate 2 is deconditioned and the data bit is lost, since it cannot get back to the input coil. Clearing the loop is usually done to prepare the delay line for entering new information.

2-18. *Write operation.* Let us start with a clear loop and write a data bit into the delay line memory. We first clear the control F/F to the ZERO state. The ZERO side of the control F/F conditions one leg of AND-gate 3. The data bit is now applied to the other leg of gate 3. The output of gate 3 feeds one leg of the OR-gate, and the OR-gate feeds one leg of gate 4. When the clock pulse arrives at the other leg of gate 4, the data bit is then gated into the input coil. The data bit is now represented by a shock wave that travels the length of the delay line.

2-19. If the data bit is to be stored, there are two other things to be done to complete the write operation. The first is to SET the control F/F to the ONE state. The second is that the data bit must arrive back at the input of gate 4 at the same time a clock pulse arrives on the other leg. There is no problem with only one bit; the delay line can be adjusted so that it will be rewritten with any clock pulse. However, a storage device that stores only one data bit is of little value in a computer system. Now let us store more information in the delay line and see how the operation compares with the one bit stored.

2-20. Let us say that the delay line has a 2048-microsecond delay. How many words (or bits) will the delay line store? What determines the number of bits it will store? The storage capacity of the delay line memory is determined by two things. First is the length of the delay line; second is the pulse repetition rate of the clock pulse. The delay time of the delay line we are going to use is 2048 microseconds. Let us use a clock pulse with a pulse repetition time of 1 microsecond. This will allow the delay line to store 2048 bits of information. The word length may be 4, 8, 16, or 32 bits long. However, the total number of words should not include more than a total of 2048 bits.

2-21. Recall that with the one bit we could use any clock pulse to rewrite that bit in memory, the only requirement being the delay of the delay line being equal to the pulse repetition time or multiple of the pulse time. Using the full storage capacity changes this requirement. We are now going to store 2048 bits, and the delay must be 2048 microseconds from the time the data bit leaves the output of gate 4 (see fig. 4-5) until it returns to the input of gate 4 in order to be rewritten.

2-22. The start of the write operation is the same as storing the one bit (refer to fig.

4-5). The control F/F is RESET (ZERO state) which conditions gate 3. The first data bit will produce an output from gate 3, through the OR-gate to condition gate 4, out of gate 4 to the input coil, and on to the magnetostrictive wire. This same operation continues until bit 2048 is reached. After bit 2048 is gated through gates 3 and 4, and into the delay line, the control F/F must be SET (to the ONE state) before the first data bit arrives at gate 2. If the control F/F is not SET in time, the data is considered destroyed because it has not passed through gate 2. A second problem that might occur, and the most likely, is timing. Let us say the timing is 2047 microseconds. What would result? The first data bit would be lost because it is not at gate 2 ready for rewrite when bit 2048 is being stored. The result is that the first data bit is lost because the delay line now stores 2047 bits, not 2048.

2-23. From the above discussion, we see that timing is critical in the delay line memory. This is why the output coil is adjustable along the length of the wire. If the timing is off, as in the above example, the coil is moved to correct the timing error, so long as the error is not excessive. In this case, the output coil would be moved away from the input coil to increase the delay time. This completes the write operation. Let us now discuss the read operation.

2-24. *Read operation.* The read operation requires only the data and the readout pulse. The clock pulses may be used to gate the data through gate 1 (fig. 4-5) or a "gate pulse" the same width as the data word may be used. Let us see what is required to read out one word from memory.

2-25. One method might be to count the clock pulses, starting with data bit one and going to bit 2048. Let us say that 2048 bits are equal to 256 eight-bit words. If the second word is to be read out, the counter would count the first eight clock pulses, then send the next eight pulses to gate 1. The second method might be to use a "gate pulse." The gate pulse would go active at the end of the 8th clock pulse and stay active until the end of the 16th clock pulse. The timing here is critical just as it is in the write operation.

2-26. *Magnetostrictive delay line configuration.* The use of the delay line determines its configuration. Serial operation can be provided by a single delay line, and a serial parallel operation can be provided by stacking several delay lines together. The controlling and addressing of the delay line also depends on the operation desired.

2-27. *Advantages and disadvantages.* The most important advantage of the magnetostrictive delay line is that it is relatively inexpensive when compared to the ferrite core and the thin-film memories. Excessive access time and volatile storage are two disadvantages of the delay line memory. Recall that access time is the time required for a computer to locate data or an instruction word in its storage section and transfer it to its arithmetic section where the required computations are to be performed. Recall also that volatile memory is any memory that can retain (or store) information *only as long as energizing power is applied.* The ferrite core, our next subject, is one means of overcoming the disadvantages of the delay line.

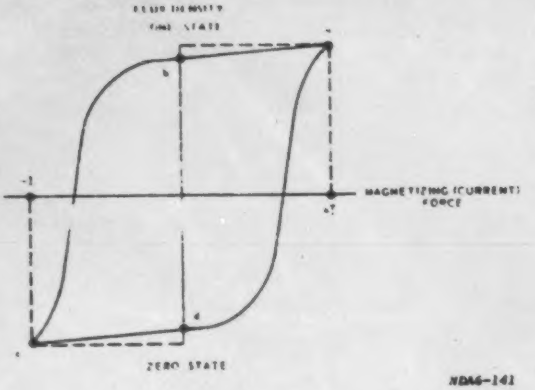


Figure 4-6. Ferrite core hysteresis looop.

2-28. Ferrite Core Memory. The ferrite core memory enjoys wide use in present-day, high-speed computers. In fact, the ferrite core is probably the most satisfactory storage device for use as an internal computer memory. It has a fast access time, is addressable either sequentially or at random (any sequence), and has a high order of reliability. The systems in which ferrite cores are used are referred to as coincident-current memories.

2-29. *Ferrite core principles.* Since the ferrite core is the main part of a coincident-current memory system, let us briefly review the characteristics of this storage device. The familiar hysteresis loop for a ferrite core is shown in figure 4-6. From it, you can see two characteristics of the core that make it a useful binary storage device: (1) its ability to remain in one of two stable states, and (2) the rapid switching action from one state to the other with the application of a magnetizing force. Notice that the slope of the top and bottom line of the curve is gradual; this indicates that the core holds

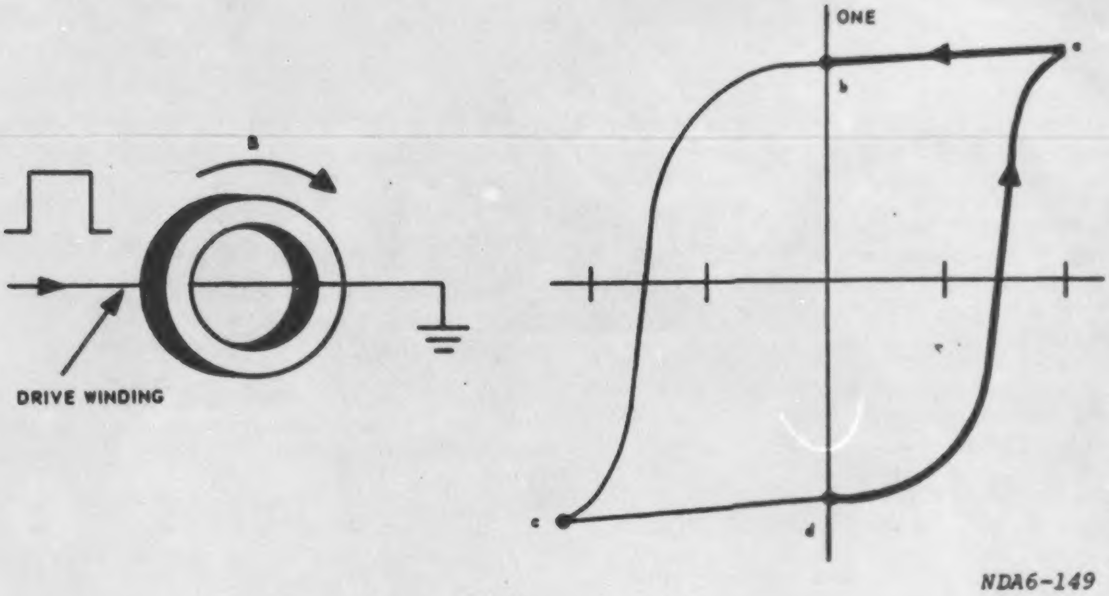


Figure 4-7. ONE writing.

most of its magnetism after the magnetizing force is removed. Also, notice how steep the sides are; this indicates that the core switches rapidly from ONE to ZERO (b to c) and from ZERO to ONE (d to a).

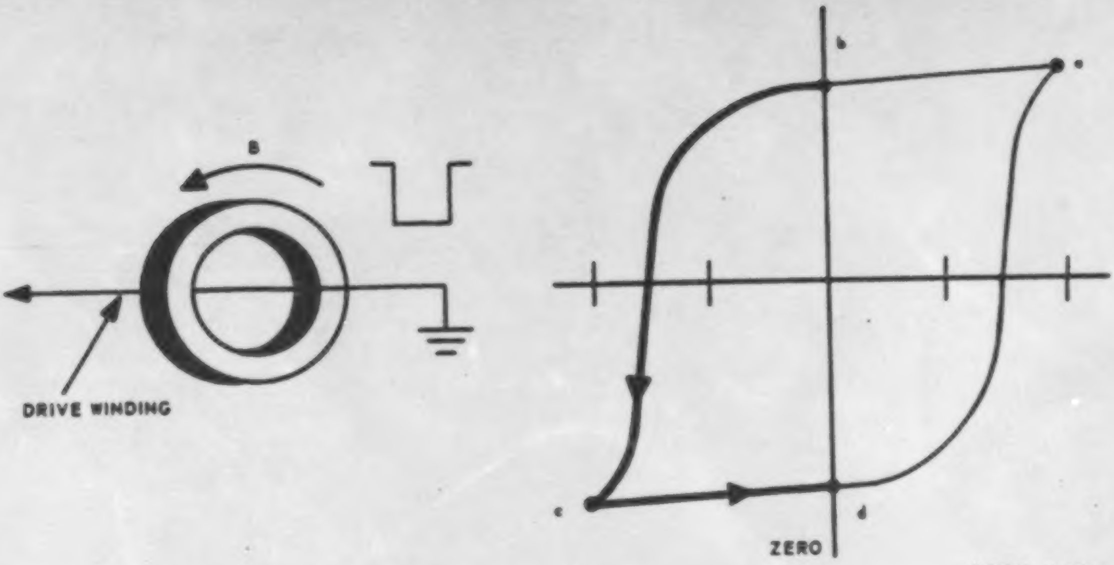
2-30. Look again at figure 4-6 and locate point a on the hysteresis loop. This point represents the flux density of the core when a magnetizing force of +I is applied. When this force is removed, the flux density drops to the value indicated by point b. Throughout our discussion, this action is referred to as having placed the core in the ONE state. When a force equal to -I is applied to the core, it becomes magnetized in the opposite direction. The flux density is indicated by point c on the curve. If this force is removed, the density drops very little to point d on the curve. In our discussion, this action is referred to as having placed the core in the ZERO state.

2-31. Assume that the core contains a ZERO and you wish to switch it to a ONE. To do this, it is necessary to pass enough current through the core's drive windings to cause the flux to reverse direction. This is shown on the loop in figure 4-7 as a change from point d to point a. Current flowing in the direction necessary to write a ONE into the core is also illustrated in this figure. While current is flowing in this direction, the core is saturated; that is, further increase in current will not cause a change in flux in the core point a. When the current is removed, the flux drops back to point b and the core retains residual magnetism that is almost equal to the saturation flux. The core remains in this condition until it is pulsed again. If the core had contained a ONE and you attempted to write a ONE into it, the flux would have changed from point b to point a and then back to point b, a very slight change in magnetic flux.

2-32. Now assume that you wish to set the core back to the ZERO state. To do this, pass current through the drive winding in the opposite direction as shown in figure 4-8. This drives the core to saturation in the opposite direction, causing the flux to change from b to c. Upon removal of the drive current, the flux drops from c to d and remains there. The core is now in the ZERO state.

2-33. *Addressing.* Ferrite cores in a memory are normally arranged as shown in figure 4-9. This type of arrangement is called a matrix; however, in common terminology it is referred to as a plane. Note that there are four rows (X direction) and four columns (Y direction). Therefore, the number of cores in this plane is 4^2 or 16. Memories may be described as 16^2 or 64^2 memory, etc., to indicate the number of cores in a plane. Since each core is capable of storing one bit of information, a 16^2 plane can store 256 bits. As each core represents an address location, some method for selecting a single address must be used.

2-34. To address a core, two drive lines are used. Each line carries one-half the current required to switch a core. Reference X and Y



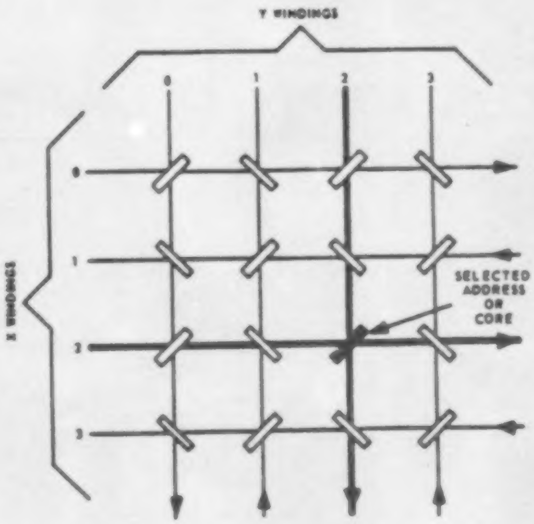
NDA6-147

Figure 4-8. ZERO writing.

lines in figure 4-9; neither current (X or Y) alone is of sufficient amplitude to switch any core it passes through. When the currents applied to the X and Y windings are in the proper direction—that is, when they aid each other—then the intersected core becomes a fully selected core. The two half currents flowing through the windings (X and Y) produce the amount of current required to switch the selected core. Figure 4-9 shows current being applied to the X-2 and Y-2 windings. Assume that the two lines are pulsed in the proper direction with half currents; the selected core (the darkened one in figure 4-9) is at the intersection of the two windings and will be selected.

2-35. Addressing circuits, within an address selection section, select the desired X and Y lines. This section usually consists of a number of flip-flops (called the memory address register), an address decoding network, and current drivers. Figure 4-10 shows an address selection section connected to a memory plane. One-half of the flip-flops and an address decoder control the X part of the selection section. The rest of the flip-flops and a second address decoder control the Y part of the selection section. The two parts operate exactly the same and are controlled together to select one X line and one Y line simultaneously. The selection of X and Y lines determines which core is fully selected.

2-36. In figure 4-10, assume that a binary 1010 is fed to the memory address register. The output from the memory address register flip-flops is fed to the X and Y address decoders (10 to the X decoder and 10 to the Y decoder). These decoders are diode matrixes which decode the address register output. The output of the X and Y decoders determines which X and Y lines are pulsed by the current drivers. In this case, since a 10 is fed to the X and Y current drivers, lines X-2 and Y-2 are pulsed. When these selected lines are pulsed, the selected core is at the



NDA6-148

Figure 4-9. Ferrite core matrix.

intersection of the two pulsed lines as indicated in figure 4-10.

2-37. The addressing process for either writing or reading is the same except for the direction of current flow in the X and Y windings. During the read cycle, current flows in the opposite direction to that of the current during the write cycle. This method of addressing is not the only one in use within computers. The design of the address selection section and the memory address register flip-flops varies according to the type of addressing desired, such as consecutive, up-down, and random.

2-38. A coincident-current memory array is constructed by stacking a number of ferrite core planes to form a stack. The addressing is the same as that for one plane, and all planes in the stack are addressed simultaneously. This is accomplished by connecting similar coordinate lines of all planes in series. For example, the X-2 coordinate lines of all planes are connected in series to form one X-2 line for the memory. The Y-2 lines are also connected in series to form one Y-2 line for the memory.

2-39. *Read operation.* The operation of any core memory involves reading out of and writing into the core memory array. Reading means sensing the flux state of a core to determine if it holds a ONE or a ZERO. This is done by driving the core to its ZERO state. This is also referred to as "writing" a ZERO.

2-40. The flux of a core is sensed by the use of a winding, as shown in figure 4-11. Appropriately, it is called the *sense winding.* Its primary purpose is to detect the presence of a ONE in a selected core. We stated that addressing for reading is the same as for writing, except that current flows in the opposite direction through the selected X and Y lines. With this in mind, look at figure 4-11 to see how the reading process is accomplished. Assume that the X-0 and Y-0 lines have been selected and pulsed in the proper direction (write current flows with the arrows, read current against the arrows). The core intersected by these two lines is the selected core. If the core contains a ONE, it is

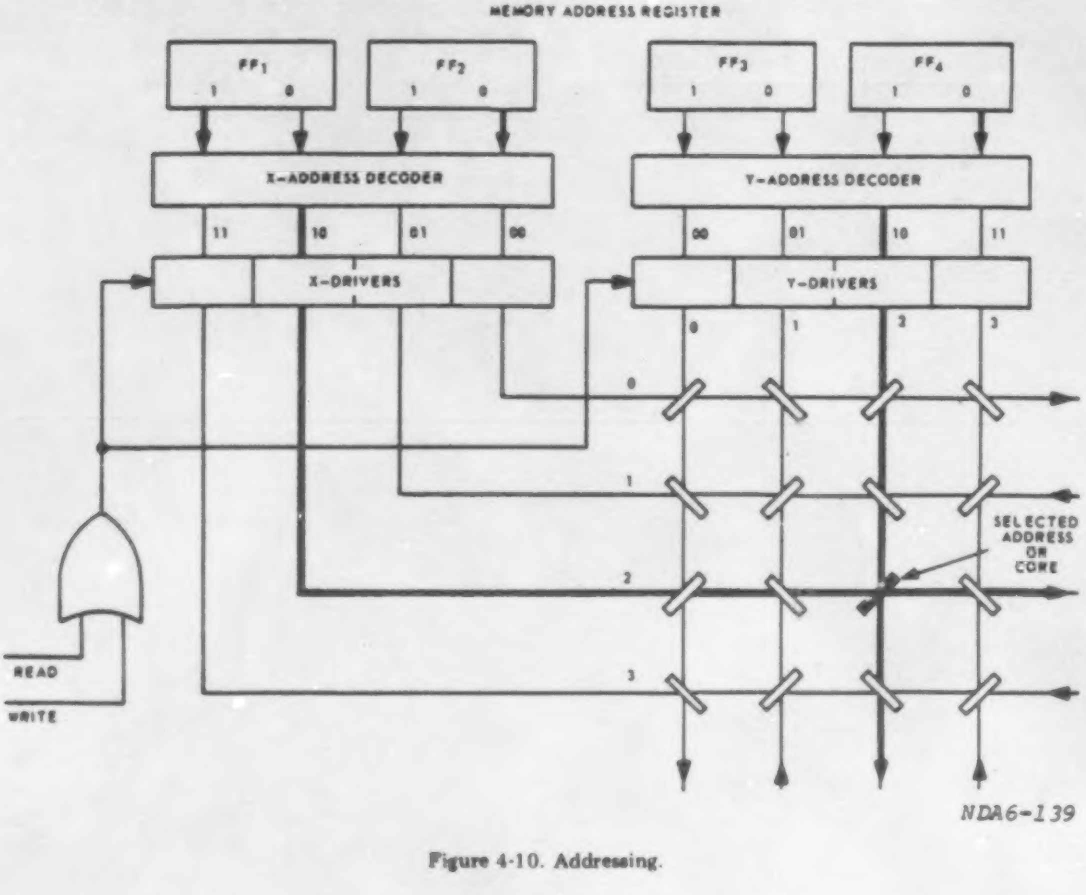


Figure 4-10. Addressing.

attempt to write a ONE in the selected core; but at the same time these lines are pulsed, a pulse is applied to the inhibit winding, causing current to flow in the direction of the arrow. The current through the inhibit winding is opposite to the flow through the Y line. This cancels the effect of the Y line. As a result, the selected core feels only the half-select current of the X line and does not switch. Thus, the core remains in the ZERO state.

2-46. Four-Plane Ferrite Core Memory. Now that we have discussed the principles of reading, writing, and addressing individual cores within a plane, let us stack four planes together to make a memory. Then, let us connect this memory to the circuits necessary to perform the memory cycle function. Foldout 1, included as a separate insert in the back of this volume, shows a simplified memory. It contains four planes; therefore, this memory can store a four-bit word. Also, the planes are 4^2; that is, there are four X lines and four Y lines. This means that there are 16 cores per plane, and a total storage capacity of the memory is 16 four-bit words.

2-47. We said before that one memory cycle is composed of a read and a write portion. With this in mind, we will go through the read portion first and then the write portion. This is the order in which they occur within a memory cycle.

2-48. *Read.* At the beginning of each memory cycle, the memory register and memory address register (MAR) are cleared (set to ZERO). At this time, the read portion of the memory cycle begins, and new address information is transferred to MAR. The outputs from both the ONE and ZERO sides of the four flip-flops are applied to the X and Y lines that are to be pulsed by the read current. Let us assume that X-3 and Y-3 are the selected lines and the read current pulse has begun. The read pulse is normally present for the first half of the memory cycle. For example, if your equipment has a 6-μsec memory cycle time, the duration of the read cycle is approximately 3 μsec.

2-49. Now follow the X-3 and Y-3 lines from the diode decoders through plane 1 of foldout 1. Notice that the two windings intersect the core in the upper left corner of plane 1. This is the selected core. The two half-currents flowing in X-3 and Y-3 are in the same direction, and they aid each other in producing a full-select current through the selected core. Now follow the current path of the two pulsed lines through the remaining three planes. Which core in each plane is pulsed? Is the selected core in the remaining three planes identically located to that of the first plane? The answer is yes—the same core in each plane is pulsed.

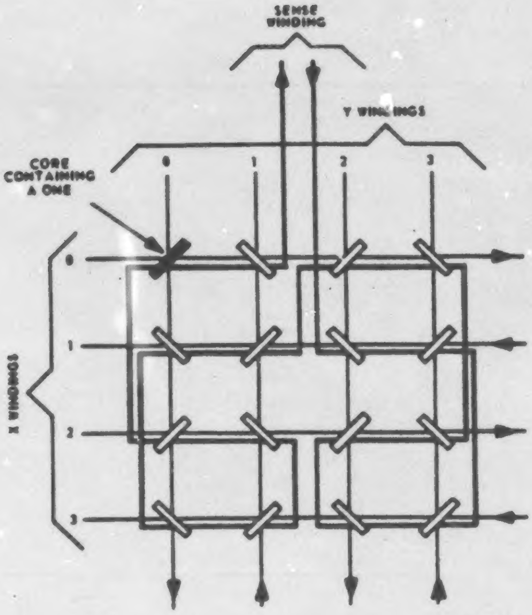
2-50. Before we go any further with this explanation, let us put a binary word into the selected core locations in order to have something to read out. This is necessary to see how the sense windings operate. Assume that the binary word 1101 is in the selected location. Therefore, the selected core in plane 1 contains a ONE (1); plane 2, a ZERO (0); plane 3, a ONE (1); and plane 4, a ONE (1).

2-51. Since this is a read cycle, the current flow from the decoders through the cores is opposite to the direction shown by the arrows. The arrows show the direction of current flow for writing a ONE, and reading is the process of writing ZEROs in all cores. Therefore, when the selected core of each plane feels full-select currents, it is switched to the ZERO state. Looking at foldout 1 and keeping in mind the binary configuration of our selected word (1101), you can see that the sense (green) windings for planes 1, 3, and 4 feel an induced voltage. The selected core in plane 2 contained a ZERO; hence, it does not switch and, for all practical purposes, no voltage is induced into the sense winding. Actually, the core is driven to ZERO, causing a change in flux that is so slight that the voltage induced in the sense winding is not amplified by the sense amplifier.

2-52. The sense winding for each plane is connected to a sense amplifier which is cleared prior to each read cycle. The purpose of the amplifier is to amplify the voltage pulse induced in the sense winding when a core switches from the ONE to the ZERO state. The sense amplifier is gated; that is, during the time the amplifier is pulsed by the sense winding, a gating pulse must also be applied in order for the amplified sense winding pulse to be passed on to the memory register. This pulse is labeled the "read-sample pulse" on foldout 1. This read-sample pulse occurs at the same time as the read-current pulse. Any time the read portion of the memory cycle occurs, the read-sample pulse gates the amplifiers.

2-53. Since the selected core in plane 2 contained a ZERO and was not switched, the sense winding for that plane felt no induced voltage. From this, you can see that one of the required inputs to sense amplifier 2 is missing, and no output is present to set flip-flop 2 of the memory register. The other three amplifiers have both inputs present; thus, they produce outputs that set flip-flops 1, 3, and 4 of the memory register to the ONE state.

2-54. In summary, during the reading, the



NDA6-135

Figure 4-11. Sense winding.

switched to the ZERO state by the read current. The switching of the selected core induces a voltage into the sense winding. This voltage is then amplified and used to SET that core's associated memory register (MR) to the ONE state, indicating that the core contained a ONE. If the selected core contained a ZERO, no core switching action would take place. A very slight voltage would be induced in the sense winding, but the amplitude of the voltage would not be enough to SET the core's memory register. The indication would then that the core contained a ZERO.

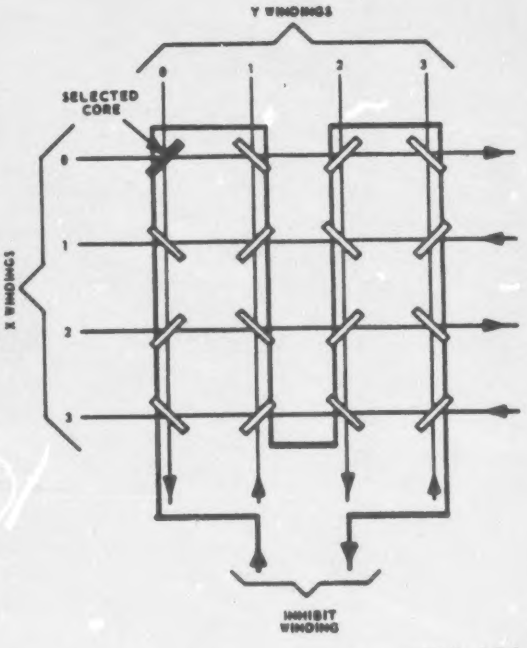
2-41. The construction, or threading pattern, of sense windings through a ferrite array varies with engineering design of the manufacturer's choice, but the basic operation is the same. One method can be seen in figure 4-11. Normally, there is one sense amplifier (SA) and sense winding for each digit plane. The sense winding passes through each core of its associated plane in such a manner as to minimize capacitive and inductive coupling between itself and other windings of the plane.

2-42. *Write operation.* Writing consists of either driving a selected core to the ONE state or inhibiting the driving of a core to the ONE state when a ZERO is to be written. Remember that reading consisted of driving a core to the ZERO state to determine whether it held a ONE or a ZERO. Writing is the reverse of reading; the selected lines are always pulsed in such a direction as to write a ONE in the core. Since you do not always want to write a ONE, it is necessary that some means be used to prevent the writing of a ONE. This is accomplished by the use of an inhibit winding (reference fig. 4-12). Notice that the inhibit winding parallels the Y drive lines.

2-43. *Complete memory cycle.* A typical core memory cycle consists of a read portion followed by a write portion. Taken together, these operations are referred to as a memory cycle. The memory cycle is arranged so that the data word which has been read may be reinserted in the same location during the write portion of the cycle.

2-44. Assume that you wish to write a ONE in core X-0, Y-0. The core is in the ZERO state, since it has just been read (remember that a write is always preceded by a read). To write the ONE, the X-0 and Y-0 lines are pulsed, and current flows in the direction of the arrows. This switches the core to the ONE state.

2-45. Now assume that you wish to write a ZERO in a selected core. Assume that the core is already in the ZERO state. Again, the X-0 and Y-0 lines are pulsed, and current flows in the direction of the arrows to



NDA6-134

Figure 4-12. Inhibit winding.

information at the selected address was read out and transferred to the memory register. At the end of the read portion of this memory cycle, the data (1101) is in the memory register awaiting further processing, and the selected cores are in the ZERO state.

2-55. *Write.* You have seen how information is selected and read from a specific location in the core memory array. Also, you learned that when information is read from a core memory location, the selected cores are switched to the ZERO state. It should now be evident to you that a ferrite core array operates on the principle of destructive readout; that is, the information in the selected core locations is destroyed when read out. This is not a desirable characteristic, and some type of compensation must be made for it. This destructive characteristic is compensated for through the use of a write cycle. As previously stated, the read portion uses the first half of the memory cycle. The second half of the memory cycle is used to write the previously read information back into the selected memory location, thus preserving it. The write cycle is also used to write new information into a specified memory location. This function is discussed later.

2-56. Refer again to foldout 1. The information transferred to the MR, during the read portion of the memory cycle, placed ONEs in F/Fs 1, 3, and 4, and a ZERO in F/F 2. Since the memory address register isn't stepped until *after* the memory cycle is complete, the same address (X and Y lines) is still selected. This means the information just read will be written back into the same address it was read from. The write portion of the memory cycle is now initiated by a write pulse applied simultaneously to the address drivers and the inhibit driver gates. The write current pulses the same lines as the read current (X-3 and Y-3). Now current flows in the opposite direction to that of the read current (in the direction of the arrows). Remember, the selected core of each plane is located in the left-hand column, top row. With write current applied, the selected cores now feel full-select current in the direction opposite to that of the read cycle; therefore, these cores should all switch to the ONE state. But, is this what we want? No, since the original information read was 1101, we don't want the core in plane 2 to switch to the ONE state.

2-57. To prevent writing ONEs, the ZERO-side output of each MR F/F is fed to one leg of the inhibit gates. The other input to the inhibit gates is the write pulse. As previously stated, the data in the MR is 1101. This means that the output of the MR ZERO side is 0010 to the inhibit gates. Inhibit gate 2 is the only gate that produces an output to an inhibit driver. All other gates have one leg disabled by the ZERO (low) outputs of the MR. The output of inhibit gate 2 is fed to plane 2's inhibit driver. The output of that inhibit driver is then fed to plane 2's inhibit winding (red line). Follow the current flow of this winding, and note that the current flows from bottom to top in the left-hand column of plane 2 and parallel to the Y-3 winding. Note also that the write current for Y-3 flows from the top to bottom in the same column; thus, the write current through Y-3 and the inhibit current oppose each other. Since these currents are approximately the same amplitude and opposite in direction, the magnetic fields caused by these currents cancel each other, and the selected core of plane 2 feels only half-select current (X-3). This half-select current does not switch the core; consequently, it remains in the ZERO state. Planes 1, 3, and 4 do not receive the inhibit current; therefore, a ONE is written into the selected core on these planes. We have now placed the original information, 1101, back into the selected location we read it out of during the read portion of this memory cycle.

2-58. Now that you have seen how a typical core memory cycle works during its read and write portion, one question has likely entered your mind: How is new information written into memory? The question is a good one. First of all, any time new information is to be written into core memory, a store class instruction is initiated. Recall that the operation of computer systems must be controlled. This controlling is done through the use of control programs that tell the equipment to add, multiply, subtract, store, etc. A store instruction is one that controls the storing of new or revised information into a memory. Let us see how this is accomplished during a memory cycle.

2-59. We know that the MR is cleared (set to ZERO) at the beginning of a memory cycle. Also, we know that the first portion of the cycle (read) reads out the contents of the selected cores by switching them to the ZERO state. In order to write new information (other than that just read) back into the selected cores, it is necessary to keep the information just read from entering the cleared MR. Refer again to foldout 1. Recall that during the read portion of a memory cycle, a read sample pulse is used to gate the outputs from the sense windings through the

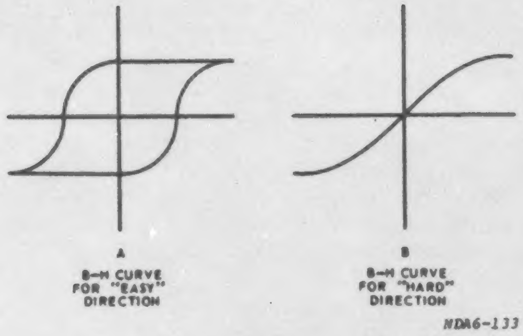


Figure 4-13. B-H curves.

sense amplifiers and into the memory register. What would happen if this read sample pulse were missing or inhibited during the read portion? You can readily see that information read would not enter the MR. At the same time this inhibit action was taking place, new information could be transferred into the MR to await the upcoming portion of this memory cycle.

2-60. Now, assume that a store instruction is programmed and a memory cycle started. This store instruction will inhibit the read sample pulse and, at the same time, cause new information to be transferred into the MR. Then, during the write portion of this same memory cycle, the new information setting in the MR will be written into the selected memory location.

2-61. The method of reading and writing discussed here is but one method. It has been described in general terms so that you can apply the same principles to your specific equipment. The terminology used here may be different from that with which you are familiar. Your equipment may sequentially address each location by means of a counter circuit. The store instruction may be called a load pulse. The read sample pulse may be termed an unload pulse. If you thoroughly understand the principles of addressing, reading, and writing as applied in this particular coincident current memory, you should have no difficulty understanding how the core memory in your equipment or any other equipment functions.

2-62. A memory system that operates much the same as the ferrite-core memory is the thin-film memory. While the operation of the ferrite-core memory is still fresh in our mind, let us cover the thin-film memory and its operation.

2-63. Thin-Film Memory. Thin-film technology is just one phase of the growing field of microminiaturization; other phases are integrated circuits (ICs) and high-density packing of components. A thin-film is a layer of material usually several thousand angstrom units in thickness (1 angstrom unit equals 10^{-8} centimeters), placed on a glass or ceramic substrate. A thin film can be made from materials such as metal, semiconductors, dielectrics, or ferrites. By use of thin-film techniques, a variety of elements and electronic devices such as capacitors, resistors, and magnetic storage elements can be formed. Compared to magnetic core memories and many other memory methods, thin-film magnetic storage memories operate at higher speeds and are less expensive to manufacture.

2-64. *Construction of thin-film memories.* Thin-film memory devices are produced by depositing nickel-iron thin films on a glass substrate while under the influence of a magnetic field. The film thickness of a typical unit is approximately 2000 angstrom units. The resultant thin film has a preferred, or *easy*, direction of magnetization and a reverse, or *hard*, direction of magnetization. For the *easy* direction, the B-H characteristic curve is rectangular; for the hard direction, the B-H curve is linear. Both of these curves are shown in figure 4-13. Recall that information can be stored in a device that possesses a B-H curve such as the one displayed by the thin-film material for the *easy* direction (part A of figure 4-13).

2-65. A magnetic thin-film memory circuit is constructed of a plate of nonconducting material; an array of small, thin disks of magnetic material is attached to this plate. A separate winding is laid across the length and width of each disk. Each disk then becomes a binary cell of the memory, and current through the respective windings appropriately magnetizes each cell. This memory cell array is constructed as a printed circuit. Deposited nickel-iron alloy films compose the magnetic cell material. The cells, in the presence of a magnetic field, assume a direction of magnetization. This direction of magnetization, as previously discussed, has two stable binary states: the ONE state and the ZERO state. An applied magnetic field (in a prescribed direction) causes the cells to switch to the opposite state and remain in that state when the magnetizing force is removed. In short, thin-film memories operate in a manner similar to magnetic core memories.

2-66. *Typical thin-film memory.* Figure 4-14 illustrates a portion of a typical thin-film

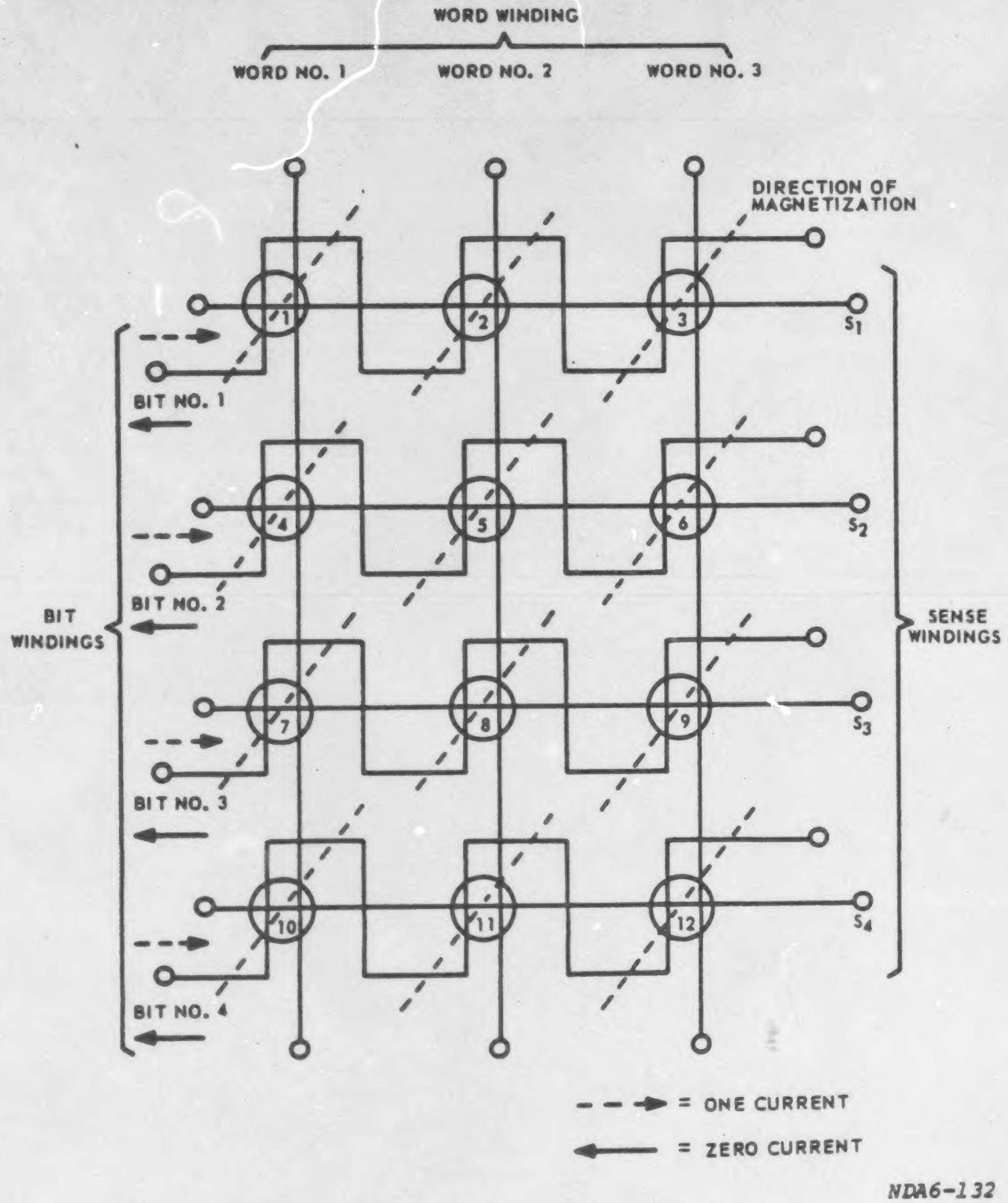

WORD WINDING
WORD NO. 1
WORD NO. 2
WORD NO. 3
DIRECTION OF MAGNETIZATION
1
2
3
4
5
6
7
8
9
10
11
12
S_1
S_2
S_3
S_4
BIT NO. 1
BIT NO. 2
BIT NO. 3
BIT NO. 4
BIT WINDINGS
SENSE WINDINGS
= ONE CURRENT
= ZERO CURRENT
NDA6-132

Figure 4-14. Magnetic thin-film memory.

memory. Three printed wires designated *bit*, *word*, and *sense* windings are required to operate the cells. We should note here that thin-film memory cells do not have holes for threading winding wires, as is the case with magnetic core memories. Note that the *bit* and *word* windings are parallel to each other within each cell. A coincidence of the bit and word winding currents switches the cell to the write position; the direction of the currents determines the ONE or ZERO state of the cell. Readout is initiated by applying a current within the word winding in a direction opposite to the write direction. This typical thin-film memory is characterized by destructive readout; therefore, each memory cycle includes a write portion to rewrite the information back into memory.

2-67. In another type of thin-film memory, buffer registers and associated circuitry may be eliminated through the use of a nondestructive and simultaneous construction method memory. Every cell is composed of a storage film spot and a readout spot for each bit. The storage film spot is made of high-coercivity material, while the readout film spot is made of low-coercivity material. The two spots are spaced closely together with their preferred direction of magnetization at write angles. The permanent state of the storage spot is sensed without a change in its magnetic state (therefore assuming nondestructive properties) through the proper switching of the readout spot. Currents for reading and resetting are lower than the writing current. This difference in currents is derived from the coercivity values of the two types of film spots.

2-68. The size and cost of magnetic devices in recent years have been reduced with new processes and materials used in constructing them. However, the use of magnetic storage devices is being challenged by solid-state memories. Following is a brief discussion of solid-state memories.

2-69. **Solid-State Memories.** A few years ago, the computer was a large vacuum-tube unit using many different types of storage devices. The ferrite-core memory reduced the size and access time of the storage unit. Transistors replaced the vacuum tube, reducing the size, cost, and power required by the computer. Then came the integrated circuits (ICs) replacing the transistors, and now we have large-scale integration (LSI) replacing the IC. LSI reduced the size, cost, and power requirements drastically. With the arrival of LSI, new solid-state memories have been developed that are small, cheap, and require power in the milliwatt range. A common item in wide use today, and a good example of the size and cost of the LSI circuits and memory, is the battery-powered, hand-held calculator with memory storage. Let us discuss briefly two of the solid-state memories that evolved from LSI.

2-70. *Solid-state random access memory (RAM).* The RAM and the ferrite core are identical in operation. The ferrite core and RAM use "X" and "Y" lines to select one location. In the ferrite-core memory, *only one core per plane* is selected at a time with a given address. The same is true for the RAM; that is, *only one "cell" per chip* is selected at a time with a given address. An 8 × 256 bit memory stores 256 eight-bit words (2048 bits total). The same is true of an 8 × 256 solid-state RAM. The RAM requires eight chips of 256 cells each for a total of 2048 cells (or 2048 bits). If this is so, what advantage does the RAM have over the core memory? Why change from the core memory to the chip when they have the same sequence of operation? Let us see what the advantages and disadvantages are when compared to the core memory.

2-71. *Advantages and disadvantages of RAM.* First, let us discuss the advantages of the RAM over the ferrite core. The core memory has current drivers for the "X," "Y," and inhibit lines. Also, the core memory must have sense amplifiers because of the low-level signal on the sense line. This all requires power supplies that supply the memory with the high current needed for its operation. The RAM also uses "X" and "Y" lines for addressing; however, no current drivers are required for their operation. No sense amplifiers are required as the "cells" in some solid-state memories have the ability to feed up to 10 circuits without additional buffers. The RAM's access time is about 50 nanoseconds with power dissipation of about 0.5 watts. From this, you can see that a much smaller power supply will do the job for the RAM. Its relatively small size is also an advantage for the RAM. An example is a 1024-bit RAM on a chip 91 mills by 125 mills. You might ask, "With all this going for it, why not use the RAM in all computers?" The answer to this question brings us to the one main disadvantage of the RAM: It is volatile.

2-72. Recall the statement "The core memory is the best overall storage device for use as computer main memory." The reason for this statement is the ability of the core memory to retain stored data indefinitely with or without power applied. The solid-state RAM must have power to retain data. If the RAM solid-state memory loses power, data is lost. This is a big disadvantage when critical data must be stored. A solid-state memory that overcomes this disadvantage is the read-only memory (ROM).

2-73. *Solid-state read-only memory (ROM).* The read-only memory (ROM) is a storage device that stores data which is not altered by computer instructions; it is sometimes referred to as a *hard-wired program.* Three examples of ROM storage devices are (1) magnetic core memory with a write lockout feature, (2) punched paper tape, and (3) solid-state ROM which we will discuss below. These storage devices are used for data that is *fixed* or not changed often.

All memories, whether ROM or not, must be programmed.

2-74. *Programming the solid-state ROM.* The solid-state ROM is constructed with all locations either in the ONE or ZERO state dependent upon the manufacture. Each bit location must then be set to the desired state by applying excessive current or voltage. With the punched paper tape, a hole punched in the wrong location means the tape is no longer useful and must be thrown away. The solid-state ROM is programmed bit by bit (location by location) much the same as the paper tape; that is, an error cannot be changed. Because of this feature, solid-state ROM programming is often referred to as *up-the-creek programming.* Since the program must be error free the first time it is written, a truth table is constructed prior to programming. There are some solid-state ROMs that can be erased and reprogrammed, but they are expensive and not widely used.

2-75. An example of a truth table constructed for a ROM that functions to activate the segment of a seven-segment light-emitting diode (LED) is shown in figure 4-15. Note that the output of each input address location consists of 1's and 0's. The 1's activate the corresponding segment of the seven-segment LED illustrated in figure 4-16. This example LED displays one of the digits 0 through 9, depending on what segments are activated by a selected address of the ROM. Once the segments are selected and activated for a particular digit, they glow a predetermined color that is a characteristic of the particular LED being used. Now, select an address in figure 4-15 and apply its output to the LED segment in figure 4-16; you should be able to visualize the digit (pattern) to be displayed by the LED. For example, if you select input address 0101$_{(2)}$ in figure 4-15, LED segments A, C, D, E, and G of figure 4-16 are selected for display. Now, if you draw out each segment selected, connecting each to one another, you'll see that the digit 5 would be displayed. Now, try another selection.

2-76. The most important point you should keep in mind about the ROM (just discussed) is that the preprogram must not have any errors. This fact revealed itself when we applied an output from figure 4-15 to the LED segment of figure 4-16. That is, if a 1 had shown up instead of a 0 in an output position of figure 4-15, the intended digit would not have been displayed correctly.

INPUT ADDRESS				OUTPUT								PATTERN
D	C	B	A	A	B	C	D	E	F	G	H	
0	0	0	0	1	1	1	1	1	1	0	0	0
0	0	0	1	0	1	1	0	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	0	2
0	0	1	1	1	1	1	1	0	0	1	0	3
0	1	0	0	0	1	1	0	0	1	1	0	4
0	1	0	1	1	0	1	1	0	1	1	0	5
0	1	1	0	1	0	1	1	1	1	1	0	6
0	1	1	1	1	1	1	0	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	0	8
1	0	0	1	1	1	1	1	0	1	1	0	9

NDA6-131

Figure 4-15. ROM programming truth table.

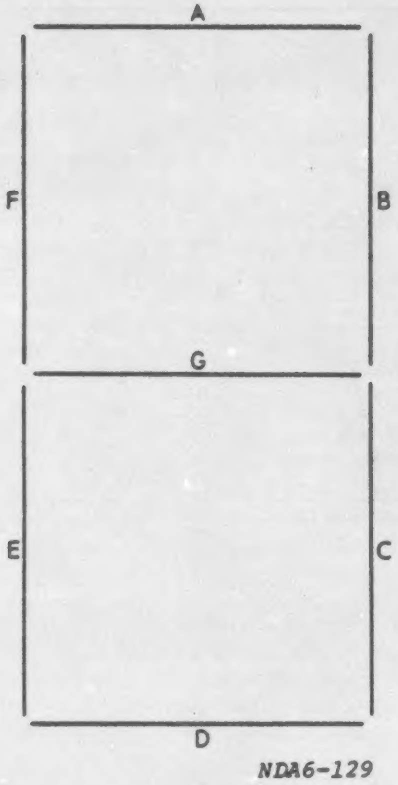


Figure 4-16. LED display (seven segment).

3. Arithmetic Unit

3-1. The arithmetic unit is the functional heart of the computer. It is that portion of the computer hardware in which all arithmetic and most logical operations are performed. This unit usually has the capabilities of performing the arithmetic operations of addition, subtraction, multiplication, and division. Most of these operations can be broken down into the simple arithmetic process of addition. Recall that subtraction can be carried out by adding the complement of the subtrahend to the minuend, multiplication by repeated addition and shifts, and division by repeated subtraction and shifts. The arithmetic unit must also be capable of recognizing both positive and negative numbers and modifying its operations accordingly. Another important requirement of this unit is to generate specific signals needed to perform specific operations (within the arithmetic unit) when arithmetic operational instructions are decoded.

3-2. A knowledge and an understanding of the counters and registers discussed in Chapter 3 and the logic gates discussed in Chapter 2 are a necessity to understanding the functioning of the arithmetic unit. Another very important circuit that is used within the arithmetic unit is the adder. There are two types of adders: half-adder and full-adder.

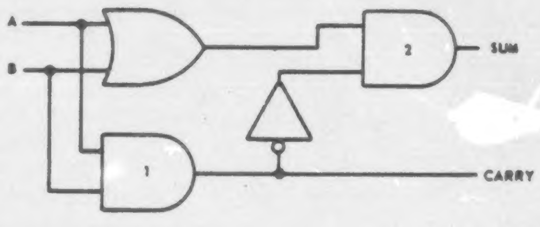
3-3. Adders. The circuit requirements for binary addition can be found by examining the rules for addition of any two bits. Recall that there are only four possible sum combinations of two bits:

0	1	0	1	Augend bit
+0	+0	+1	+1	Addend bit
0	1	1	0	Sum bit
(0)	(0)	(0)	(1)	Carry bit

From the above, you can see a need for an arrangement of logic circuits that adds combinations of any two bits and produces proper sum and carry outputs for each. The circuits that are needed must be based upon the individual requirements for the sum bit and the carry bit. If the augend bit is called A and the addend bit B, then the sum bit is 1 when:

(A OR B) AND NOT (A AND B) = 1 (Sum)
The carry bit is (1) when: (A AND B) = (1) (Carry)

3-4. *Half-adder.* It is possible to use one AND-circuit for (A AND B) and take the carry output directly from it. An inverter and a second AND-gate takes care of the AND NOT term, while an OR-gate handles the (A OR B) term. The composite logic diagram is shown in part A of figure 4-17. This arrangement for adding two binary bits and producing the proper sum and carry bits is



(A) LOGIC DIAGRAM

(B) BLOCK DIAGRAM

NDA6-137

Figure 4-17. Half-adder circuit.

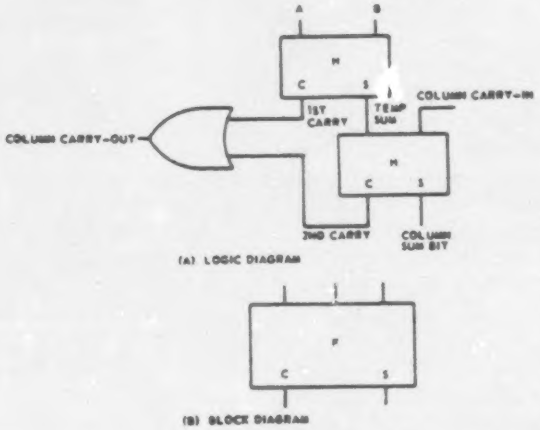
called a half-adder. A common block symbol for this circuit appears in part B of figure 4-17; it should be remembered that this symbol may represent any of several possible circuit arrangements as well as the one in part A of figure 4-17.

3-5. In operation, if only one input is 1, the output 1 from the OR-circuit is applied to one input of AND-gate 2. In this case, AND-gate 1 cannot produce an output with only one input present, so the carry is (0). This carry is inverted to 1 and applied to the other input of AND-gate 2, resulting in a sum bit of 1. If A and B are both 1's, AND-gate 1 produces a carry of 1 which is inverted to 0 and applied to the other input of AND-gate 2. With a 0 on one input, this AND-gate cannot provide an output even though a 1 comes from the OR-circuit, so the sum bit is 0. Finally, if A and B are 0's, both the sum and carry bits are 0's.

3-6. An arrangement of this type (called a half-adder) cannot add two binary numbers, although it can add two bits. The reason can be seen by performing a sample binary addition, showing the carries from one column to the next:

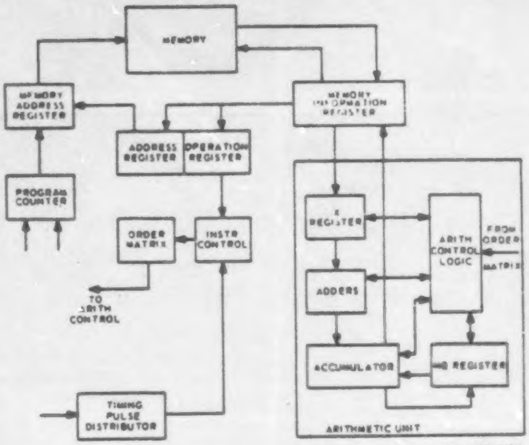
	(1)	(1)	(1)		Column carry
0	0	1	1	1	Augend
0	0	0	1	1	Addend
0	1	0	1	0	Sum

Although only two numbers are being added, some columns require that three bits be summed because of the carries from other columns. A single half-adder cannot do this, but a means for doing it has been devised: a full-adder.


A
B
H
C
S
1ST CARRY
TEMP SUM
COLUMN CARRY-IN
COLUMN CARRY-OUT
H
C
S
2ND CARRY
COLUMN SUM BIT
(A) LOGIC DIAGRAM
F
C
S
(B) BLOCK DIAGRAM

NDA6-144

Figure 4-18. Full-adder circuit.


MEMORY
MEMORY ADDRESS REGISTER
MEMORY INFORMATION REGISTER
ADDRESS REGISTER
OPERATION REGISTER
PROGRAM COUNTER
ORDER MATRIX
INSTR CONTROL
TO ARITH CONTROL
X REGISTER
ARITH CONTROL LOGIC
FROM ORDER MATRIX
ADDERS
ACCUMULATOR
MQ REGISTER
TIMING PULSE DISTRIBUTOR
ARITHMETIC UNIT

NDA6-126

Figure 4-19. Sample computer.

3-7. *Full-adder.* First of all, it was necessary to establish a fixed and definite pattern that would cover all possible addition problems. The example just given for the half-adder used five-bit words, but in an actual computer the words might be of any length and carries could occur in any column. Recall when the 1's complement system is used to represent negative numbers, the end carry (if it occurs) must be taken around and entered into the least significant column. To make the addition pattern regular, the practical thing to do is to consider that there will always be a carry into each column, but that the carry might be 1 or 0. Thus, the example becomes:

(0)	(1)	(1)	(1)	(0)	Column carry
0	0	1	1	1	Augend
0	0	0	1	1	Addend
0	1	0	1	0	Sum

3-8. The carry in the least significant column is always (0) at the beginning of an addition, although an end carry may have to be entered there later. There are now three bits to be added in every column. The first half-adder adds two of them, but a second half-adder is needed to add the third bit to the sum of the first two. Since there is a carry of (0) or (1) from each half-adder, some additional logic circuitry is needed to handle the carry out of the column. Probably the most common method of accomplishing this, as shown in part A of figure 4-18, is to add the augend and addend bits (A and B) in the first half-adder which produces a temporary sum bit and a first carry:

1	Augend bit
1	Addend bit
0	Sum bit
(1)	First carry (out)

3-9. In the second half-adder, the carry-in from a less significant column is added to the temporary sum bit, which produces the column sum bit and a second carry.

0	Temporary sum bit
(1)	Column carry (in)
1	Sum bit
(0)	Second carry (out)

If either the first or the second carry is 1, it must be the column carry-out. Since any carry resulting from addition in a given column must be sent to the next, some additional circuitry is needed. Notice, however, that both carries cannot be 1's; if the first is a 1, as in the preceding example, the second can only be (0). Thus, all that is necessary to produce the column carry-out is to feed both first and second carries to an OR-circuit, as shown in part A of figure 4-18.

3-10. The arrangement shown in this figure is a full-adder, so-called because it can properly handle all of the addition that might occur in a column, including the carries between columns. Part A of figure 4-18 represents only one of a number of possible circuit arrangements. The usual block symbol is shown in part B of figure 4-18.

3-11. **Sample Computer.** The simplified block diagram illustrated in figure 4-19 shows the arithmetic unit in relationship to the memory unit and a portion of the control circuitry. Recall that the memory stores both the program (instruction words) and the operands (data words). Each of these computer words is of vital importance to the operation of the arithmetic unit. The instruction word supplies the command (ADD, SUB, etc.) to the *instruction control* logic which, in turn, sequences the arithmetic unit through an arithmetical operation. The data word, as its name implies, supplies the data to be manipulated during the operation.

3-12. The *instruction control* circuits are considered a part of the control unit and contain the command decoders and the order matrix. Command decoders simply detect the contents of the *operations register* to identify what operation is to be performed. The *order matrix* logic circuits control the operation of the computer once the command has been detected. At the conclusion of an arithmetic operation, the results are in the accumulator. To write this data into memory necessitates the generation of the STORE command and its appropriate control signals. Also, to cause the computer to stop functioning requires the generation of a HALT and its associated control signals.

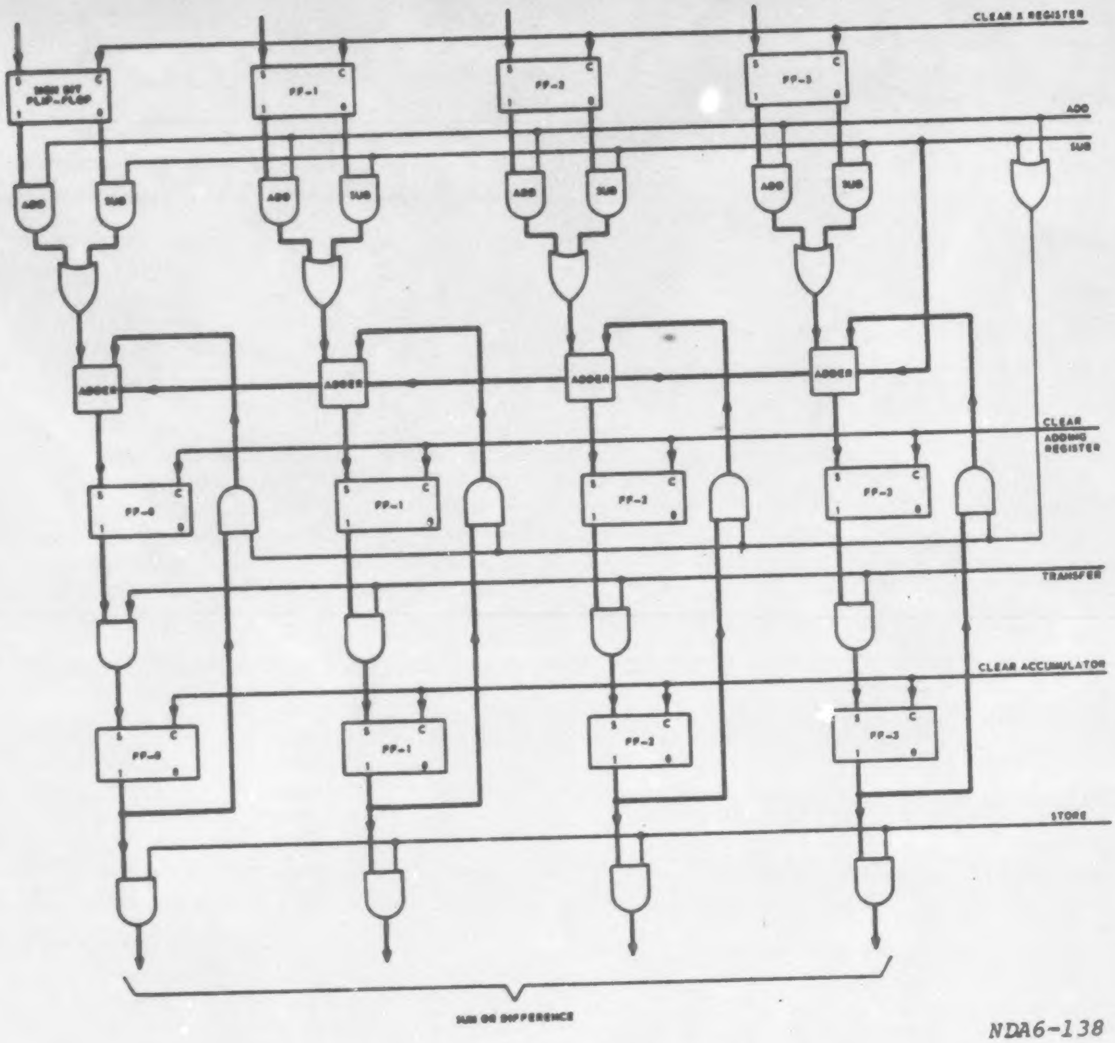
3-13. That portion of the block diagram in figure 4-19 in the enclosed area shows the general organization of a typical arithmetic unit. It consists primarily of three registers, an adder circuit, and control logic. For convenience, the various registers of the arithmetic unit are generally given designations such as "A-register," "B-register," "X-register," and "MQ-register."

3-14. *Accumulator.* The basic register of the arithmetic unit is generally referred to as the accumulator register. As its name suggests, an accumulator keeps a running total of the arithmetic operations. The accumulator also provides storage for one of the operands (numbers to be operated on) during the arithmetic operation. The operands handled by the accumulator are the augend, minuend, multiplier, and dividend. The multiplier and dividend are found in this register at the start of the multiplication and division operations, and as these operations proceed, this register provides temporary storage of the partial products and quotients as they are developed. Results of an arithmetic operation may be stored into memory from this register through the memory information register (MIR).

3-15. *MQ-register.* This register acts as an extension of the accumulator, and it is used during the multiply and divide operations. During these operations, the final product or quotient is developed here. In order to perform these operations, this register must be capable of arithmetic shifts in conjunction with the accumulator.

3-16. *X-register.* Like the accumulator, this register is used to temporarily store one of the operands during an arithmetic operation. This operand may be the addend, subtrahend, divisor, or multiplicand, depending on the operation to be performed. It should be noted that this is the only arithmetic register capable of receiving data from memory that is going into the arithmetic unit.

3-17. *Adders.* To be functional, the adders must be capable of handling both positive and negative numbers during add and subtract operations. Often, the adder circuits are used as comparators to compare the equality or inequality of the operands stored in the X-register and the accumulator. This logical operation is made possible by simply inhibiting the carry input to each full-adder stage and monitoring the sum outputs. In effect, with the carry input inhibited, the


CLEAR X REGISTER
SIGN BIT FLIP-FLOP
FF-1
FF-2
FF-3
S
C
1
0
ADD
SUB
ADD
SUB
ADDER
CLEAR ADDING REGISTER
FF-0
TRANSFER
CLEAR ACCUMULATOR
STORE
SUM OR DIFFERENCE

NDA6-138

Figure 4-20. Simplified arithmetic circuit.

full-adder functions as a half-adder with the sum output being the equivalent of the exclusive OR (comparator) circuits; that is, $\overline{A}B$ or $A\overline{B} = C$.

3-18. *Arithmetic control logic.* Within this portion of the arithmetic unit are found:

- Circuits to translate and carry out the subcommands received from the order matrix.
- Arithmetic pause timing circuits which control the operation of the arithmetic unit during the multiplication and division operations.
- Sign bit control circuits which control, to some extent, the overflow circuits and determine the sign of the results of an arithmetic operation.

3-19. **Arithmetic Unit Operational Instructions.** Instructions are required to command and direct the operation of the arithmetic unit. They are part of the program which is usually stored in memory. A few of the most important instructions and the actions that take place within the arithmetic unit, when they are received in the instruction control circuits, are as follows.

3-20. *GET.* The GET (or FETCH) instruction first applies a clear pulse to the accumulator register, then adds to it the contents of the specified memory location. It should be easy to see why this instruction is usually the initial instruction in most arithmetic programs.

3-21. *Addition.* The ADD instruction adds the contents of the specified location to the contents of the accumulator register. The resultant sum is found in the accumulator at the end of the operation. It should be noted that when a computer has the capabilities of handling both positive and negative numbers, as is usually the case, this sum will be the "algebraic sum" as follows:

Addend	+3	-3	-3	+3
Augend	+2	-2	+2	-2
Sum	+5	-5	-1	+1

3-22. *Subtraction.* The SUB instruction subtracts the contents of the specified memory location from the contents of the accumulator. This instruction differs from the ADD instruction only insofar as the contents of the specified memory location (subtrahend) are complemented before being added to the accumulator. Again, due to the signed quantities, the resultant difference is the "algebraic difference." An example is as follows:

Minuend	+3	+3	-3	-3
Subtrahend	-2	+2	-2	+3
Difference	+5	+1	-1	-6

3-23. *Multiplication.* The MULT instruction multiplies the contents of the specified memory location by the contents of the accumulator. When multiplying signed quantities, the arithmetic unit must determine the sign of each of the operands and assign the proper sign to the product. The rules for the multiplication of signed quantities are that like signs produce a positive product while unlike signs produce a negative product.

3-24. *Division.* The DIV instruction divides the contents of the accumulator (dividend) by the contents of the specified memory location (divisor). When dividing signal quantities, the rules are the same as for multiplication; that is, a negative quantity divided into a negative quantity results in a positive quotient.

3-25. **Analysis of Arithmetic Functions.** Now that we have discussed the makeup of a typical arithmetic unit, the functions it performs, and some of the arithmetic instructions required to perform its function, let us analyze two of these functions: addition and subtraction. To make it easy to understand these functions, a comparison is made between the computer functions and pencil-and-paper functions for each operation.

3-26. *Addition.* This function is discussed first since it is the basic operation of the arithmetic unit. Figure 4-20 is a simplified version of the arithmetic unit's X-register, adders, and accumulator. This figure shows only those gates and registers necessary for explanation of these two basic functions. Your reference to this figure should make it easier to follow the explanations.

3-27. In working any problem on paper, we usually start with a clean sheet. The same effect is achieved in a machine by clearing the registers. Looking at figure 4-20, we see that a clear pulse is sent to each register of the arithmetic unit and resets all registers to the ZERO state. We now have our "clean paper" in the machine and are now ready to start bringing in the data words that are to be worked on. In our example, we add the numbers $0\,1\,1\,1_{(2)}$ (augend) to $0\,1\,0\,1_{(2)}$ (addend). These small numbers do not exceed the bit capacity of the accumulator; therefore, the MQ-register is not required. This keeps the operation simple and makes the explanation easier to follow. As each step of the operation is discussed, the resultant status of the registers in the arithmetic unit is indicated.

STEP 1. Apply CLEAR pulse to all registers.

0 0 0 0	X-register
0 0 0 0	adding register
0 0 0 0	accumulator

STEP 2. Enter the augend into the X-register. The information that we are now putting into the X-register is coming from memory in parallel form. Looking again at figure 4-20, you can see that the information input is to the SET (ONE) side of the X-register flip-flops (F/Fs). In this case, a F/F is set only when its corresponding place position within the number contains a ONE. Thus, we now have:

0 1 1 1	X-register
0 0 0 0	adding register
0 0 0 0	accumulator

3-28. Now, because the X-register is our receiving register by which all numbers enter the arithmetic unit, it is necessary to move the augend to the accumulator so that we can transfer in the addend. Looking at figure 4-20, you can see that the only way to transfer from the X-register to the accumulator is to combine (using the add pulse) the contents of the X-register and the adding register, and then transfer (using the transfer pulse) the resultant from the adding register to the accumulator. When this is done, we have:

0 1 1 1	X-register
0 1 1 1	adding register
0 1 1 1	accumulator

Since the machine does not destroy the information in a register when it transfers from one register to another, it is necessary to clear (using the clear pulse) the X- and adding registers before bringing in the second part of our problem. When this is done, we have:

0 0 0 0	X-register
0 0 0 0	adding register
0 1 1 1	accumulator

STEP 3. Enter the addend into the X-register.

0 1 0 1	X-register
0 0 0 0	adding register
0 1 1 1	accumulator

STEP 4. Add the contents of the X-register and accumulator. A pulse representing the command to ADD comes from the control unit and enters the circuit shown in figure 4-20 on a line labeled ADD. Tracing this line to the left, we see that it is connected to AND-gates. We also see that the other input to each of these gates is from the ONE-side output of a F/F in the X-register. Therefore, when the ADD pulse is present, there is a conditioning output from each AND-gate that has a ONE on its other input line from the X-register. The output from these AND-gates is coupled through an OR-gate to the adder circuits. Looking at these adder circuits, we find that their other input comes from the ONE-side output of the accumulator F/Fs through additional AND-gates that are also conditioned by the ADD pulse. Therefore, when the ADD pulse is present, there is an output from each AND-gate having a ONE on its input line from the accumulator. This is how the contents of the accumulator and X-register are transferred simultaneously to the ADDERS in order to accomplish the adding function. The adders, in turn, are connected directly to the ONE-side outputs of the adding register which now holds the SUM. The adding register holds the sum until it is commanded to transfer it to the accumulator. We now have the following configuration in the arithmetic unit:

0 1 0 1	X-register
1 1 0 0	adding register
0 1 1 1	accumulator

STEP 5. Clear the accumulator and transfer the contents of the adding register to the accumulator. The command lines for the transfer-and-clear of the accumulator are shown in figure 4-20. This completes the actual arithmetic operation. The final action is to transfer the contents of the accumulator to storage, where it remains for later use. The computer now halts or proceeds with the next problem, dependent on the next instruction.

3-29. *Subtraction.* Remember that earlier we made the statement that an arithmetic unit performs all operations by addition. We will now see how the machine does subtraction through the use of addition. This explanation is brief, since a detailed analysis of the machine action was given during the explanation of addition. The discussion is based upon the circuit shown in figure 4-20.

STEP 1. Apply CLEAR pulse to all registers.

0 0 0 0	X-register
0 0 0 0	adding register
0 0 0 0	accumulator

STEP 2. Enter the minuend 0 1 1 1 into the X-register.

0 1 1 1	X-register
0 0 0 0	adding register
0 0 0 0	accumulator

STEP 3. Now, as we did in addition, combine the contents of the X-register and accumulator in the adding register.

0 1 1 1	X-register
0 1 1 1	adding register
0 0 0 0	accumulator

STEP 4. Our next operation is to transfer the contents of the adding register to the accumulator and then clear the X-register and adding register.

0 0 0 0	X-register
0 0 0 0	adding register
0 1 1	accumulator

STEP 5. Enter the subtrahend 0 1 0 1 into the X-register.

0 1 0 1	X-register
0 0 0 0	adding register
0 1 1 1	accumulator

STEP 6. Subtract the contents of the X-register from that of the accumulator. This is accomplished by taking the ONE's complement of the subtrahend. When the ONE's complement of a number is required, as in operations involving subtraction and division, it is taken from the ZERO side of the register F/Fs. Also, in order to simplify machine operations, the ONE's complement is changed to the TWO's complement. This is done by adding 1 to the ONE's complement of the number. Keep these things in mind as we proceed with the explanation. To illustrate the procedure, a pencil-and-paper presentation of the problem is first given.

0 1 0 1	subtrahend
1 0 1 0	ONE's complement of the subtrahend
1	add one
1 0 1 1	TWO's complement of subtrahend
0 1 1 1	minuend
1 0 0 1 0	difference (obtained by addition)

NOTE: When the TWO's complement of the subtrahend is added to the minuend, there is a carry generated in the most significant position. This carry is indicated as 1. There is no register stage to store this carry, and it is therefore lost. This carry from the most significant position is disregarded; therefore, it is not considered as part of the answer. Is this correct? To be sure, write the binary numbers with their decimal equivalents next to them and subtract.

Example:

0 1 1 1 = 7 minuend
0 1 0 1 = 5 subtrahend
0 0 1 0 = 2 difference

3-30. Now let us proceed with the machine operation by pulsing the SUB line shown in figure 4-20. The result of this is to add the complement of the number (subtrahend) in the X-register and the number (minuend) in the accumulator. Notice that the SUB pulse is fed to the first adder stage. Addition of this SUB pulse gives the TWO's complement. The register configuration is now:

1 0 1 0	X-register (complemented subtrahend)
1	subtract pulse to adder
0 1 1 1	accumulator
0 0 1 0	resultant in the adding register

STEP 7. The remaining steps are shifting and clearing steps. They are as follows:

a. Clear the accumulator and X-register.
b. Shift the content of the adding register to the accumulator.
c. Clear the adding register.
d. The contents of the accumulator may be sent to memory for storage, or retained in the accumulator to be used in the next operation.

3-31. With the exchanging of information between the input, output, memory, and arithmetic units, there must be some means of control. This is where the control unit fits into the computer operation, and it is the next subject to be discussed.

4. Control Unit

4-1. In all the arithmetic arrangements, the need is clear for control pulses and signals. These must be fed to the proper places at the proper times in order to open or close gates, start or stop operations, transfer numbers from one place to another, and control other functions of the computer.

4-2. The circuitry that generates, times, and distributes the control signals, usually called commands, may be as complex as the actual arithmetic circuitry—especially in a large-scale computer. The generating, timing, and major distributing circuits, taken together, make up the control unit. This unit must provide commands not only to the arithmetic portion of the computer but also to the main storage, input, and output portions as well.

4-3. For a complete understanding of the role played by the control unit, it is necessary to recall some of what you have learned about the manner in which the program governs the operation of the entire computer. The program, of course, is a set of instructions, coded in the form of numbers (words) that are stored within the computer's memory.

4-4. Regardless of where the program is stored, each instruction word is taken in a separate step—in the proper sequence—by the control unit and decoded to see what major operation must be performed next. The control circuitry then develops the complete set of commands or control signals that enables all the parts of that operation to be carried out by the other units of the machine.

4-5. An instruction, for example, gives the order add; it also gives the storage address of the number to be added to the contents of the accumulator. The control unit must then put out a series of commands which may be single pulses, signal levels, a series of pulses, or any combination of these. There are as many possible variations in a set of commands to perform the addition operation as there are variations in adder-accumulator circuitry.

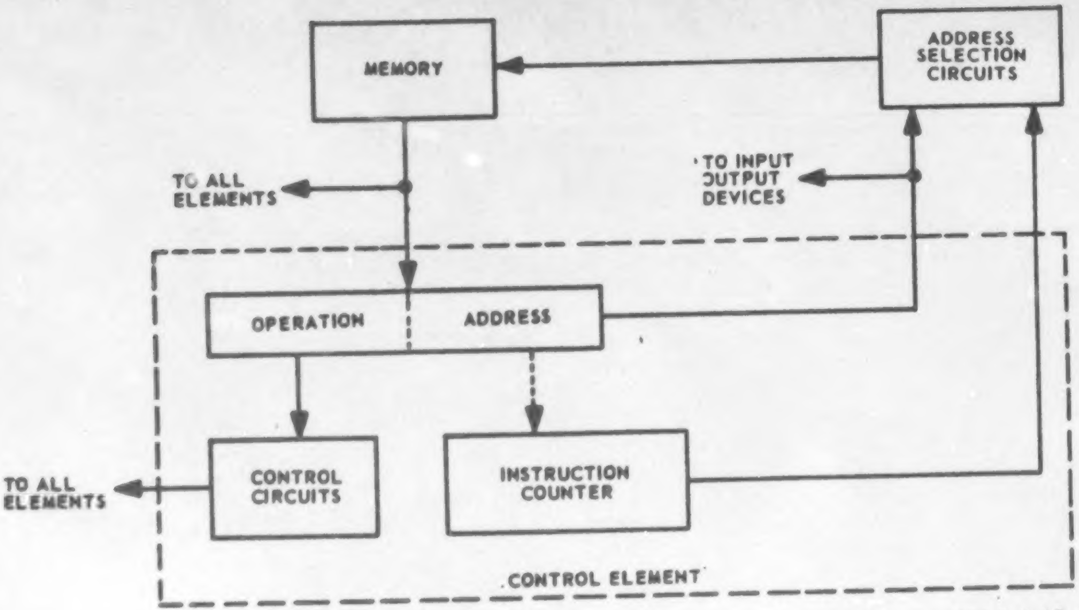


Figure 4-21. Instruction control.

4-6. The operation portion of an instruction may, of course, call for any number of jobs to be done in the computer instead of an arithmetic operation. The variety of operations depends upon the capabilities of the computer. Examples of these jobs found in nearly every computer are the transferring of numbers from place to place and the control of input-output devices.

4-7. Program Control. After one instruction (program step) has been carried out, the control unit must obtain the next one from storage. But how does it know the location of the next instruction? There are several possible solutions to this problem. One of the easiest is to set aside a block of memory addresses in which the program is always kept, and use an *instruction* or *program counter*—usually a binary counter—to keep track of the progress of the program and the instruction address. An arrangement for doing this in the stored program computer appears in figure 4-21.

4-8. In this arrangement, the memory or main storage unit must be capable of storing many numbers, including the input information (data words) with which the computer is to work, the partial results to be held for later use, the final results, and the program itself. Each memory location is identified by an address. Therefore, there must be selection circuitry to translate the address part of the instruction and arrange circuitry to form an actual electrical connection to the correct memory location so that information can be put in or taken out.

4-9. Ordinarily, a block of the lowest numbered memory address is set aside for the program. Assuming that addresses 00 through 99 were reserved for this purpose, any program would be stored with its first instruction in address 00, its second in address 01, its third in address 02, etc. Thus, a 67-step program would be stored in sequence in address 00 through 66.

4-10. The instruction counter shown in figure 4-21 is cleared before the program begins. Its indication of 000. . .000 is sent to the address selection circuits, causing them to make a connection to memory address 00. The first instruction is taken out of memory and sent to the control circuits through switching circuits operated by commands issued for this purpose. The time spent in the process of obtaining the instruction is called *program cycle time* or *instruction cycle*.

4-11. Once in the control unit, the instruction is placed in a temporary storage register called either the *instruction register* or the *operation-address register*. The control circuits issue commands to carry out the operation called for by this first instruction during what is called the *execution* or *operation cycle*. The address part of the instruction goes to the address selection circuits causing memory to be addressed, thus obtaining the number representing the data to be operated upon. The address may, in another instance, call for a connection to one of the input or output devices to obtain or send out information.

4-12. Toward the end of the operation being performed, a pulse is sent from the control circuits to advance the instruction counter by 1. When the operation cycle ends, control is turned over again to the instruction counter and a new instruction cycle begins. The counter now sends 000. . .001 to the address-selection circuits. This second instruction of the program is taken from memory address 1 and sent to the operation address register to be executed.

4-13. The process of bringing each instruction in sequence from the memory, executing it, and stepping the instruction counter by 1, continues in this manner until the entire program has been performed or until a *branch* instruction, sometimes called *transfer* or *jump*, makes it possible to change a program or repeat parts of it, either unconditionally or under control of the results that have been computed. For example, the programmer may choose to order a branch only if the number left in the accumulator is negative. If sensing (checking its state) shows it to be positive, the branch is not accomplished.

4-14. When a branch is to be made, the address part of the instruction is taken from the instruction register and loaded directly into the instruction counter, replacing whatever number was previously there. Therefore, the next instruction taken from memory is not from the next address in the sequence that was being followed but is from the address given by the *branch* instruction. From this point on, the instruction counter is again pulsed once for each instruction carried out, so a fresh numerical sequence of instructions is followed until another branch can be made to either a higher or lower numbered step of the program.

4-15. In other types of computer, those not storing the program instruction in the memory elements, different methods of instruction control may be used. These depend to a great extent, of course, upon the nature of the device or arrangement used to hold the program. Usually, the instructions are made available in sequence, and, when each operation is completed, the control element senses the next instruction. This procedure is somewhat similar to that used by a stored-program computer.

4-16. Operation Control. The commands necessary to carry out an instruction have been described as a set of pulses (sometimes other types of signals) sent to the proper places at the proper times. Different sets (pulses) are needed, of course, to carry out different operations, although certain individual commands may well be used in a number of operations.

4-17. There are two basic approaches to the problem of handling operations in sequence. First, it is possible to use a timing arrangement (oscillator) and rigidly control each separate operation, issuing each command at the proper time. The timing arrangement is called the *clock*, and it is a *synchronous* control method because all operations performed in the computer are synchronized by the clock. The device which produces the clock pulse is an accurate oscillator, generally crystal-controlled, followed by amplifying and pulse-shaping circuits.

4-18. In the second method of control, called *asynchronous*, no clock is used for timing operations, although there may be a clock for other purposes. As soon as one operation is finished, a signal is provided to start the next. The timing of commands is done by starting a pulse through a long delay line (when each operation begins) and tapping off commands at the proper time intervals.

4-19. Some computers use the synchronous system, others the asynchronous system, and quite a number use combinations of the two—with synchronous control for short operations and asynchronous control to simplify handling of the longer ones. Although it is true that operations are performed faster under asynchronous control because no fixed time intervals (cycles of the clock device) are used, the circuitry is generally more complex than the synchronous control.

4-20. *Synchronous control.* The first item of interest in this system is the clock and the method of timing. There are certain time limitations in any computer, one of which is the period required to transmit a single bit of information and allow the circuits to recover from transients. This period sets the minimum limit of one bit time.

4-21. In a serial-mode computer, the bits of a word follow each other on a single wire, and exact timing is so essential (at the inputs to an AND-circuit, for example) that a clock must be used to set the basic pulse repetition frequency or bit-time interval. If pulse-type signals are used, clock pulses at bit-time intervals must be distributed throughout the

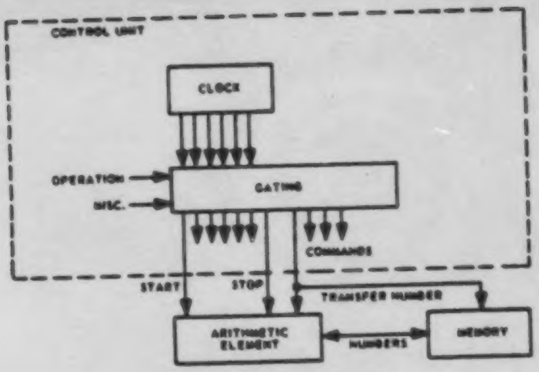


Figure 4-22. Synchronous control of operations.

circuitry to provide the frequent reshaping and retiming of information pulses. This holds true even if the control element itself is asynchronous in operation and does not depend on the clock.

4-22. In parallel-mode operations, the bit-time interval is usually less vital to successful operation, so the clock pulses need not occur every bit time. Instead, they may be produced at some longer or shorter interval, which is more useful in synchronizing the operations of the computer. However, since the bit time is the basic measure of the speed with which numbers can follow one another in the circuitry, it is not often that a different interval is selected.

4-23. Whatever the basic interval selected, the clock-pulse intervals bear some relationship to *real time* (time in the "real world"). Many types of problems solved by computers involve keeping track of real time. Military weapons control computers, for instance, must solve time-speed-distance problems in order to cope with an incoming enemy, while computers operating various types of input-output devices must time their operations. It is frequently valuable to select a clock-pulse interval that can be easily converted to real time. A fairly common rate is 1 megacycle, which means pulses are at 1-microsecond intervals. Using decimal counters or other circuits for frequency division, it is possible to obtain pulses at 1-second intervals for useful time measurements within the computer.

4-24. It becomes apparent that the continuous stream of clock pulses cannot be used in this form. Some method must be used to keep track of the pulses. This is usually done by a counter. For example, how many clock intervals are required to perform addition or division? How many for an instruction cycle, or for transferring a number? It is obviously impractical to run a continuous count of the clock pulses, because in 10 seconds of operation the count would be between 5 and 20 million for most computers. A cycling count, on the other hand, proves to be very practical. By counting a given number of clock pulses and then beginning the count over again, the passage of time in the computer is divided into intervals of useful length that can be called *clock cycles* or *machine cycles.* A simple ring counter can do this and provide a different active output for each step of the count.

4-25. A factor that must be considered in all machines, parallel or serial, is the time required (access time) to transfer numbers into or out of memory. This puts a limitation on the speed of operation, because each number to be used in computation and each result must go through this transfer. The access time in some computers is somewhat longer than the time needed for the shorter operations, such as addition. By making the length of the clock interval equal to the access time, the all-important transfer or numbers and the shorter operations can be performed in one clock interval. When one of the longer operations such as multiplication or division must be done, the required number of complete clock intervals is allowed.

4-26. Using an arrangement of this sort, illustrated in figure 4-22, two complete clock cycles are the minimum required to carry out any instruction. The first must be a program or instruction cycle to get the instruction out of memory and load it into the operation address register. The active (true) signals from the various stages of the clock-ring counter are gated or otherwise switched to provide commands controlling the address selection and other circuits to obtain the instruction from memory. When this instruction cycle is nearly done, a command sets a flip-flop or switch to start the operation cycle. Now, the circuit gating the clock-ring counter outputs comes under control of the signal representing the operation called for, and the result is a set of commands necessary to perform that operation. The commands must be timed to provide the maximum time for each part of an operation plus a safety factor. In binary addition, for example, time must be allotted for the propagation of a possible carry from each place, even though no carries occur in some problems. If more than one clock interval is required, a simple counter keeps

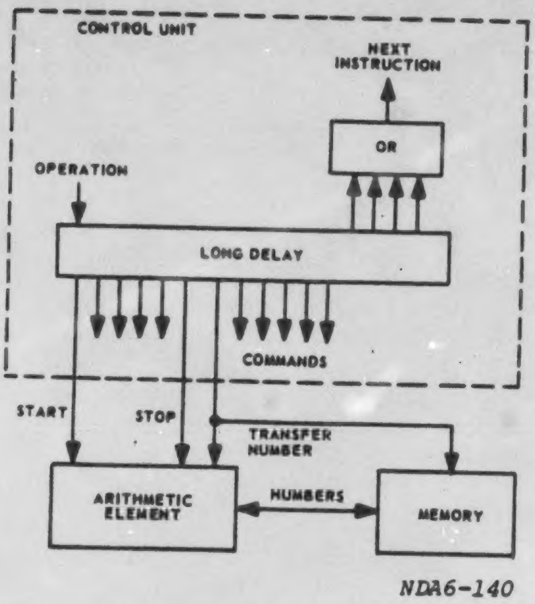


Figure 4-23. Asynchronous control of operations.

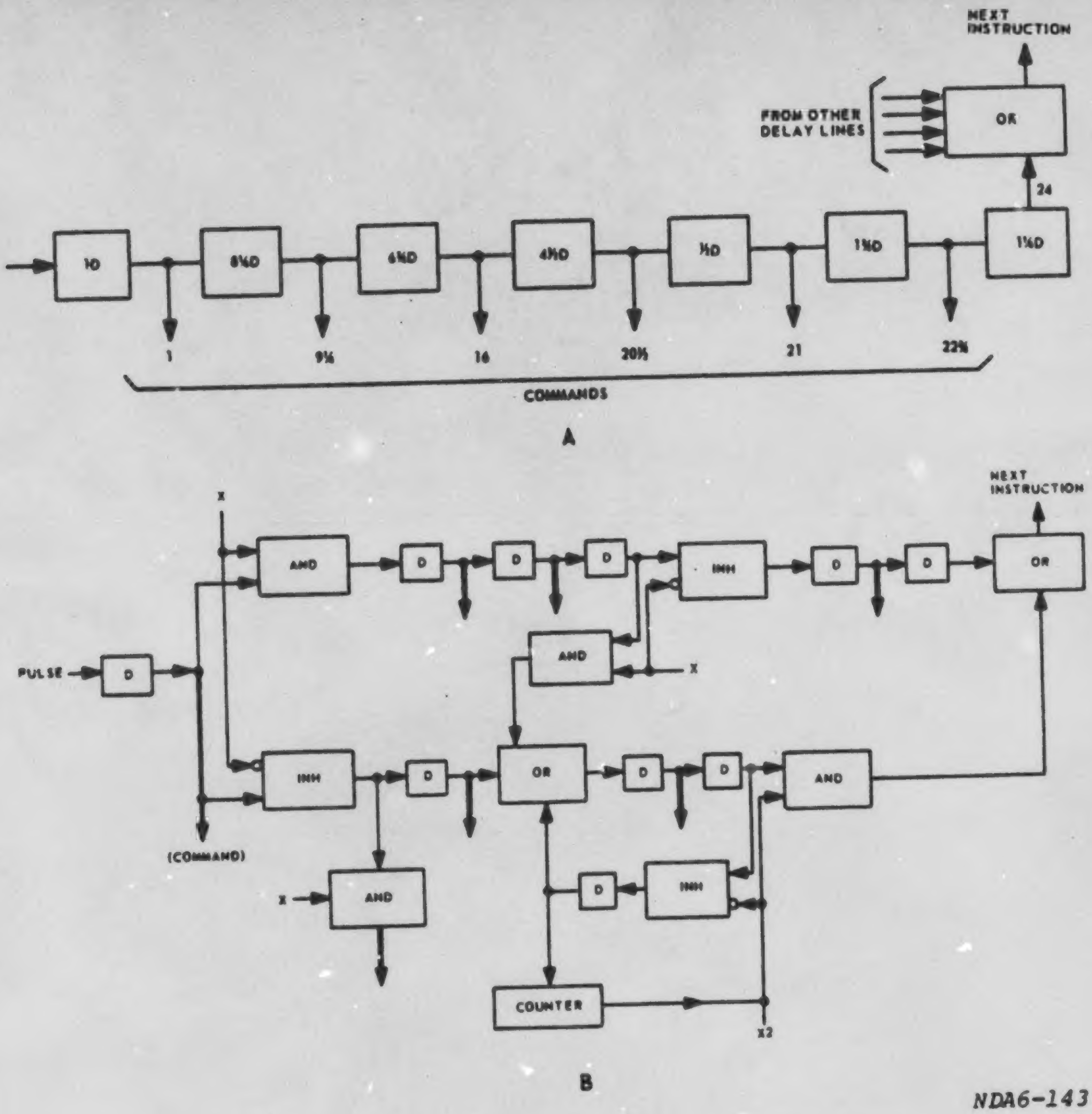
track of them and stops the execution of the instruction when the proper number of intervals has occurred.

4-27. When the operation is almost completed, the switching is reset for another instruction from memory. In this arrangement, all program or instruction cycles are identical, but the operation cycles depend upon the operation to be performed. All commands are provided by the timed pulses from the clock-ring counter. They are switched through the gating circuitry under control of either the operation signal or various miscellaneous signals, such as the one that determines whether an instruction or operation cycle is required. The operation signal is translated (usually in a matrix) from the operation portion of the instruction which is contained in the operation address register (see fig. 4-20).

4-28. *Asynchronous control.* There are a number of possible variations of the asynchronous control method. The basic approach appears in figure 4-23. It shows how the timing of commands is accomplished through the use of a long delay line instead of a clock. This delay line consists of a number of delay paths and switching circuits where necessary. Commands are tapped off between circuits at the required intervals. An operation which requires 24 bit times for its operation cycle, for example, can be handled by a string of delays totaling 24 bit times. Commands may be taken off at the end of 1, 9¼, 16, 20½, 21, 22¾, and 24 bit times, as shown at A of figure 4-24.

4-29. A pulse is inserted in the delay line where the operation signal appears. One bit time later, it emerges from the first delay circuit, goes on the first command line, and also enters the next delay section. Perhaps this first command might clear a storage register and start the address selection circuitry through the process of taking a number out of memory. The pulse emerges from the second section 8¼ bit times after the first operation was started and is sent out on another command line to perform some other control function. In this fashion, the pulse travels through the entire length of the delay line and is tapped off at intervals to form the commands. From the end of the line, the pulse goes to an OR-gate from which it emerges as a command calling for the next instruction.

4-30. Although it might seem necessary to have one delay line for the process of obtaining instructions and one for each different operation, this would require an unnecessary amount of circuitry. Actually, many operations are quite similar and the parts of longer ones are often repeated; it is possible to use one long delay line with switching circuits, alternate paths, and feedback loops to produce commands for all operations. One small portion of such a line is shown in part B of figure 4-24. The heavy, downward pointing arrows are commands, and the operations called for control the leads labeled X. Some, but not all, of the X-leads are energized when a given operation is to be performed. The operation of the circuitry is straightforward and should be clear enough, except possibly for the feedback loop involving the counter. If a pulse enters this loop through the OR-gate and finds that operation signal X2 is present, the feedback loop through INH is inoperative while the AND-gate is activated, letting the signal through without additional delay. If X2 is not present, however, the pulse does not get through the AND-gate but does enter the feedback loop through the INH circuit. The pulse is delayed each time it circulates through the loop. Each time the pulse returns to the OR-gate, it also steps the counter. When a predetermined count is reached, meaning the pulse has circulated and been delayed this many times, the counter output opens the loop by generating a signal similar to X2 and enables the pulse to exit through the AND-gate.


NEXT INSTRUCTION
FROM OTHER DELAY LINES
OR
24
1D
8½D
6½D
4½D
½D
1½D
1½D
1
9½
16
20½
21
22½
COMMANDS
A
NEXT INSTRUCTION
X
AND
D
D
D
INH
D
D
OR
AND
X
PULSE
D
INH
D
OR
D
D
AND
(COMMAND)
X
AND
D
INH
COUNTER
X2
B

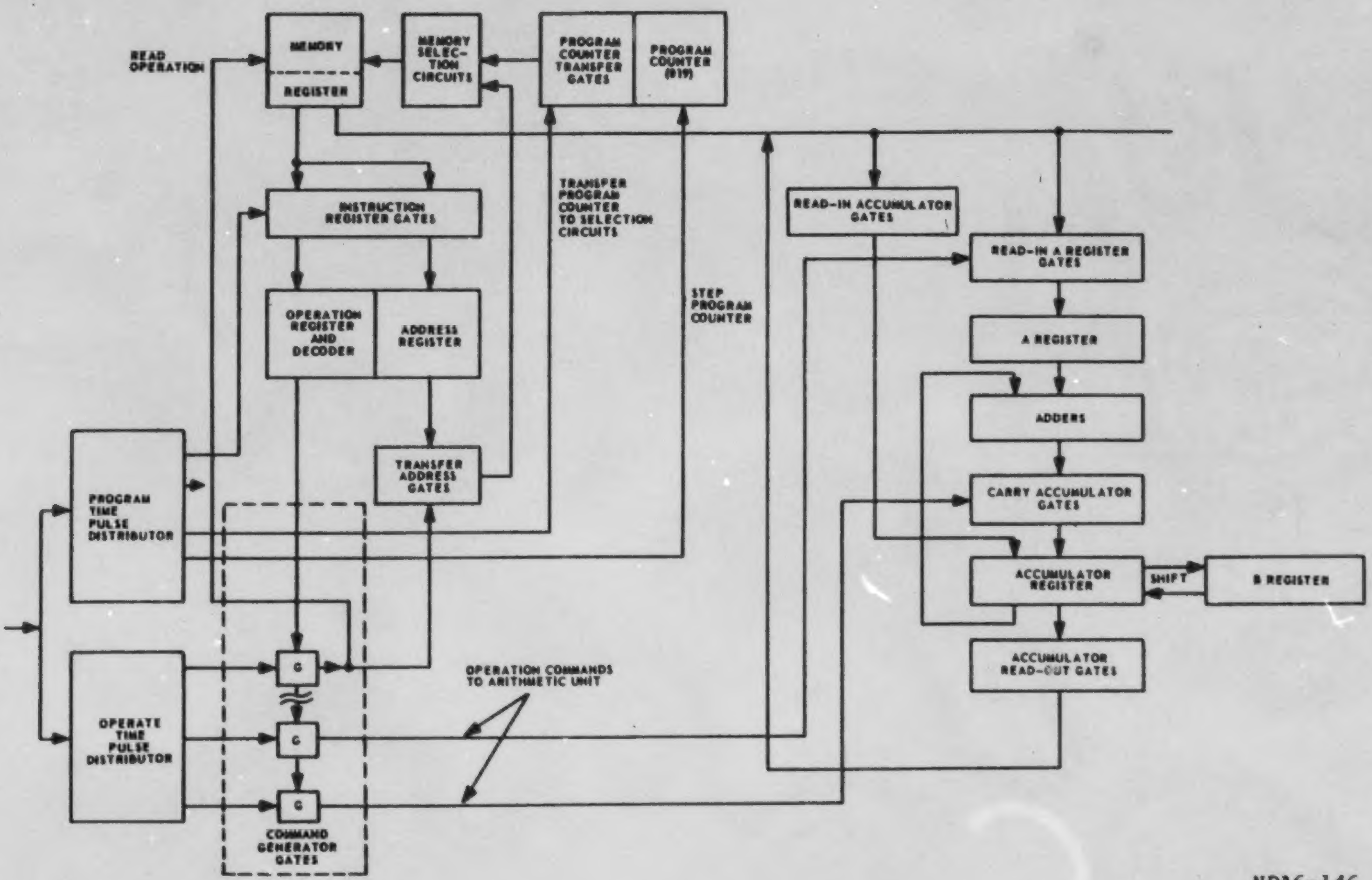
NDA6-143

Figure 4-24. Delay lines for asynchronous control.

4-31. Thus, one long delay line with many possible paths and loops enables the commands for any operation to be produced. A common path at the beginning of the delay produces the commands necessary for procuring each instruction. The timing for each operation is exactly what is requires, not a number of fixed length cycles with the possibility of wasted time if the actual operation ends before the end of the last cycle. This idea of asynchronous control can be extended in some types of circuitry by letting the control pulse run through the circuits themselves as the operation is being performed. An asynchronous adder, for example, can be built to allow the control pulse to run with the carries. As soon as carry propagation is completed, the control pulse is returned to the control element as a *next instruction* command.

4-32. Multiplication can be handled in similar fashion. In this type of arrangement, the control element tells the arithmetic element "start" and then waits for a signal to come back, saying "finished."

4-33. Arithmetic Control Operation. To illustrate the action of a typical arithmetic


READ OPERATION
MEMORY
REGISTER
MEMORY SELEC-TION CIRCUITS
PROGRAM COUNTER TRANSFER GATES
PROGRAM COUNTER (819)
INSTRUCTION REGISTER GATES
TRANSFER PROGRAM COUNTER TO SELECTION CIRCUITS
READ-IN ACCUMULATOR GATES
READ-IN A REGISTER GATES
OPERATION REGISTER AND DECODER
ADDRESS REGISTER
STEP PROGRAM COUNTER
A REGISTER
ADDERS
TRANSFER ADDRESS GATES
PROGRAM TIME PULSE DISTRIBUTOR
CARRY ACCUMULATOR GATES
ACCUMULATOR REGISTER
SHIFT
B REGISTER
G
G
G
OPERATION COMMANDS TO ARITHMETIC UNIT
ACCUMULATOR READ-OUT GATES
OPERATE TIME PULSE DISTRIBUTOR
COMMAND GENERATOR GATES

NDA6-146

Figure 4-25. Arithmetic control circuit.

control circuit, we will follow the execution of an instruction in the circuit shown in figure 4-25. Assume that the instruction ADD 36 occurs in a program. This instruction means that the number in memory location 36 should be added to the number which is already in the accumulator. Assume also that this instruction is Step 20 of the program. The following summarizes what happens as the instruction is executed:

a. At the completion of the previous instruction, the computer automatically goes into program time. Therefore, the program time pulse distributor is active.

b. Since 19 instructions have been executed, the contents of the program counter is 019, which is the address of the 20th instruction. The program counter transfer gates are conditioned by the program count to the memory selection circuits. Here, the program count is decoded to activate memory addressing circuits, resulting in a transfer of the memory location contents to the memory register.

c. The instruction word which is now in the memory register conditions the instruction register gates. A pulse from the program time pulse distributor activates the instruction register gates, transferring the instruction word to the operation and address registers. Here, the instruction is decoded. The operation part conditions the command generator gates, and the address part conditions the transfer address gates.

d. The program counter is stepped by 1 so that it contains the address of the next instruction to be executed.

e. The computer goes into operate time so that the operate time pulse distributor is now active. The transfer address gates are activated, transferring the address part of the instruction to the memory selection circuits, where it is decoded, and this results in addressing of the memory. The same signal which activated the transfer address gates also pulses the memory to cause a read operation and transfers the selected operand to the memory register. The operand which is now in memory register conditions the read in the A-register gates.

f. Command lines are now pulsed to cause the arithmetic unit to add. This is accomplished as follows: The read in the A-register gates is activated to cause a transfer of the operand from the memory register to the A-register. Thus, the contents of the A-register and the accumulator are applied as inputs to the adders where they combine to generate a sum which conditions the carry accumulator gates. These gates are now activated to cause the sum to be transferred from the adders to the accumulator register.

4-34. Any instruction which exercises the arithmetic unit follows the same basic pattern described in the ADD instruction. The program counter is stepped and the instruction selected from memory. The instruction, in turn, addresses the memory to select the operand. The arithmetic unit is now commanded to accept the operand and execute the instruction.

4-35. In this chapter, we have discussed three of the five basic units of a typical computer system; that is, the memory, arithmetic, and control units. The next chapter presents a discussion of the two remaining computer units: input and output.

CHAPTER 5

Input-Output Units

THE INPUT AND output components of a computer system play an important role in interfacing the computer with various input-output devices. Without these components, computer communication with an input or output device would be difficult and time-consuming. In this chapter, we'll discuss the primary functions of the input and output components and the basic operating principles of several input-output devices.

1. Input and Output Components

1-1. There are many other names associated with these two components. For example, in some computer systems they are referred to as input-output control, and in other systems they are called input-output buffers. Normally, the input and output components of a computer system consist of the control, interface, and buffer circuitry that performs two primary functions:

(1) Decrease computer waiting time.

(2) Translate incoming and outgoing data to a usable form.

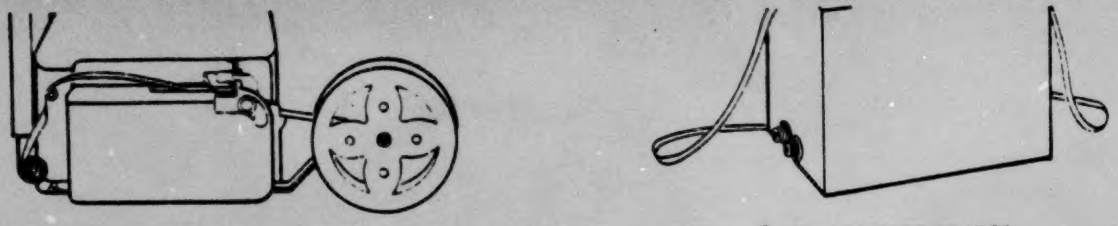
1-2. In many older computer systems, the input control and output control circuitry are separate entities in that they are in separate cabinets. This type of input and output control functions to provide communication with the computer on a device priority basis. In later computer systems, the input and output control circuitry is a physical part of an individual input or output device. Device priority in these systems is provided by the computer.

1-3. **Decreasing Computer Waiting Time.** As we know, computers work at very high speeds. This is understandable, since there is much work to be done in a minimum amount of time. If the computer demands information from an input device and then has to wait until the input device can deliver it, computer time is lost. The input system, therefore, includes a buffer device which greatly decreases the computer waiting time. An input buffer is a storage unit which is written into at the pace of the input device and read from, by the computer, at the computer's pace. An output buffer performs the same function in reverse between the computer and an output device. That is, the output buffer is written into at the fast pace of the computer and read from at the slower pace of the output device.

1-4. **Translating Incoming and Outgoing Data to a Usable Form.** In order for us to communicate with people who speak a different language, we need an interpreter. The same holds true when an input device communicates with the computer or the computer communicates with an output device. The interpreter in this case is the input or output control and interface circuitry which translates one language to another that is usable by the computer or an output device.

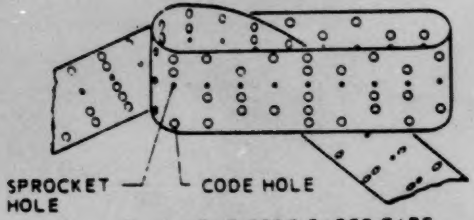
1-5. There are several types of input-output (I/O) devices associated with computer systems. Recall that an I/O device is also referred to as a peripheral device. The type of peripheral devices that will be discussed in the remainder of this chapter are indicated below. It is not the intention in our discussion of these peripherals to present the complete theory of operation for each device—this would just about require a complete CDC volume for each device. Our intention here is to discuss the more important basic operating characteristics of the devices and, in some instances, illustrate their basic, mechanical, and electronic features.

- Paper tape.
- Magnetic tape.
- Card punch.
- Card reader.
- Keyboard.
- Printer.



A PAPER TAPE PUNCH

B PAPER TAPE READER



C 5-HOLE CODE PAPER TAPE

Figure 5-1. Paper feed with associated reader and punch.

- Magnetic drum.
- Magnetic disk.

2. Tape-Handling Devices

2-1. There are two types of tapes available for use with computer systems: paper and magnetic. Both types can be used for either input or output functions. Each type of tape has its own distinctive processing equipment, and the tapes are not interchangeable. A paper tape must be used with a paper punch and reader, and a magnetic tape must be used with a tape transport unit.

2-2. **Paper Tape.** Paper tape is normally used as an I/O device, but it can also be used as a memory device for storing computer outputs. Information is coded on the basis of a hole-no-hole code. In a typical system, the holes are punched in the tape by using a manual keyboard-type paper-tape punch or by a computer-controlled paper punch. Normally, a computer-prepared tape is an output function and a keyboard-prepared tape is an input function. A paper tape, with the associated paper-tape punch and reader, is shown in figure 5-1.

2-3. The paper-tape reader interprets and converts the punched paper tape into electrical impulses for input into a printout device or computer unit. This is done by sensing a pattern of hole-no-hole with a photoelectric system or a system of metallic brushes. The reader circuitry is also used to verify the correctness of a keyboard-prepared tape before the tape is processed as input information.

2-4. A paper-tape system is relatively slow for processing information. It is, however, less expensive than a magnetic tape system and is generally used with a special-purpose computer solving scientific problems of a fixed type.

2-5. **Magnetic Tape.** Magnetic tape is a thin, flexible plastic tape with a uniform coating of ferrous oxide on one side similar to the tape used in home-style tape recorders. The coating varies with the commercial processes used to manufacture the tape and is composed of magnetic properties that enable it to be magnetized in discrete units (very small magnetized spots). Different patterns of magnetized spots represent information. In one form of tape recording, a magnetized spot (bit) may represent a binary 1; a nonmagnetized spot on the tape may represent a binary 0. A more common system of recording on tape requires that both 1's and 0's be expressed as magnetized bits. This

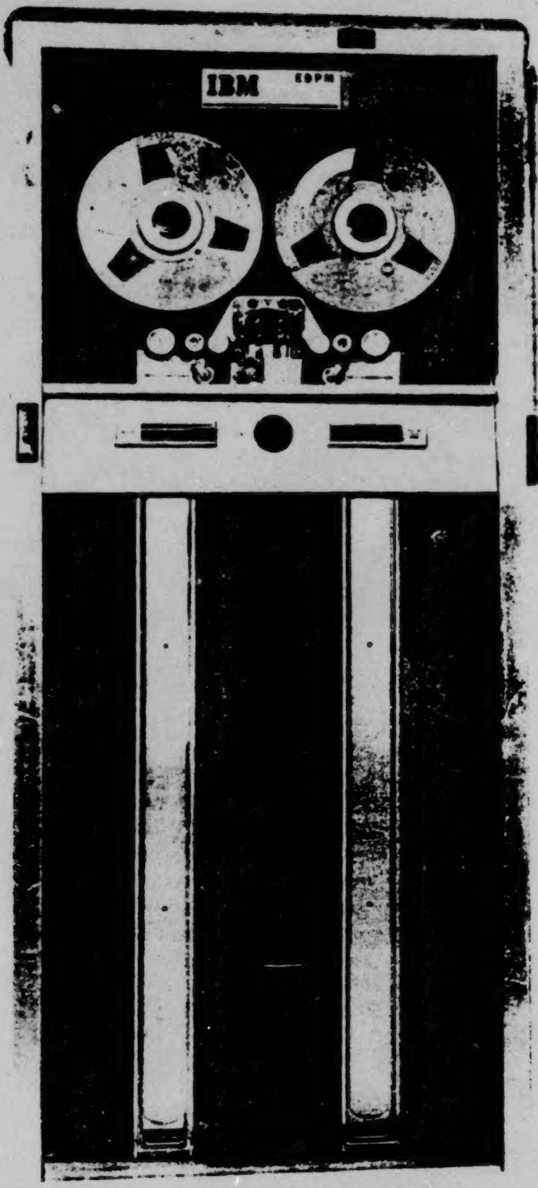


Figure 5-2. Magnetic tape transport unit.

is accomplished by recording 1's with a north-south magnetic alignment and 0's with a south-north alignment. A large amount of information can be stored on a length of tape. A typical tape is about 2000 feet in length and has a word density of 40 or more computer words per inch.

2-6. Information may be transferred to magnetic tape through various means such as special typewriters, card-to-tape converters, card machines, from a magnetic drum, or directly from a computer. Once information is transferred to magnetic tape, the reel of tape can either be stored for future use or placed in a tape transport unit. If placed in a tape transport unit, the information on the tape is then read by the read-write head(s) of this unit and the pulse pattern transferred to the computer. A typical magnetic tape transport unit is illustrated in figure 5-2.

2-7. Tapes are also used to receive and record computer outputs. The outputs are processed from the computer to the tape unit. Generally, the information is left on the tape for future use. But if a hard-copy printout of the tape is desired, then this can be accomplished through the use of an auxiliary device (connected separate from the computer), thereby maintaining the high speed of the computer outputs.

2-8. Tapes are slow-access memory-type storage units. They are normally classified as an I/O device, since they are used initially to load information into the computer and then to record computer outputs.

2-9. *Write operation.* Writing on magnetic tape occurs as the tape is moving across the magnetic gap of a recording or write head. Electrical pulses are sent through the recording head coils at desired intervals, and the oxide coating is magnetized by these pulses. These magnetized areas may be later sensed as a 0 or 1. The number of recording tracks in a write head is determined by the code that is used to represent alphabetic and numeric characters.

2-10. Magnetic tape moves at high speed during write and read functions. Typical speeds are 75 inches per second and 112.5 inches per second. The write pulses to the

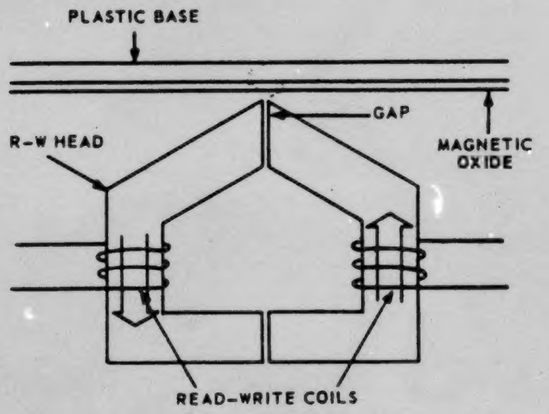


Figure 5-2A. One-gap read-write head.

write heads are fast enough that the magnetized spots are almost the same as if the tape were stopped for the time that the pulse is present.

2-11. Figure 5-2A shows one type of read-write head used with tape. This head has a single gap for each channel. The head shown in figure 5-2B has two magnetic gaps. One gap is used for writing and the other is used for reading. The principles of reading and writing are the same for both type heads. However, the two-gap head has the advantage of being able to read the data immediately after it is written. This allows data to be immediately checked for errors.

2-12. If it is vital that information on a tape remain unaltered while on line (not

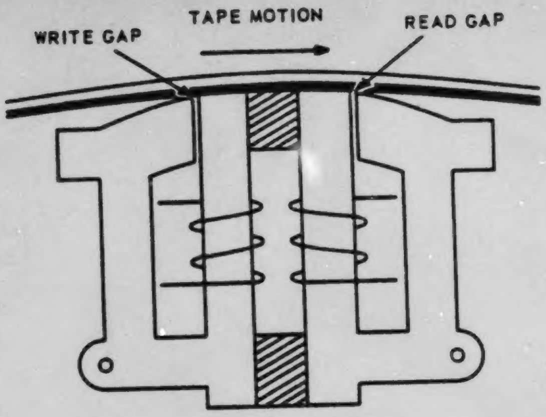


Figure 5-2B. Two-gap read-write head.

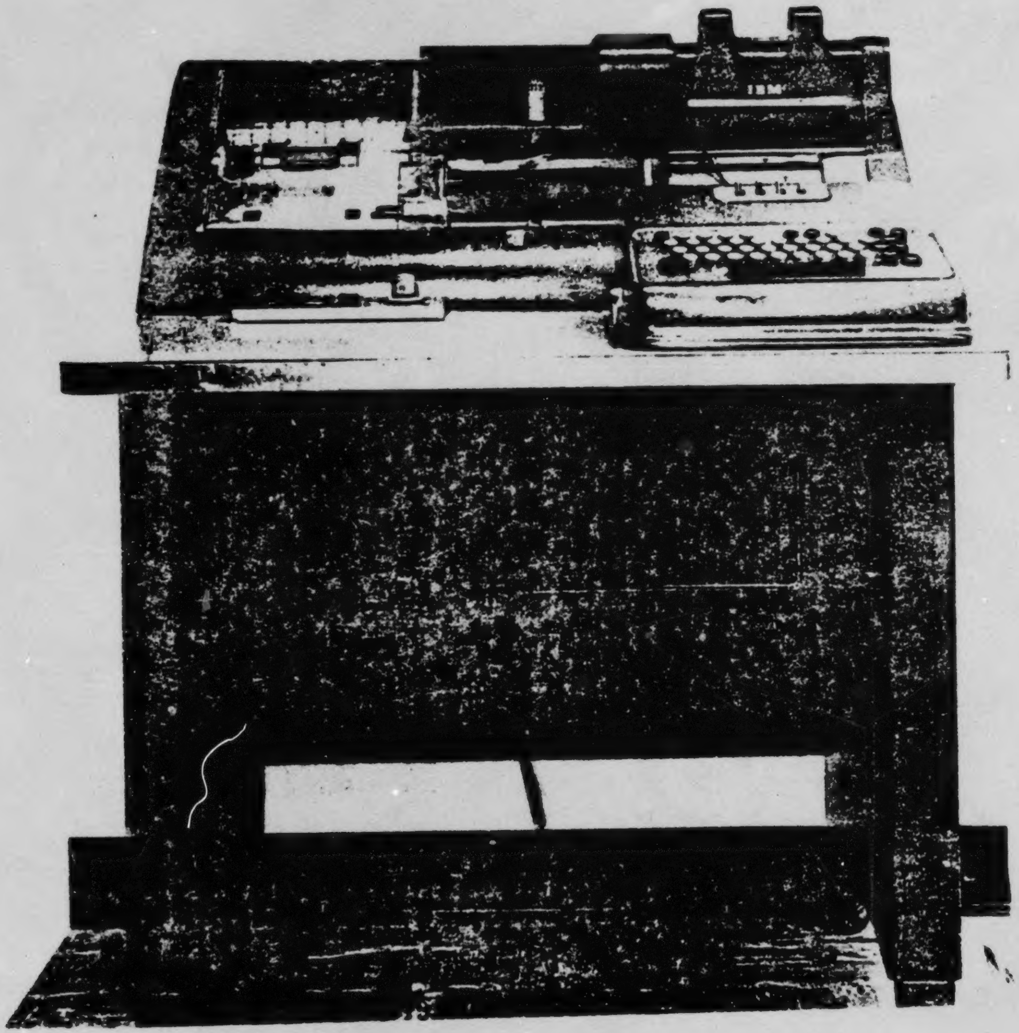


Figure 5-3. Computer entry punch.

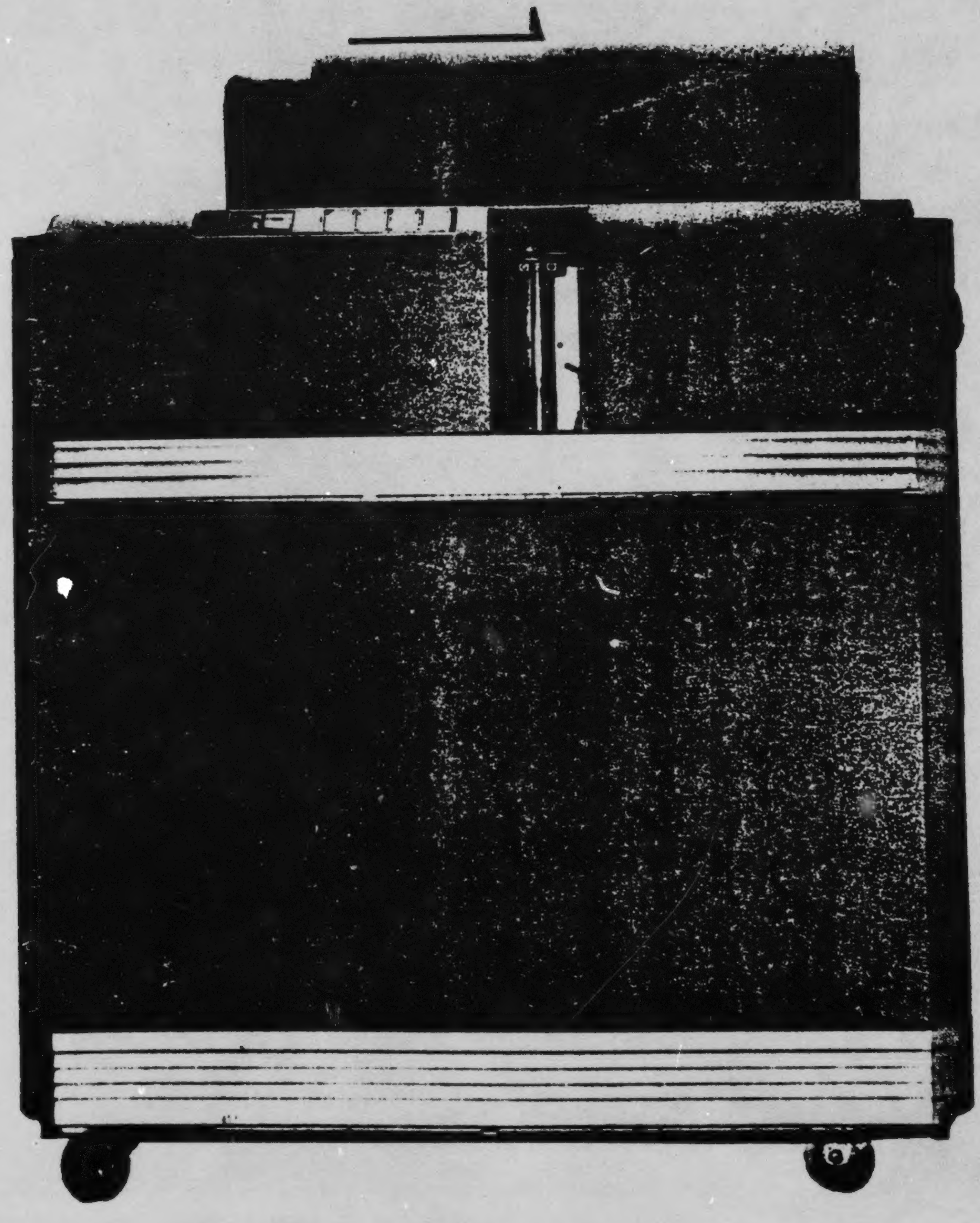


Figure 5-4. Computer-operated card punch.

written on), there is a means of protecting it. On many tape reels, there is a circular groove on the back of the reel. A pawl must ride in this groove to inhibit the writing operation. There is a plastic ring that fits into this groove; it is called the *file protection ring*. When installed, it keeps the pawl depressed, which allows writing on the tape to take place.

2-13. *Read operation.* During the read operation from magnetic tape, the magnetized spots pass the gaps in the read head and small pulses which represent data are induced in the coil of the read head and sent to the computer.

2-14. During the writing operation on magnetic tape, old information is erased from the tape. Reading does not erase, so the tape can be read over and over.

3. Card-Handling Devices

3-1. The term *card machines* includes all units of a card-handling system that use holes punched in paper cards to represent information. Such a system must be capable of punching information cards, reading the information from the punched cards, and printing it in a form that can be directly read without further decoding. A complete card-handling system includes a card punch and a card reader/printer.

3-2. Card Punch. The equipment used to manually punch information onto a card is a card punch. A manual card punch is an electromechanical device which punches information holes in the cards and prints the same information along the top of the cards. An operator performs the punching operation at a keyboard similar to a standard typewriter keyboard. A typical example of a manual card punch is illustrated in figure 5-3. This particular card punch also performs the additional function of reading the punched cards and converting the information into a pulse-no-pulse pattern for direct computer input. This type of punch is called a *computer-entry punch*. First, the card is punched; then the card is automatically sent to the reading station. At the reading station, mechanical contacts sense the hole-no-hole pattern and generate voltages corresponding to this pattern which, in turn, are fed to the computer.

3-3. A card punch for transferring outputs from the computer to cards is illustrated in figure 5-4. This card punch is operated by the computer through circuits controlled by the program. The computer generates voltages which operate punch-select electromagnets which activate the *punch dies* that actually punch the hole in the card. When the punches operate, they punch out a card-hole pattern corresponding to the computer output information. No manual operation of this machine is required. The computer-operated card punch is faster than the manual-operated punch. It processes about 100 cards per minute while the manual-operated punch is limited to the skill of the operator. A processing of about three cards per minute is within an operator's capability.

3-4. *Punched cards.* Practically all computer systems today use punched cards

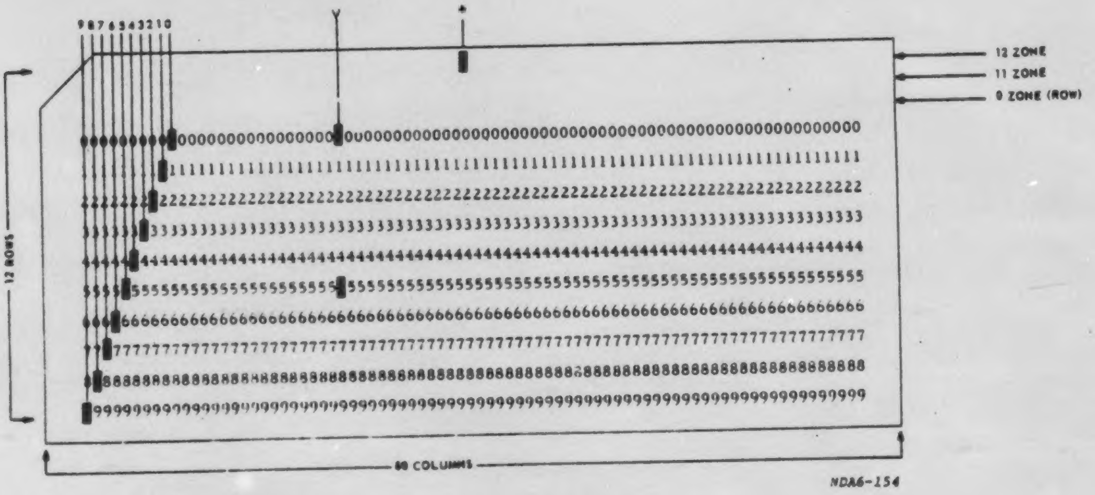


Figure 5-5. A Hollerith coded card.

TABLE 5-1
HOLLERITH CODE

NUMERIC PUNCH	NO ZONE	12 ZONE	11 ZONE	0 ZONE
NONE	(BLANK)	&	-	0
1	1	A	J	/
2	2	B	K	S
3	3	C	L	T
4	4	D	M	U
5	5	E	N	V
6	6	F	O	W
7	7	G	P	X
8	8	H	Q	Y
9	9	I	R	Z
8–3	#		$	
8–4	@	⌑	*	%

NDA6-152

for data input, output, and storage functions. Punched cards are very common; in fact, your Government payroll check is one form of this card. The information contained on the card is in the form of holes. It is easy to understand this system. A hole represents a YES state, or a ONE; and the absence of a hole represents the NO state, or ZERO.

3-5. A standard punched card is illustrated in figure 5-5. Cards often contain a cut corner, usually at the top left or right corner of the card. These corner cuts are normally used to identify a type of card visually, or to insure that all cards in a group are facing the same direction and are right side up.

3-6. The card in figure 5-5 is divided into 80 vertical columns, called card columns. These are numbered 1 to 80 from left to right. Each column is then divided into 12 punching positions which form 12 horizontal ROWS across the card. The punching positions are designated from the top to the bottom of the card by 12, 11, 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. The 0 through 9 punching positions correspond to the numbers printed on the standard stock card. The 12 and 11 punching positions normally are not printed on the card, since this area is generally reserved for printed headings or for interpreting punched information.

3-7. Since one or more punches in a column represent a character, the number of columns used depends on the amount of data to be punched. If a record requires more than 80 columns to hold its data, two or more cards may be used. However, continuity between cards of one record must be established by punching identifying information in a particular column of each card.

3-8. The top edge of the card is known as the "12" EDGE, and the bottom edge as the "9" EDGE. The manner in which cards are placed in machines is governed by their respective feeding requirements. Therefore, cards are fed either 12 edge first or 9 edge first, and either FACE UP, which means the printed side of the card is facing up, or FACE DOWN, meaning the opposite. Cards are read and punched by machines, either row by row or column by column.

3-9. *Hollerith code.* The standard card language, commonly referred to as the

Hollerith code, uses the 12 punching positions of a vertical column to represent numeric, alphabetic, or special character punching. These 12 positions are divided into two areas known as numeric and zone. The first nine punching positions from the bottom edge of the card are the NUMERIC or DIGIT positions of 9 through 1. The remaining 0, 11, and 12 are the ZONE positions. (The 0 is used interchangeably to represent a zone punch or numeric punch.)

a. Numeric—Rows 0 through 9 are used to store the 10 decimal digits and are represented by a single punch in a particular column. For example, a single punch in the 0 zone position would represent an assigned numeric value of zero.

b. Alphabetic—To accommodate any of the 26 letters in one column, a combination of a zone and digit punch is used. The alphabet is divided into three groups, and each group is identified with one of the three uppermost rows, or zones. The first nine letters of the alphabet, A through I, use a 12-zone punch and a numeric punch of 1 through 9, respectively. The 12 punch

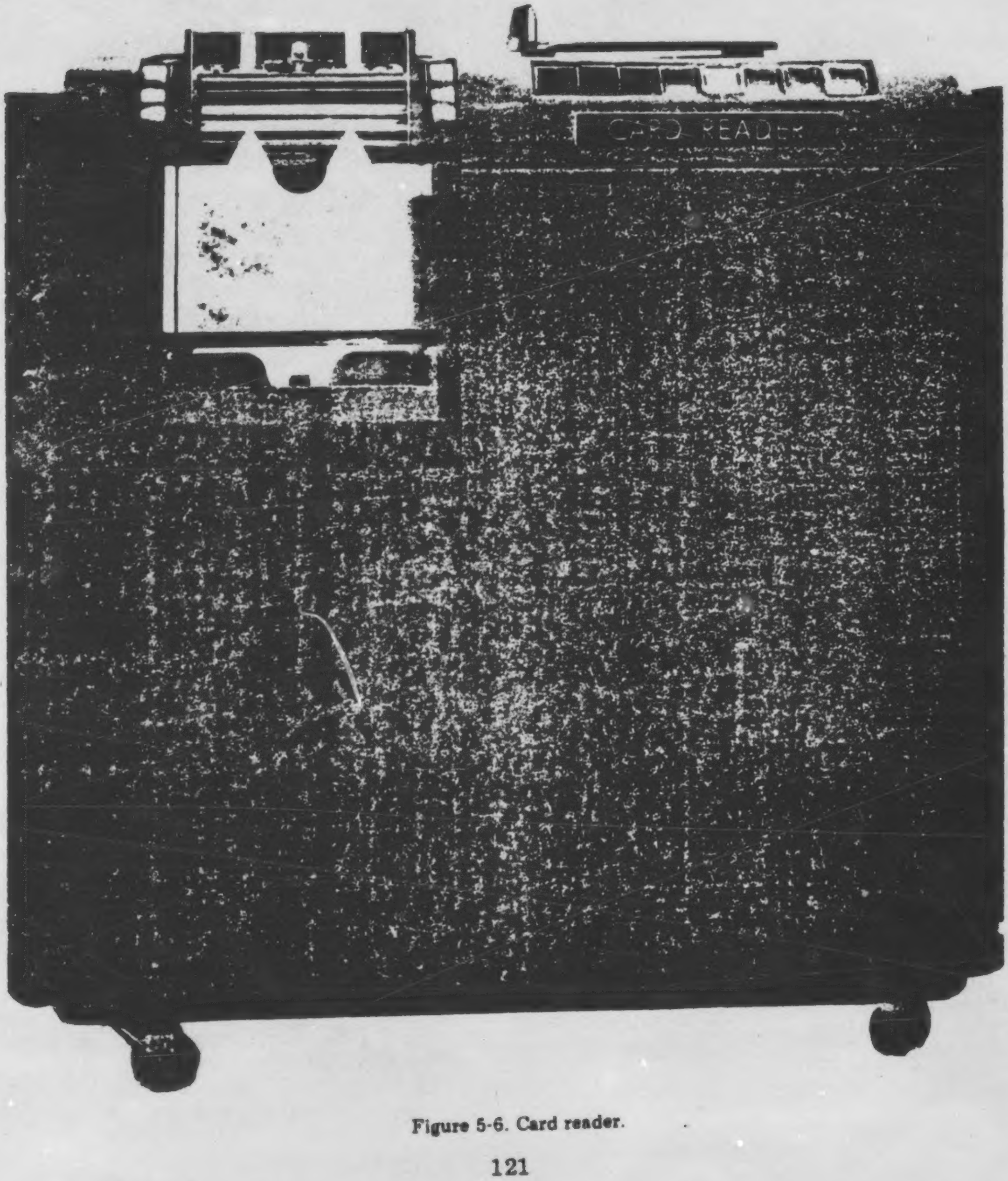


Figure 5-6. Card reader.

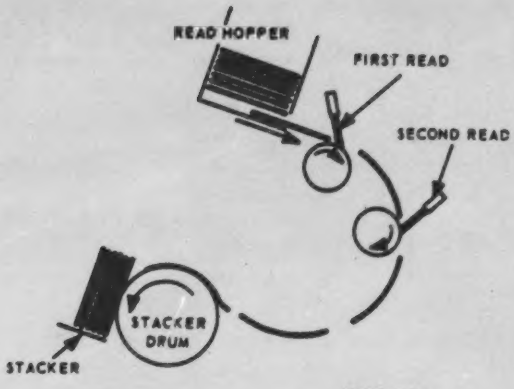


Figure 5-7. Brush reading.

indicates that the character in that column lies in the first group of nine letters of the alphabet. A punch in any of the 1 through 9 rows of the same column specifies which letter of the nine is represented. (Thus, 12 and 1 represent A, 12 and 2 represent B, etc.) The second group of nine letters, J through R, use the 11-zone punch and a numeric punch 1 through 9, respectively. (Thus, 11 and 1 represent J, 11 and 2 represent K, etc.) Since only eight letters are left for the 0 zone, letters S through Z are represented by the 0 zone punch and a numeric punch 2 through 9, respectively.

c. Special Characters—These characters provide printed symbols, cause certain machine operations to occur, and identify various cards. Standard special characters consist of one, two, or three punches in a card column but differ from the configurations used to represent numeric or alphabetic characters. Figure 5-5 shows the special character + represented by a 12-zone punch. Normally (depending on the type keyboard), 11 special characters are available for punching. Refer to Table 5-1 for the complete Hollerith code.

3-10. Card Reader. There are many different types of card readers available for use with a computer system, and from system to system the type used might be different. A typical card reader is illustrated in figure 5-6. Regardless of the type of reader you are familiar with, its primary function is to convert the hole-no-hole data on punched cards into electronic form for input into a computer. Two common methods of reading this data from punched cards are reading brushes and photoelectric cells.

3-11. *Reading brushes.* In the brush-type card reader, cards pass between a set of reading brushes and a contact roller. The brushes electrically sense the presence or absence of holes in each column of the card, as illustrated in figure 5-7. The card reader circuitry utilizes the electrical impulses that are converted from the electrical sensing and stores them as data.

3-12. After the cards have been read, they are passed onto the card stacker and stacked in the same sequence as they were read. Some card readers have two sets of reading brushes, as illustrated in figure 5-7. This enables each card to be read twice as it moves through the card feed unit. Two sets of brushes serve as a check on the validity of the reading process.

3-13. *Photoelectric cells.* The photoelectric-type card reader performs the same function as the brush type; the only difference is in the method of sensing the holes. Photoelectric card reading is performed by 12 photoelectric cells, one for each of the 12 rows of the card. Cards are passed between the photoelectric cells and the light source. If the cards are punched, the light penetrates the holes and activates the photoelectric cells; thus, a ONE is detected.

3-14. Another use for a card reader is to provide a medium for transcribing punched card data onto magnetic tape for use in magnetic tape systems. The magnetic tape can then be used as direct input to the computer.

4. Keyboards

4-1. A keyboard is basically a typewriter. However, there is a difference in the primary function of the two. As you know, a typewriter's primary function is to produce a hard copy of the keys depressed by an operator; whereas a keyboard's primary function is to input information to or output information from a computer.

4-2. Keyboard as an Input Device. Many computer systems utilize a keyboard with a digital encoder as an input device. When a key is depressed, the encoder converts the action of depressing that particular key to a digital code. By this means, it is possible to insert data into a digital computer in the computer's language—digital code. In this case, the keyboard and its encoder function as an interpreter between man and machine. At the same time you are inputting data into the computer, a hard copy is being produced which allows you to verify the keys you depressed.

4-3. As an input device, the keyboard is very useful. It can be used to select other I/O devices for reading or writing, and it causes the actual reading or writing of that device to occur. This is a very useful feature in that it is a simple matter to initialize a computer system for its primary mission through the use of the keyboard.

4-4. **Keyboard as an Output Device.** As an output device, the keyboard is under control of the computer. The computer can then inform the operator of program actions required. A hard copy of maintenance program results is provided by the keyboard facility under computer control. One of the most useful output features of the keyboard is the instant identification of system integrity. That is, all failures, including pertinent failing data, are made available under computer control to maintenance personnel.

4-5. One of the most difficult problems that you might encounter with a keyboard is in the actual typing of characters—the mechanics of the keyboard. For this reason, we will present a discussion of the typing principles associated with a typical keyboard.

4-6. **Typing Principles.** Since we have compared the keyboard to a typewriter, let us discuss how the keyboard causes the actual typing of characters to take place. The way it types is a clue to how it generates digital codes (input device) and types from digital codes (output device).

4-7. The typewriter portion of our *typical keyboard* is not a conventional typewriter. Instead of a hammer (with a character on it) flying up and striking a ribbon, a ball (with many characters on it) rotates, tilts, and then strikes the ribbon when a key is depressed. Our typewriter then has the characters imprinted on a typehead ball, as illustrated in figure 5-8. This is the action that we want to discuss then: What causes the ball to rotate and tilt to a desired character, move forward, and strike the ribbon when a keyboard key is depressed? Now look at figure 5-9; it shows the typehead character arrangement of the typehead ball illustrated in figure 5-8.

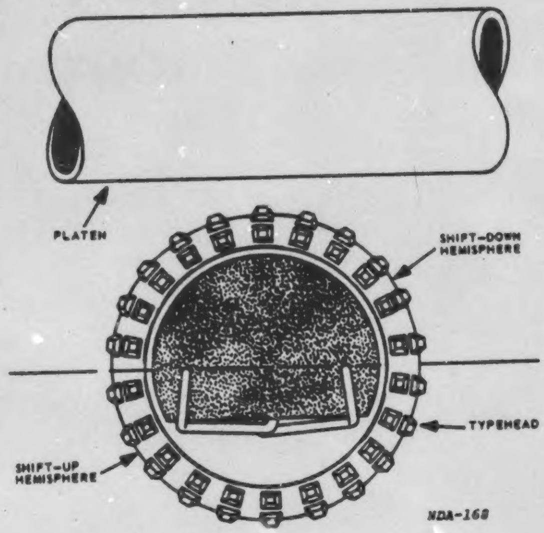
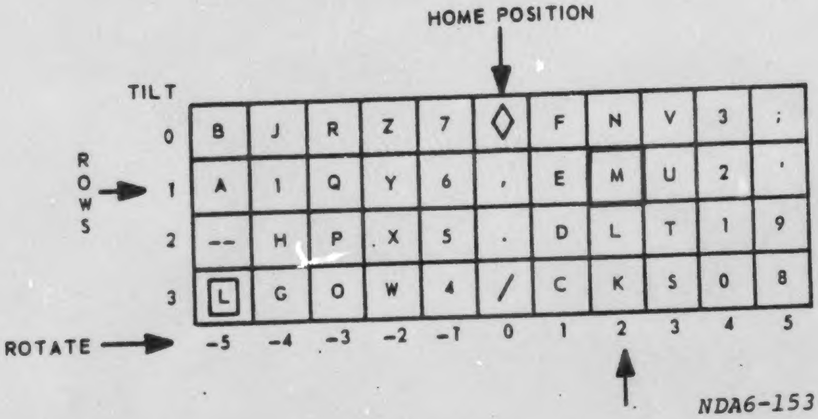


Figure 5-8. Typehead and platen.

4-8. Note that the typehead ball in figure 5-8 is divided into two character hemispheres—shift-up and shift-down. Now look at figure 5-9. It shows the character arrangement for the shift-down hemisphere of the typehead ball. In order to simplify this



TILT	-5	-4	-3	-2	-1	0	1	2	3	4	5
0	B	J	R	Z	7	◊	F	N	V	3	;
1	A	1	Q	Y	6	,	E	M	U	2	'
2	--	H	P	X	5	.	D	L	T	1	9
3	L	G	O	W	4	/	C	K	S	0	8

Figure 5-9. Typehead character arrangement.

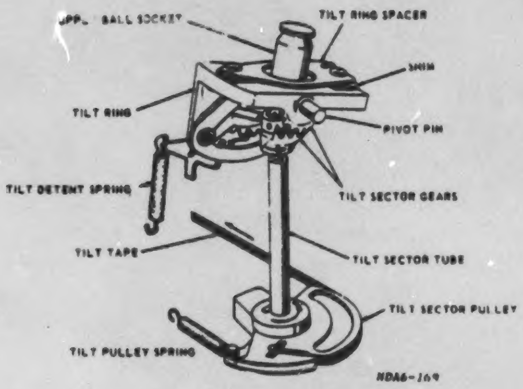

UPPER BALL SOCKET
TILT RING SPACER
SHIM
TILT RING
PIVOT PIN
TILT DETENT SPRING
TILT SECTOR GEARS
TILT TAPE
TILT SECTOR TUBE
TILT SECTOR PULLEY
TILT PULLEY SPRING
NDA6-169

Figure 5-10. Rocker portion of tilt mechanism.

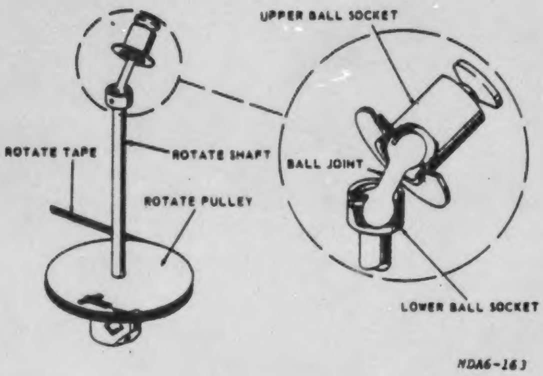

UPPER BALL SOCKET
ROTATE TAPE
ROTATE SHAFT
BALL JOINT
ROTATE PULLEY
LOWER BALL SOCKET
NDA6-163

Figure 5-11. Rocker portion of rotate mechanism.

discussion, we'll use only characters in the shift-down hemisphere.

4-9. *Character selection.* From the typehead character arrangement in figure 5-9, it should be apparent that selection of a character is done by two different movements of the typehead: rotate and tilt. For example, to select the letter M, the typehead must be tilted 1 row and rotated 2 columns in the positive direction. This is expressed as tilt 1, rotate +2. All movements are with respect to the tilt 0, rotate 0 (home) position of the typehead. The typehead returns to this position after typing each character. For example, typing the word "ARE" causes the following action to take place:

- Depress key A - Typehead tilts 1, rotates -5, moves forward to strike ribbon, moves back, and returns to home position.
- Depress key R - Typehead tilts 0, rotates -3, moves forward to strike ribbon, moves back, and returns to home position.
- Depress key E - Typehead tilts 1, rotates +1, moves forward to strike ribbon, moves back, and returns to home position.

4-10. *Tilt and rotate mechanism.* The typehead is tilted and rotated by gears, tapes, and pulleys. First, let us examine the tilt

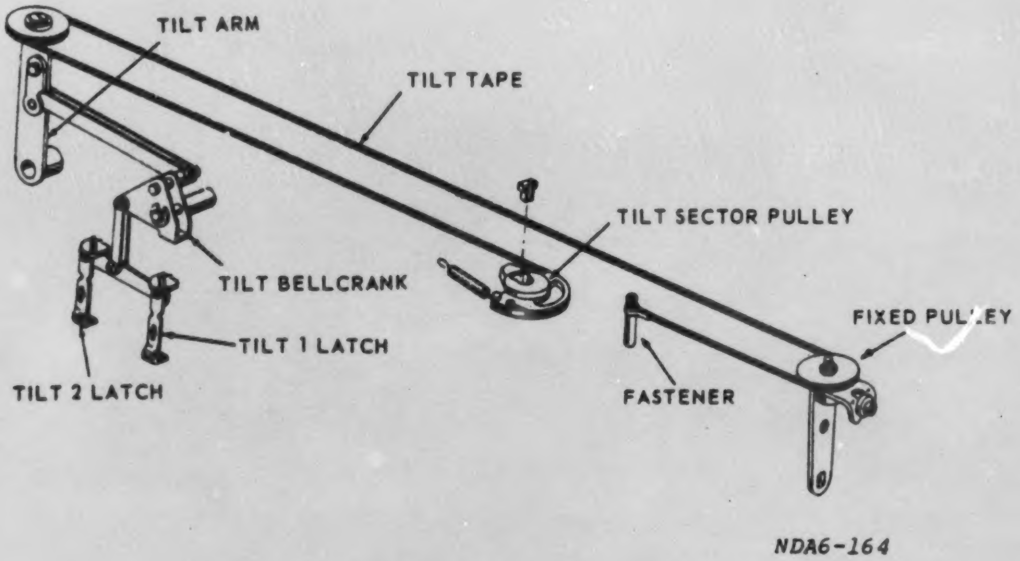

TILT ARM
TILT TAPE
TILT SECTOR PULLEY
TILT BELLCRANK
FIXED PULLEY
TILT 1 LATCH
TILT 2 LATCH
FASTENER
NDA6-164

Figure 5-12. Tilt tape system.

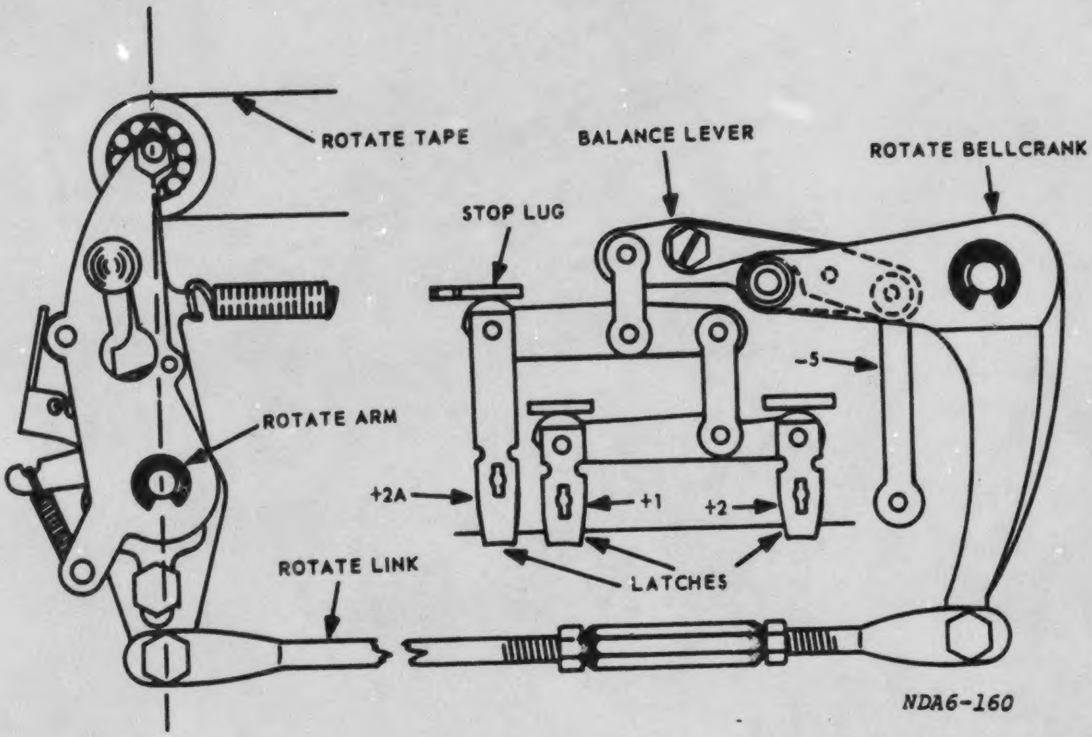

ROTATE TAPE
BALANCE LEVER
ROTATE BELLCRANK
STOP LUG
-5
ROTATE ARM
+2A
+1
+2
LATCHES
ROTATE LINK
NDA6-160

Figure 5-14. Rotate differential at rest.

selector lug, illustrated in figure 5-15. When pushed down, it rotates the typehead to the +1 column. The latch labeled +2 is the R2 latch; it causes the typehead to rotate to the +2 column. When both R1 and R2 are pushed down, the typehead rotates to the +3 column. Latch R2A (labeled +2A) is never used alone; it adds with R2 to provide +4 rotation. R2A, R2, and R1 add to provide +5 rotation.

4-15. The latch labeled - 5 is called the R5 latch; it functions in conjunction with the R5 lug of the interposer. This latch only functions during negative rotate operation; that is, columns - 5, - 4, - 3, - 2, and - 1 in figure 5-9. Combining the action of the - 5 latch, in figure 5-14, with the positive latches, results in a negative rotate operation of the typeball. For example (refer to figs. 5-14 and 5-15):

Interposer Lug (Selector Latch)	=	*Typeball Rotation*
R5(-5)+R2(+2)+R2A(+2)	=	-1
R5(-5)+R2(+2)+R1(+1)	=	-2
R5(-5)+R2(+2)	=	-3
R5(-5)+R1(+1)	=	-4
R5(-5)	=	-5

4-16. *Latch selection.* Now we'll see how depressing a key selects the latches to be

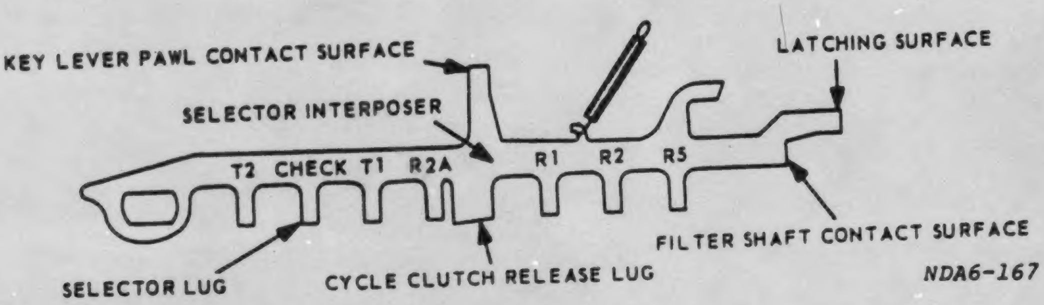

KEY LEVER PAWL CONTACT SURFACE
LATCHING SURFACE
SELECTOR INTERPOSER
T2
CHECK
T1
R2A
R1
R2
R5
FILTER SHAFT CONTACT SURFACE
SELECTOR LUG
CYCLE CLUTCH RELEASE LUG
NDA6-167

Figure 5-15. Interposer.

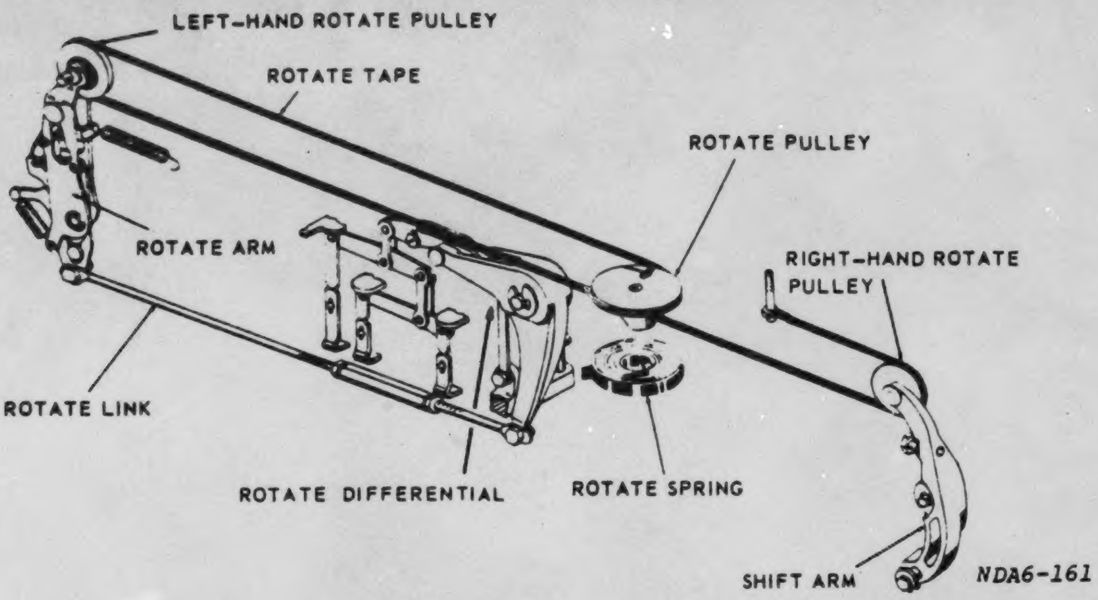


Figure 5-13. Rotate tape system.

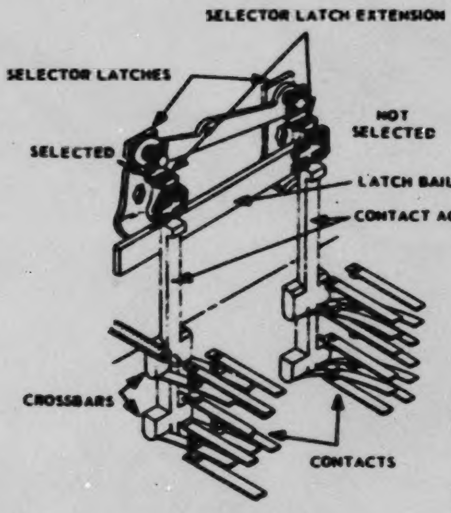
mechanism which is shown in figure 5-10. The typehead fits over the upper ball socket. The typehead has been removed in the illustration in order to show the tilt mechanism. Rotating the tilt sector pulley rotates the bottom tilt sector gear. This rotating motion is translated into a tilting motion by the gears and causes the tilt ring and upper ball socket to tilt. Notice the arrows on the figure. Pulling the tape in the direction of the arrow causes the tilt ring to tilt up. Since the typehead is fastened to the ball sockets, the typehead tilts in the same direction as the tilt ring. When the tape is released, the spring pulls the pulley back to its original position, setting the typehead back to the 0-tilt position.

4-11. Now let us see how the typehead is rotated. Look at figure 5-11; it shows the upper ball socket connected to a rotate shaft. The two ball joints between the shaft and the upper ball socket allow the typehead to be moved in both the rotate and tilt directions. Notice that the rotate pulley is also moved by pulling on a tape attached to the pulley. Now that you understand that pulling on a tilt tape tilts the typehead and pulling on a rotate tape rotates the typehead, the next step is to take a look at the mechanical linkages that pull the tapes. We are progressing from the motion of the typehead to the motion of the typekey. This may seem like going backward, but it is the easiest way to see this action.

4-12. *Tilt tape system.* This system is shown in figure 5-12. One end of the tilt tape is fastened to the tilt sector pulley. The other end passes over a pulley on the tilt arm, over a fixed pulley, and then to a fastener. The tilt arm pivots at the bottom, and, in doing so, it pulls the tape, rotating the tilt sector pulley. How much pull and how much the typehead tilts is controlled by two latches: tilt latch 1 and tilt latch 2. These tilt latches are in effect mechanical adders that have four positions: tilt position 0 through tilt position 3. The important thing to note here is that these four tilt positions correspond to the four rows of characters illustrated in figure 5-9.

4-13. *Rotate tape system.* This system is illustrated in figure 5-13. Again, a rotate arm is tilted by a mechanical linkage to position the rotate pulley. For our explanation, consider the right-hand pulley as fixed, since we stated earlier that for simplicity we would not discuss the shift-up. The rotate differential that tilts the left-hand pulley is shown in figure 5-14.

4-14. Because the rotate differential must position the typehead in 10 different positions other than 0 rotate (these positions correspond to the 11 columns shown in figure 5-9), it has a more complicated linkage. Note that the latches are all at rest in figure 5-14. The latch labeled +1 is called the R1 latch, because it is selected by the R1 interposer



NDA6-159

Figure 5-18. Control actuator.

selector bails that are contacted are forced forward to engage the latch interposers. The latch interposers move forward, pulling the selector latches back.

4-18. Look at figure 5-18 and note the latch bail. The same mechanism (cycle clutch bail) that allows the filter shaft to rotate causes a downward movement of this latch bail. If a selector latch *is selected*, it is pulled back and, as the latch bail moves down, it *doesn't* make contact with the contact actuator. Therefore, the normally closed (NC) contact points associated with that particular selector latch remain closed. If a selector latch *is not selected*, it is not pulled back and, as a result, the following actions occur:

- The latch bail pulls down on the selector latch.
- The selector latch extension moves down.
- The contact actuator arm moves down.
- The contact actuator crossbars open the NC contacts.
- When the selector latch bail restores, the contact actuator rises under the spring tension of the opened contacts.

4-19. The above action is true for all the selector lugs on each interposer (fig. 5-16) except lug R5 (-5 rotate). Its point contacts are normally opened (NO) and remain opened for all positive (including 0) column rotate positions. These were illustrated in figure 5-9. When a negative column rotate position is required, the R5 contacts are closed.

4-20. Let us tie together the mechanical rotate-tilt mechanism, the latch selection, and the binary field data code associated with our typical keyboard. Figure 5-19 is a simplified schematic of switches associated with the field data code. These switches are arranged in the order of our field data code excluding the control bit (D6) and the parity bit (D7). Negative logic levels of - 12V (logic 1) and 0V (logic 0) are used for our explanation. Notice that each data bit (D0 through D5) is controlled by the operation of interposer lugs T1, T2, R5, R1, R2, and R2A. Recall that these lugs control the operation of corresponding selector latches as explained above. Now refer to figure 5-9 and locate the letter A; it is selected by rotating the typehead - 5 units and tilting it 1 unit. To obtain this mechanical movement, the following latches must be selected:

- Rotate latches:

	R2A	R2	R1	R5
Rotation	0	0	0	-5

- Tilt latches:

	T2	T1
Tilt	0	1

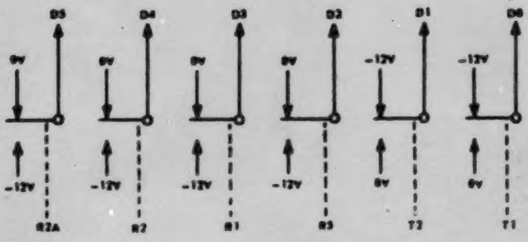
4-21. Notice in figure 5-19 that the following contacts are transferred by its associated latch.

Contacts:	D5	D4	D3	D2	D1	D0
Transferred:	yes	yes	yes	yes	yes	no
Voltage:	0V	0V	0V	-12V	-12V	0V
Binary:	0	0	0	1	1	0

The resultant field code for character A is $000110_{(2)}$ which is equal to $06_{(8)}$.

5. Printers

5-1. A printer provides another means of



NDA6-155

Figure 5-19. Digital coding switches.

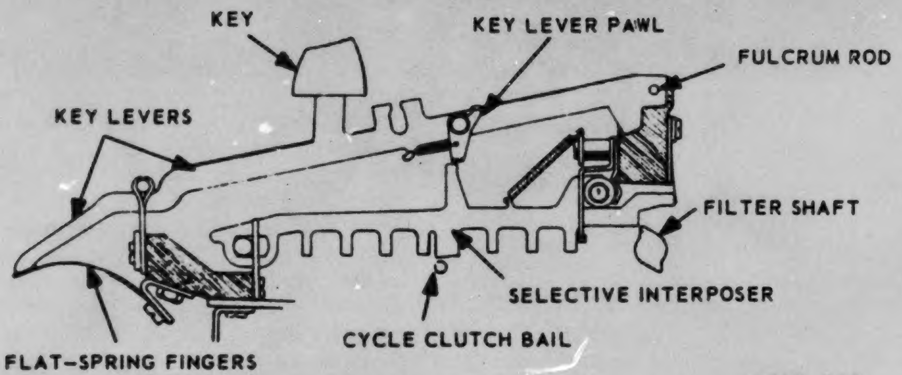

KEY
KEY LEVER PAWL
FULCRUM ROD
KEY LEVERS
FILTER SHAFT
SELECTIVE INTERPOSER
CYCLE CLUTCH BAIL
FLAT-SPRING FINGERS
NDA6-165

Figure 5-16. Key and interposer mechanism.

operated and at the same time generates a digital code. Figure 5-16 shows a key attached to its key lever pawl and its selective interposer mechanism. When the key is depressed, the key lever pawl strikes the selective interposer. This action causes the interposer to move down in front of the filter shaft. The large-cycle clutch-release lug of the interposer, shown in figure 5-15, releases a clutch that allows the filter shaft (fig. 5-16), which is geared to an electric motor, to rotate 180° and forcing the interposer forward.

4-17. Note in figure 5-16 that there are seven lug positions on each interposer in addition to the clutch-release lug. A combination of these lugs determines the character to be printed and a particular code to be transmitted. Each key has its own selective interposer. When a key is depressed, the key lever pushes its selective interposer down so that each selector lug rests immediately behind the selector bail, as shown in figure 5-17. The cycle clutch is released, the filter shaft rotates, and the

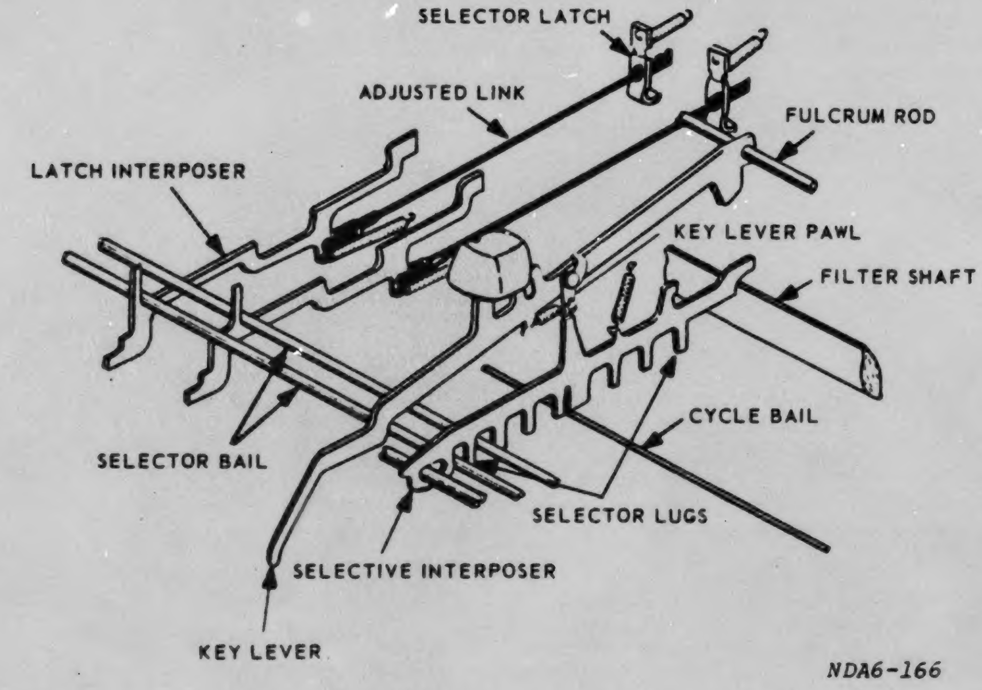

SELECTOR LATCH
ADJUSTED LINK
FULCRUM ROD
LATCH INTERPOSER
KEY LEVER PAWL
FILTER SHAFT
CYCLE BAIL
SELECTOR BAIL
SELECTOR LUGS
SELECTIVE INTERPOSER
KEY LEVER
NDA6-166

Figure 5-17. Selection.

outputting data from a computer. Data from the computer system are provided in permanent visual records, at rates ranging from a few characters to several hundred characters per second. As output units, printing devices receive data from the computer system is symbolized electronic form. Once these electronic signals enter the appropriate circuits and actuate the printing elements, printing takes place. The two types of printers discussed here include the impact and electrographic printer.

5-2. Impact Printer. The impact printer (sometimes referred to as a line printer) is an outgrowth of the typewriter. The term *line* designates that the printer is capable of printing a line of characters at a time. Impact printers vary in speed of printout from about 100 lines per minute to over 1000 lines per minute. The number of characters per line also varies from one type of impact printer to another.

5-3. *Mechanical description.* The mechanical parts that do the work of printing in a typical line printer are shown in figure 5-20. The printing operation is accomplished by the print hammer striking the paper-and-ink ribbon against a raised character on the print wheel, thereby impressing the character on paper in the same manner as on a typewriter. An advantage of this type of printing is that multiple carbon copies may be produced.

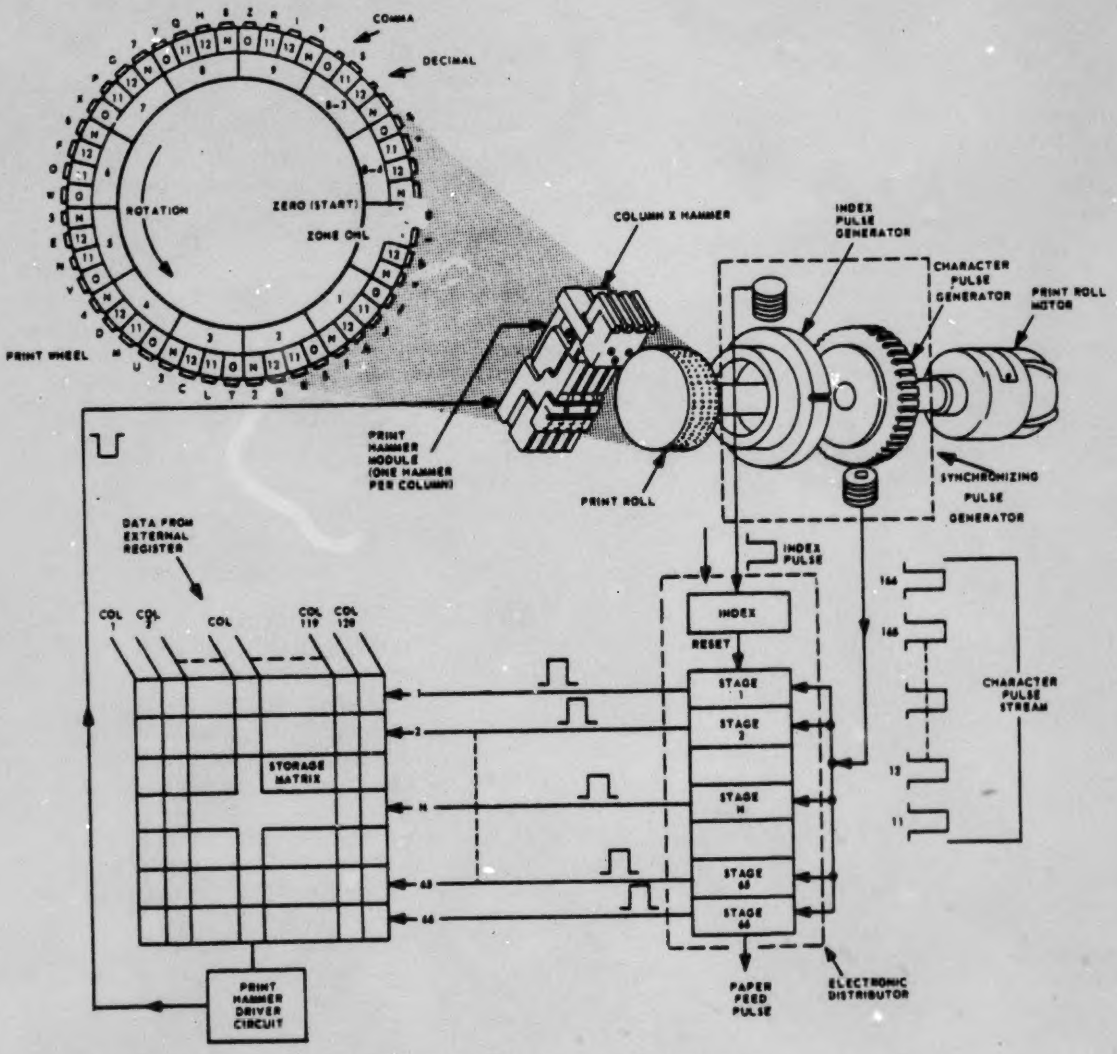

COMMA
DECIMAL
ROTATION
ZERO (START)
PRINT WHEEL
COLUMN X HAMMER
INDEX PULSE GENERATOR
CHARACTER PULSE GENERATOR
PRINT ROLL MOTOR
PRINT HAMMER MODULE (ONE HAMMER PER COLUMN)
PRINT ROLL
SYNCHRONIZING PULSE GENERATOR
INDEX PULSE
DATA FROM EXTERNAL REGISTER
COL 1
COL 2
COL
COL 119
COL 120
INDEX
RESET
STAGE 1
STAGE 2
STAGE N
STAGE 65
STAGE 66
STORAGE MATRIX
1
2
N
65
66
CHARACTER PULSE STREAM
12
11
PAPER FEED PULSE
ELECTRONIC DISTRIBUTOR
PRINT HAMMER DRIVER CIRCUIT

Figure 5-20. Impact printer diagram.

5-4. The hammers are mounted in modules. A typical impact printer has four hammers per module. There is a print hammer for each vertical column of print; or, to put it another way, there is a hammer for each possible character in a line of print. Each hammer has its own driving electromagnet which is activated with an electrical pulse.

5-5. The print roll consists of a number of individual wheels (as many as 120) mounted on a common shaft. Each of these print wheels has raised characters around its outer edge, as shown on the insert of figure 5-20. When these print wheels are mounted to form the full print roll, all like characters are aligned with a selected notch on a timing disk. These notches cause electrical pulses to be generated as they pass the pole pieces of a magnet. Since each pulse represents a certain character, this disk is called the *character pulse generator.* Its function is to identify the row of a character. A second disk with a single notch is provided to identify the first character on the roll.

5-6. The print roll is driven directly by a motor. Speeds up to 2000 rpm have been attained; however, 1000 rpm is a more common operating speed. It is not always possible to print a line per revolution of the print wheel due to delays in feeding paper, but speeds of 1800 lines per minute have been attained.

5-7. *Electrical circuits.* The electrical circuits of major importance in the printing cycle are listed and discussed below. These circuits are shown in block form in figure 5-20.

- Synchronizing pulse generator.
- Character generator.
- Electronic distributor.
- Storage matrix.
- Hammer drivers.

5-8. The function of the *synchronizing pulse generator* is to produce pulses that are synchronized to the rows of characters on the print roll and identify these characters. The index pulse identifies the No. 1 character on the print roll by resetting a counter in the electronic distributor to zero.

5-9. The *character generator* simply produces a pulse stream at the rate of one pulse per character row on the print roll. When the No. 1 (first) character row on the print roll passes under the print hammers, the first character pulse after the index pulse is generated; the No. 2 row is under the print hammer at the generation of character pulse 2; row 3 matches pulse 3, etc., through pulse 165. This series of character pulses is called the *character pulse stream*. The character pulse sequence is repeated as the print roll makes each revolution.

5-10. The *electronic distributor* accomplishes several functions. Its primary function during the print cycle is to channel each individual pulse of the pulse stream into separate lines that connect to the storage matrix in accordance with the number of the pulse (with reference to the index pulse). Also, it is the circuit that recognizes the index pulse and is reset by it.

5-11. Upon identifying the first pulse, the distributor does two things: (1) it selects a line to the storage matrix that corresponds to row 1 on the print roll, and (2) it sends an electric pulse through this line to the storage matrix. When the second pulse is detected, the distributor selects a second line and pulses it—the No. 3 pulse is channeled through a third line. Thus, each character pulse is sent to the storage matrix on a separate line, and each of these lines is pulsed as a corresponding character row passes under the print hammers. Each line, therefore, represents a separate character.

5-12. After all characters in a line are printed (end of print cycle), the paper must be moved up one space for the next line of print. It is then ready to begin another print cycle. An additional function of the electronic distributor is to produce the pulse that initates the paper-feed mechanism.

5-13. It is important for you to remember the following: The electronic distributor receives the character pulse stream; it uses these pulses to energize specific lines in accordance with the character row count; then, at the end of the print cycle, produces a pulse that triggers the paper-feed mechanism.

5-14. The *storage matrix* serves as a data storage buffer and hammer trigger pulse generator. Data from an external register is stored in this matrix at desired locations. For example, let us assume that AN is the first word in the line to be printed; also, that row 1 on the print roll is all N's and row 2 is all A's. We use this example to point out that the characters need not be in alphabetical and/or numerical order.

5-15. For the letter A, the computer would write a binary 1 in the storage matrix at the intersection of the column 1 line and row 2. For the letter N, it would write a binary 1 at the intersection of the column 2 line and row 1. Nothing would be written in any of the rows for column 3 since it is to be a space. All of the other words would be written in the storage matrix in this manner.

5-16. The matrix enters into the printing process as follows: When the No. 1 row of characters (N's) is about to pass under the print hammers, the first pulse of the print cycle (T1) is received from the signal distributor on line 1. The T1 pulse simultaneously reads all N characters for all words of the line being printed. It is the function of the storage matrix during T1 pulse time to produce an output hammer trigger pulse for all columns that have a binary 1 written into the N's row. In our example, the N (column 2) of the word "AN," therefore, would be written during the T1 pulse. The A (column 1) will be printed during the second pulse (T2), along with all other A's that appear in the line. Column 3 has no data written in it since it is to be a space; therefore, no print hammer trigger pulse is generated from the storage matrix for this column. As the print cycle progresses, all characters and spaces are printed in this manner until the print cycle is completed.

5-17. The pulses from the storage matrix are not of the proper power and shape to drive the hammers; therefore, they are shaped and amplified in the print *hammer driver circuits.* A power driver and shaper is provided for each hammer.

5-18. *Mechanical action of printing.* The method of printing discussed here is referred to in some textbooks as printing "on-the-fly," because the print roll does not stop as the print hammer strikes. The hammer must strike quickly (with a short dwell time) so that the character is not smudged by the raised character on the print wheel as it passes.

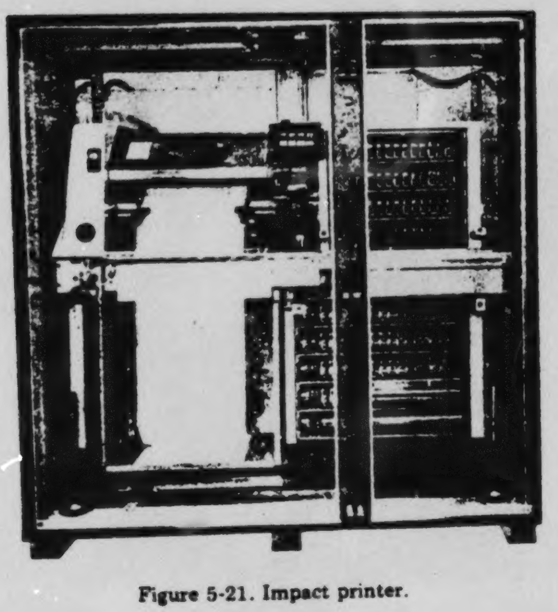


Figure 5-21. Impact printer.

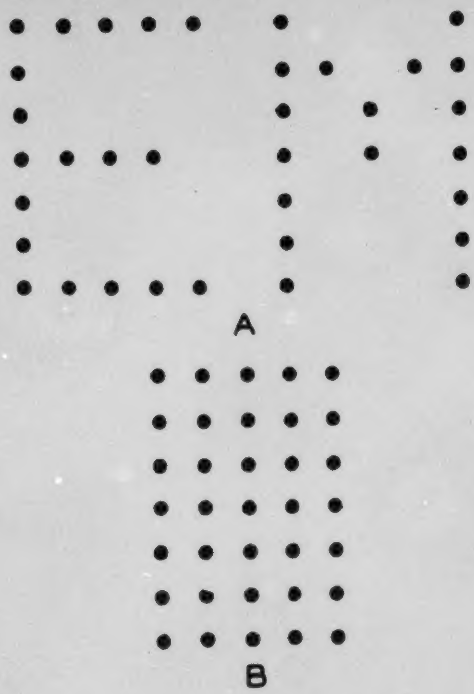


Figure 5-22. Dot matrix character format.

5-19. Adjustments are built into each hammer circuit for individual adjustment of the darkness of the printed character. All hammers are adjusted for the same force of print. Also, there is a line adjustment for setting the darkness of the print for the full line.

5-20. A high-speed line printer with the cabinet doors removed is shown in figure 5-21. The paper is stored in the bin below the print roll. During printing, the paper passes through the printer and onto a shelf behind the machine. The modules that make up part of the electrical circuits, including the matrix, are shown at the right of the figure.

5-21. Electrographic Printer. In some ways, the electrographic printer is similar to the usual typewriter or printer, but in other respects it is quite different. Its description here emphasizes how it differs.

5-22. *Character format.* The electrographic printer is sometimes referred to as the wire matrix burn printer, because it burns the imprint of a wire matrix character onto a specially prepared paper. Upon close

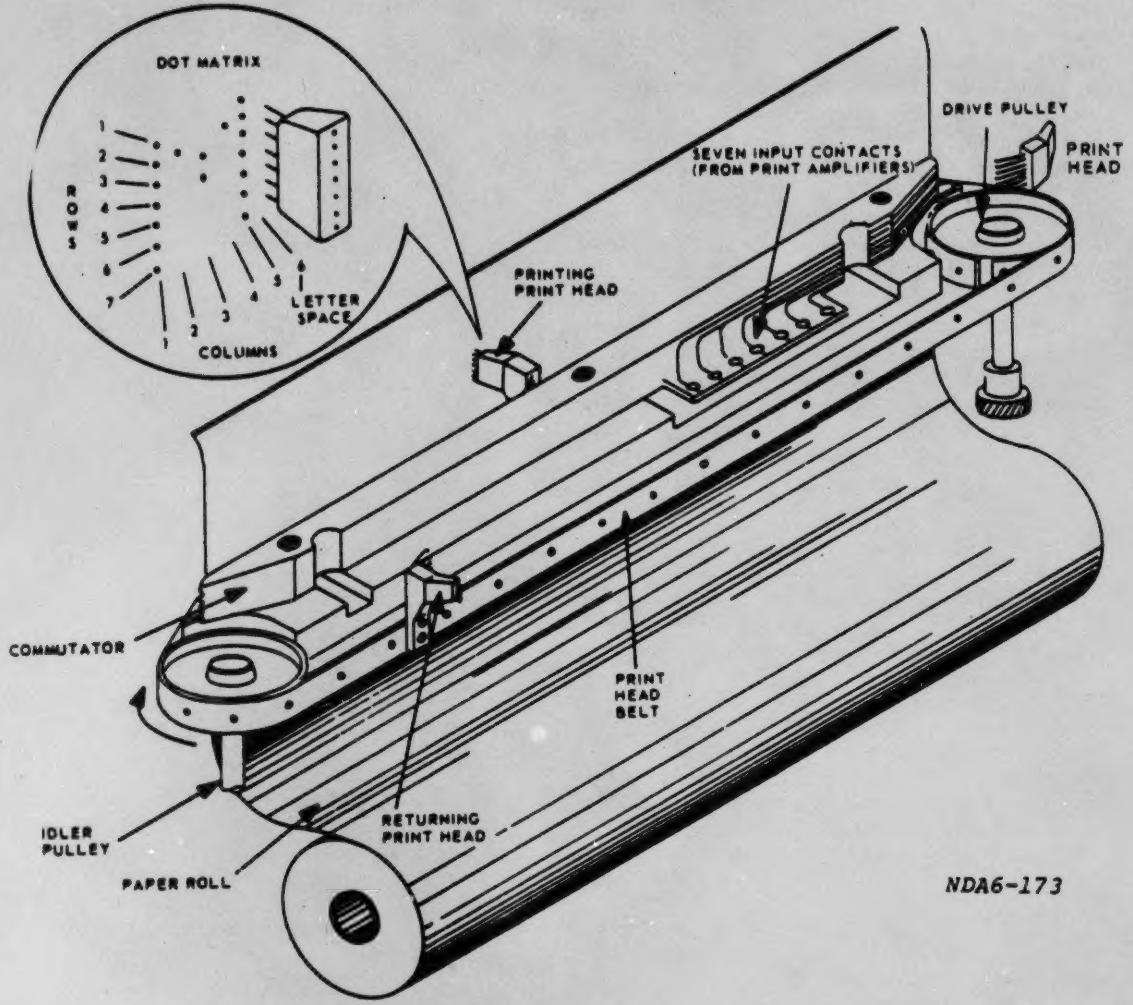

DOT MATRIX
ROWS
1
2
3
4
5
6
7
COLUMNS
1
2
3
4
5
6
LETTER SPACE
PRINTING PRINT HEAD
SEVEN INPUT CONTACTS (FROM PRINT AMPLIFIERS)
DRIVE PULLEY
PRINT HEAD
COMMUTATOR
PRINT HEAD BELT
IDLER PULLEY
RETURNING PRINT HEAD
PAPER ROLL
NDA6-173

Figure 5-23. Electrographic printer.

inspection, the printed character looks like a group of dots. Figure 5-22,A, shows an example of two such characters, an E and M. Of course, the actual print is smaller than shown in the figure. If every dot of the print code was printed, it would appear as shown in figure 5-22,B. Looking at figure 5-22,B, observe that the dots are arranged in five columns and seven rows to form a 5 by 7 matrix. By proper selection of dots in this matrix, any desired character can be printed.

5-23. *Print heads.* Messages are printed a character at a time on continuously moving electrosensitive paper by three continuously moving print heads, shown in figure 5-23. The print heads are transported on a belt which is skewed (slanted) at an angle so that the print head rises as it travels across the page. The rate of rise of the print head is the same as that of the paper. These actions result in parallel, horizontal lines of print. As one print head completes a line, the following head on the belt is drawn into position to start the next line. Since there are three print heads on the belt, a given head prints every third line.

5-24. Each print head, as shown in figure 5-24, contains seven styluses arranged vertically. These styluses make electrical contact to the print amplifiers through "fingers" which slide along a commutator. The dots which make up a character are formed by burning away a thin white coating on the surface of the electrosensitive paper, exposing a black underlayer. The styluses print the selected dots a column at a time. As the print head moves across the page, additional columns are printed until a total of five columns has been used to complete a character. A one-column letter space is left between characters (see insert on fig. 5-23).

6. Magnetic Drums

6-1. A magnetic drum storage system provides both an input and an output device feature. A magnetic drum can have binary data written onto its drum surface and read from the same surface. In today's computer system, magnetic drums provide two primary functions: auxiliary storage and buffer storage.

6-2. **Auxiliary Storage Device.** When used as auxiliary storage, the drum stores information that is needed only periodically; therefore, it is not economical to use storage space in main memory to store the information. Also, the information is of such a nature that the medium access time of the drum does not slow down the use of the data in a processing problem.

6-3. **Buffer Storage Device.** When used as buffer storage, the drum is effectively a time buffer between slow-speed equipment and a high-speed computer. As a time buffer, the drum receives data from slow-speed equipment and transfers this data to the higher speed computer. This transfer also works in reverse. That is, transfers are made from a high-speed computer system to the slow-speed equipment through the drum. Thus, data processed by the computer is stored on the drum at a rapid rate and is delivered to the output system at a slower rate. This permits the slow-speed equipment and the high-speed equipment to function at their own rates independently. Since the drum system performs no computations, data enters and leaves the drum without alteration.

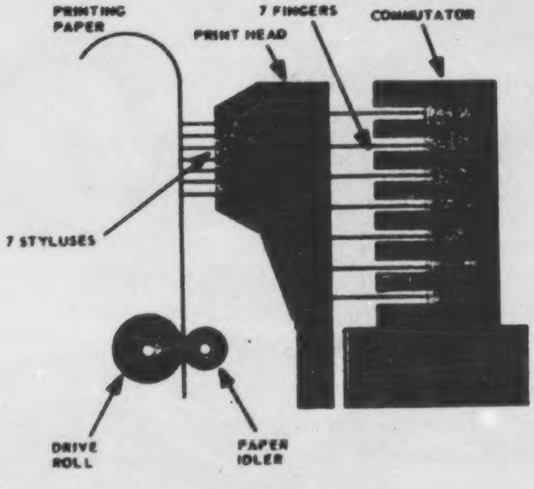


Figure 5-24. Print head.

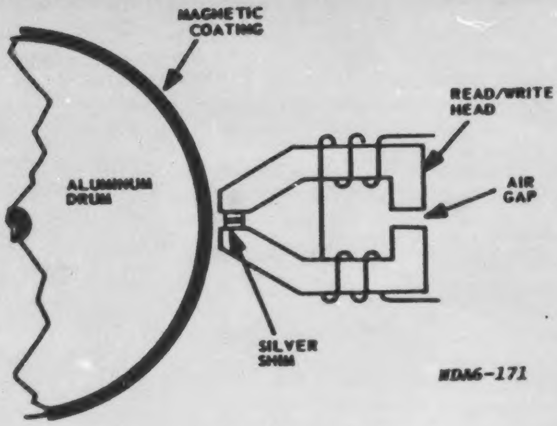


Figure 5-25. Read/write head.

6-4. **Physical Characteristics.** The drum is a metal cylinder of nonmagnetic metal. Aluminum is widely used, because it is paramagnetic and dissipates heat readily. A thin layer of ferromagnetic material is applied to the surface of the basic cylinder to provide the recording surface. The most common method of applying the surface is electroplating.

6-5. The magnetic drum may be mounted either vertically or horizontally on a shaft through its center. The shaft is either belt-driven from a drive motor or the drive motor is connected directly to the shaft.

6-6. *Read/write heads.* The actual reading from or writing on a drum is done through the use of one or more electromagnets, called read/write heads. The same head can be used to read and write. In some cases, two sets of heads are used, one for reading and another for writing.

6-7. A typical read/write head is composed of a ferromagnetic alloy core which is usually made up in two sections with an airgap at each end; see figure 5-25. Each core is wound with several turns of fine wire which is pulsed when reading or writing. These cores must have a *low retentivity* (ability of a material to hold its magnetism); if not, the head would continue to magnetize the drum after write current is removed. The cores are mounted with one airgap placed close to the magnetic surface of the drum. When the core is pulsed to write a binary digit, this gap permits a flux leakage that magnetizes the surface of the drum. In some cases, a paramagnetic

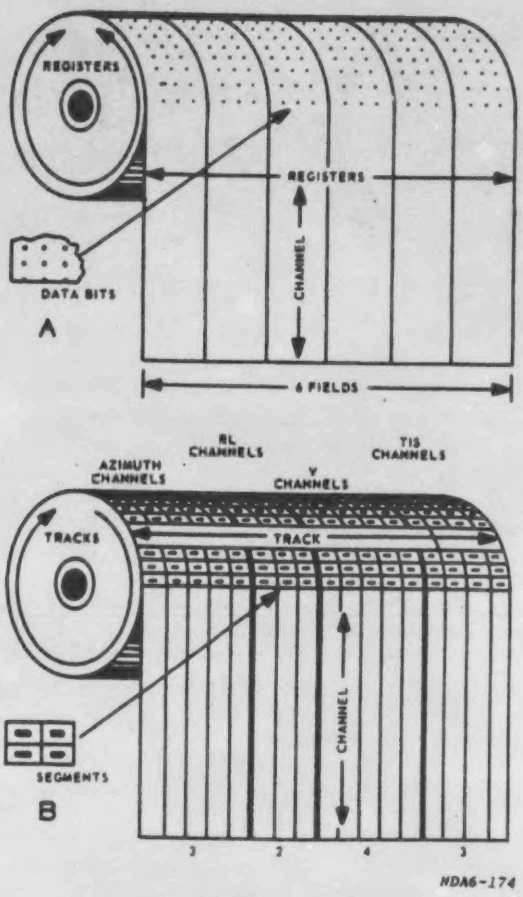

REGISTERS
REGISTERS
DATA BITS
CHANNEL
A
6 FIELDS
RL CHANNELS
TIS CHANNELS
AZIMUTH CHANNELS
V CHANNELS
TRACKS
TRACK
CHANNEL
SEGMENTS
B
3
2
4
3
NDA6-174

Figure 5-26. Drum surface layout.

shim—usually silver—is placed between the poles in the airgap. This increases the amount of flux leakage and increases the induced flux density on the surface of the drum. The airgap at the opposite end of the core prevents saturation of the core during a write or readout pulse.

6-8. Notice that the heads in figure 5-25 do not touch the recording surface. This is because the friction generated by direct contact would wear away the surface and reduce the life of the drum. Direct contact would allow a binary digit to be stored with a minimum write current, would provide a higher amplitude read pulse, and would reduce the area required to store a binary bit. But since the advantages are offset by the disadvantages, the heads are normally brought as close as possible to the drum without touching.

6-9. Heads are usually adjusted to within 0.001 to 0.002 inches of the drum surface. The adjustment is made with the drum at operating temperature. If the adjustment were made with the drum cold, the drum could expand as it heated and cause the heads to drag on the drum.

6-10. *Drum surface layout.* Consider the surface of the drum as a rectangle. In other words, visualize it as if the surface were unwrapped from the cylinder and laid out flat. This visualization is illustrated in figure 5-26, A. You would find that the area passing under a drum head is called a *channel.* Also, a row of data bits grouped into areas in which a single drum word is written in parallel is called a *register.* Finally, you would find a set of registers that extend in columns around the drum is called a *field.* A drum is not necessarily divided into specific field separations as shown in figure 5-26, A. The fields are actually *interleaved* around the drum surface.

6-11. Figure 5-26, B, shows the layout of a drum surface with different terminology applied. Each bit position is called a *segment.* A row of segments across the drum is called a *track*, and, as in part A of the figure, the area that passes under one head is called a *channel.* In addition, this drum groups the channels

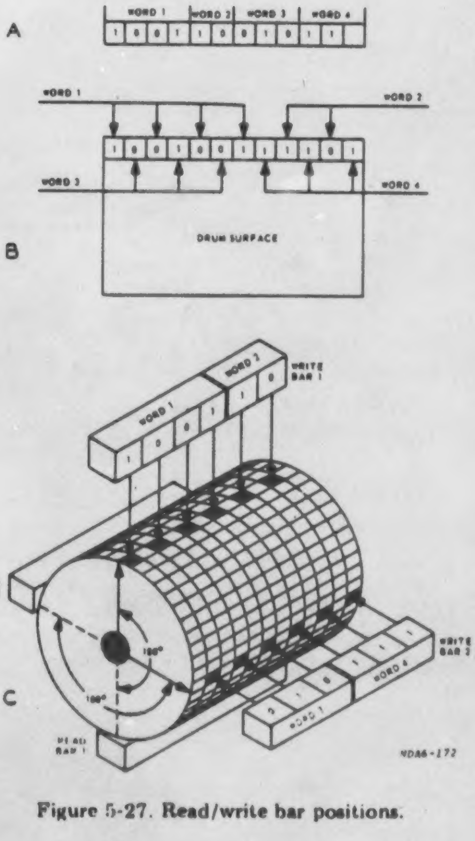

A
WORD 1
WORD 2
WORD 3
WORD 4
1
0
0
1
1
0
0
1
0
1
1
WORD 1
WORD 2
1
0
0
1
0
0
1
1
1
1
0
1
WORD 3
WORD 4
DRUM SURFACE
B
WORD 1
WORD 2
1
0
0
1
1
0
WRITE BAR 1
READ BAR 2
180°
180°
C
WRITE BAR 2
WORD 4
WORD 3
READ BAR 1
NDA6-172

Figure 5-27. Read/write bar positions.

together and titles them according to the type of information written into that group. For example, the azimuth information contains 12 bits of information; thus, the 12 channels that store azimuth information are called the *azimuth channels*. The drum surface layouts shown in the figure are for drums which are written into and read out of in parallel.

6-12. *Mounting bars*. Mounting bars are devices used for mounting read/write heads over the drum surface. To understand how heads are physically arranged on a mounting bar, you must first understand how words are arranged on the drum. Figure 5-27, A, shows four words, labeled W1, W2, W3, and W4. Note that the words are sitting in a 12-bit register. The drum, shown in part C of the figure, has 12 channels; thus, if the segments lined up in a row across the drum's surface are considered a register, the drum represents a 12-bit register. It is natural to assume that the bits would be transferred to the drum in the same order as they appear in the register. However, this is not the case, since the drum-channels are close together on the drum surface and the heads are so large in comparison that adjacent channel heads cannot be located side by side. This leads to various arrangements of heads to permit the four words to be written in parallel and to be read out in parallel. Parts B and C of figure 5-27 show one method of arranging heads. It assumes that the heads can be placed close enough together on a bar to write on every other channel.

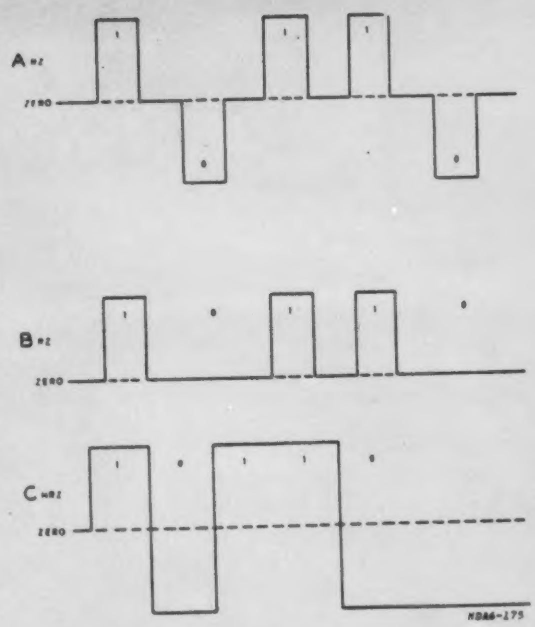


Figure 5-28. RZ and NRZ write voltage.

6-13. With this arrangement, bit 1 of word 1 is placed on channel 1, bit 2 on channel 3, bit 3 on channel 5, etc. This is called *interleaving*. The four words are written on the drum at the same time, but notice that

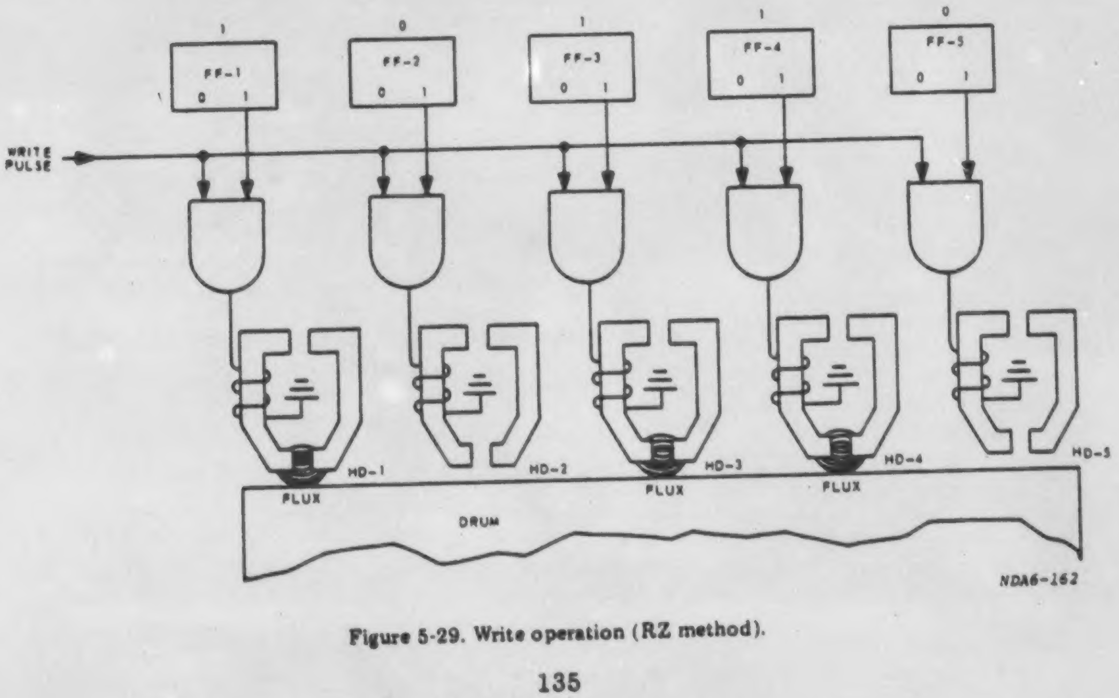


Figure 5-29. Write operation (RZ method).

they do not appear in a straight line across the drum surface, as shown in part B of the figure. Instead, words 3 and 4 are displaced 90° from words 1 and 2. If the write heads are displaced 90° from one another and it is desired to read all four words off simultaneously, the drum must have two mounting bars of read heads. Part C of the figure illustrates a drum with two write bars and two read bars. The words are being written on the drum surface interleaved. When the drum rotates 180°, the bits placed on the drum by write bar 1 pass under read bar 1, and the bits placed on the drum by write bar 2 pass under read bar 2, allowing all four words to be read off simultaneously.

6-14. **Writing.** There are two methods in which the binary digits (ONE or ZERO) are written on the drum surface. They are the nonreturn-to-zero (NRZ) method and the return-to-zero (RZ) methods. Figure 5-28 shows representative waveforms for these two methods. The same binary configuration of 10110 is used for all three waveforms.

6-15. *Return-to-zero method.* The RZ method may use a write pulse for each digit being recorded; that is, the drum surface is magnetized in one direction for ZERO and in the opposite direction for a ONE. This is shown in part A of figure 5-28. From this, you can see that a write pulse must be sent to the drum head for either a ONE or a ZERO. The RZ method shown in part B of the figure is different in that a write pulse is necessary only when a ONE is to be written. When using this RZ method, the drum must be erased before new information is written; whereas with the method shown in part A of the figure, it is not necessary to erase prior to writing new information.

6-16. *Nonreturn-to-zero method.* The NRZ method changes flux only when data being written changes from ONE to ZERO or ZERO to ONE. Part C of figure 5-28 shows the binary word 10110 in the NRZ method. Note that flux remains constant for the two adjacent ONE bits. If this configuration had two adjacent ZERO bits, the flux would remain in the opposite state.

6-17. Each method has its own advantages and disadvantages. For instance, the NRZ method requires more complex circuitry to convert the recorded voltages to a usable form but has the advantage of a greater bit density on the drum system; that is, more bits can be recorded on the drum surface, since no allowance has to be made for spaces between bits as is required in the RZ method. Since elaborate circuitry is normally very expensive, most drum systems operate on the RZ method.

6-18. Look at figure 5-29 and assume that this drum is using the RZ method. Therefore, a write pulse is sent whenever a ONE is to be recorded. Assuming that flip-flops 1, 3, and 4 contain ONEs that are to be written, you can see that the ONE-side output of the flip-flops is fed to the AND-gates. Since flip-flops 1, 3, and 4 are in the ONE state, three of the five gates will have one of the required input levels present. A write pulse is now sent to each of the five gates, fully conditioning three of them. The output from the three conditioned gates causes current to flow through the coils wound around heads 1, 3, and 4. This current sets up a magnetic field across the head gap and magnetizes a spot on the drum. Each magnetized spot represents a binary ONE bit of the word. Note that the flip-flops containing ZEROs did not condition their respective gates and the spot that heads 2 and 5 pass over is not magnetized.

6-19. **Reading.** Readouts are obtained by using either a read head or a combination read/write head. If a single head is used for both operations, it contains two coils wrapped around the same head—one for reading and one for writing.

6-20. The read heads detect magnetized spots or segments on the drum surface. The rotation of the drum surface past the read heads induces a voltage into the windings for each magnetized segment that passes under the heads. The induced voltage is then amplified and shaped to produce a pulse at the read amplifier output.

6-21. If the RZ method which uses a write pulse for both a ONE and a ZERO is employed, a voltage is induced into the read heads for either a ONE or a ZERO. The direction of the flux lines from the magnetized segments determines direction of current flow through the read head coils. This direction determines if the segment represented a ONE or a ZERO.

6-22. When the other RZ method is used, only ONEs are written on the drum. Therefore, a voltage is induced in the read heads ONLY when the segment contains a ONE. Since ZEROs are not written, the absence of a voltage indicates a ZERO.

6-23. **Addressing and Timing.** The method by which information is written into or read from a storage system usually falls into one of two categories: *random* or *sequential* addressing. Random addressing means that the storage system provides access to any desired address without regard to order. Sequential addressing means following in

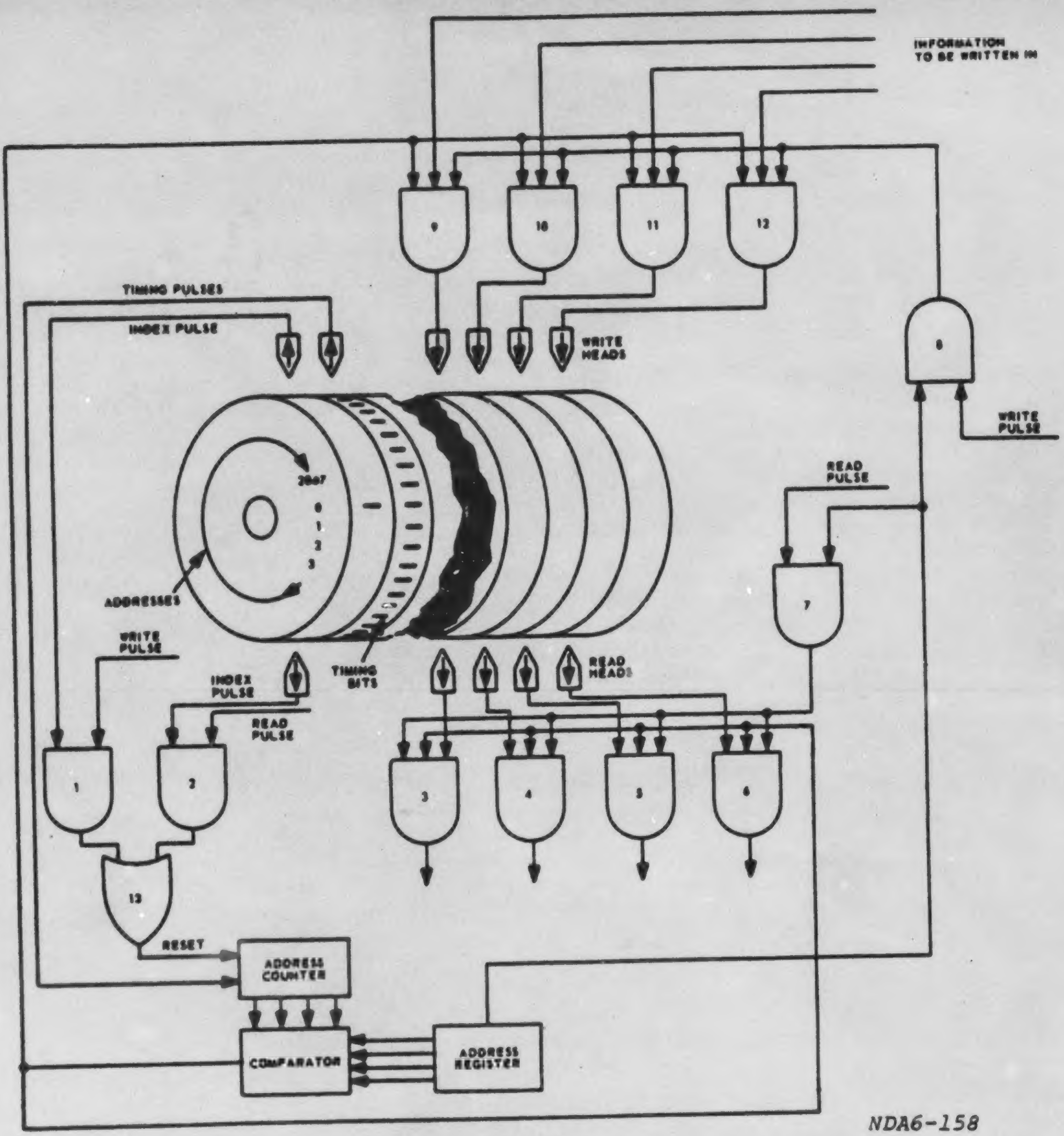

INFORMATION TO BE WRITTEN IN
TIMING PULSES
INDEX PULSE
WRITE HEADS
WRITE PULSE
READ PULSE
2047
0
1
2
3
ADDRESSES
TIMING BITS
READ HEADS
WRITE PULSE
INDEX PULSE
READ PULSE
RESET
ADDRESS COUNTER
COMPARATOR
ADDRESS REGISTER
1
2
3
4
5
6
7
8
9
10
11
12
13
NDA6-158

Figure 5-30. Random addressing.

order; that is, you start reading or writing from a given place or "index point." This reading or writing then proceeds through all locations, in order, back to the index point where the cycle starts again. This type addressing is also called *cyclic* addressing.

6-24. As you can see, a drum system can be addressed either at random or sequentially. Figure 5-30 is a typical random addressed drum. When this method of addressing is used, it is necessary to have an index channel and a timing channel.

6-25. The index channel, as shown in figure 5-30, provides a reset pulse to the address counter, insuring the same starting location for every rotation of the drum. The index pulse may be etched on permanently or written on in the same manner as the information channels.

6-26. There is one timing bit for each address, or location, on the drum. The timing channel bits apply stepping pulses to the address counter. In this manner, the counter determines which address is passing under the read or write heads at any time.

6-27. Let us look at figure 5-30 and see how an address is selected. You can see that the drum contains 2048 addresses or locations (0 through 2047). You can also see that the index bit corresponds to address zero (0) and that there is a timing bit for each address.

6-28. Assume that you wish to write information into a given address. The desired address is placed into the address register. Four of its outputs are sent to the comparator and the fifth is sent to condition AND-gates 7 and 8. This fifth output partially determines whether the read or write heads are selected. Let us now initiate a write pulse since we wish to write information. The presence of the write pulse partially conditions AND-gate 1 and fully conditions AND-gate 8 which, in turn, partially conditions AND-gates 9 through 12.

6-29. We now have to locate the desired address. When the index bit passes under the index channel head, it induces a voltage into the head. This voltage is fed to AND-gate 1, fully conditioning it. The output of AND-gate 1 is sent to OR-gate 13 and on to the address counter where it resets the counter to ZERO. Since there is a timing bit corresponding to each address, a voltage is induced into the timing channel head as each address passes under it. This voltage is sent to the address counter and used as a stepping pulse; that is, as each timing bit passes under the timing channel head, the address counter is stepped up one. This signifies which address is under the heads. When the address counter reaches the same count as that contained in the address register, an output is produced by the comparator. This output is sent to AND-gates 3 through 6 and 9 through 12. You can see that AND-gates 3 through 6 are not conditioned, since we are not reading and the output from AND-gate 7 is not present. Since

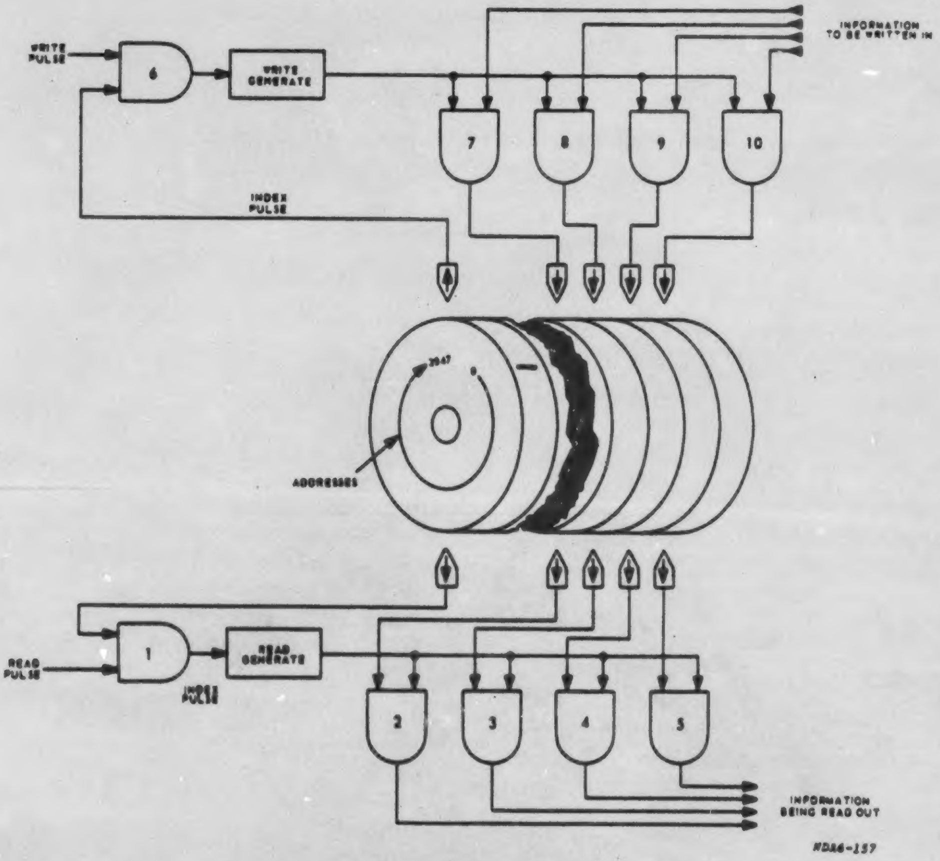


Figure 5-31. Sequential addressing.

AND-gates 9 through 12 have the information levels present and the write heads have been selected, the output from the comparator, which says the desired location is under the write head, fully conditions them and the information is then placed in the desired location.

6-30. Now that you see how random addressing works during the writing process, let us look at the reading process and see how it is done. Notice in figure 5-30 that the read heads are mounted 180° away from the write heads. This, then, necessitates an additional index channel head to insure that the reading process starts at address zero, as in the writing process. If dual read-write heads were used, an additional index channel head would not be required.

6-31. The reading process is identical to that of writing, except that AND-gates 2 through 7 are conditioned by the presence of the read pulse, and the AND-gates conditioned during writing are deconditioned by the absence of the write pulse.

6-32. Figure 5-31 shows how sequential or cyclic reading and writing is done. Notice that in this method a timing channel is not needed, since the complete drum is written on or read from before either operation is terminated.

6-33. Let us see how a write operation is accomplished (see fig. 5-31). We have information to be written present at the input of AND-gates 7 through 10. A write pulse is now initiated to bring up one leg of AND-gate 6. When the index bit passes under the index channel head, it induces a voltage into the head. This voltage is fed to AND-gate 6, fully conditioning it. The output from AND-gate 6 triggers the write generator which, in turn, conditions AND-gates 7 through 10 for the duration of one drum rotation. The information is then written on the drum.

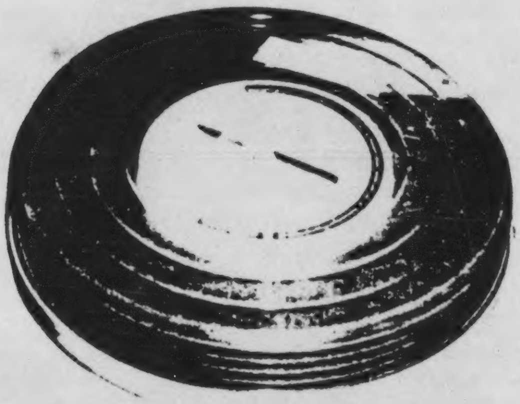


Figure 5-32. Disk pack.

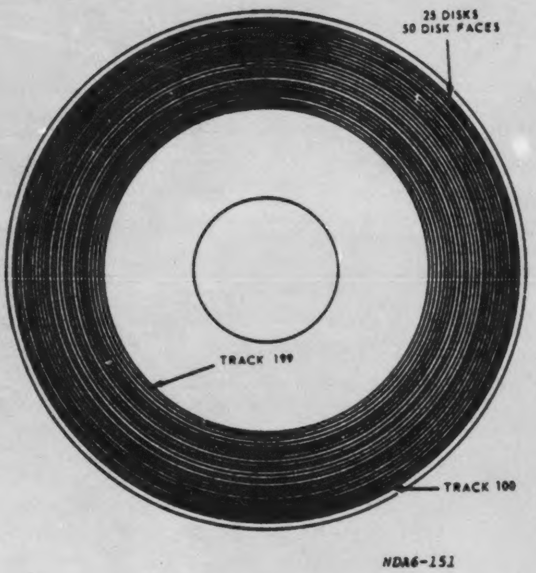


Figure 5-33. Magnetic disk.

6-34. The read operation is identical to the write except that AND-gates 1 through 5 are conditioned by initiating the read pulse. The output from AND-gate 1 triggers the read generator. The read generator's output conditions AND-gates 2 through 5. When the read heads sense data on the drum, the data passes through gates 2 through 5.

7. Magnetic Disks

7-1. Magnetic disk storage devices are similar in basic principles of operation to magnetic tapes and drums. One feature of the magnetic disk which has led to its popularity is that it becomes a simple matter to add additional disk packs to a system when additional storage space is required. Another feature of the disk pack is that they can be stored for future use once they are written on.

7-2. **Physical Appearance.** One type of disk system arrangement has the disks stacked in a disk pack as illustrated in figure 5-32. There are various types of disk packs in use today. The one we have illustrated is representative of many now in use.

7-3. *Disk pack.* The disk pack in figure 5-32 is composed of several disks mounted on a vertical shaft. Circular protective plates are mounted above the top disk and below the bottom disk to protect the assembly. If there

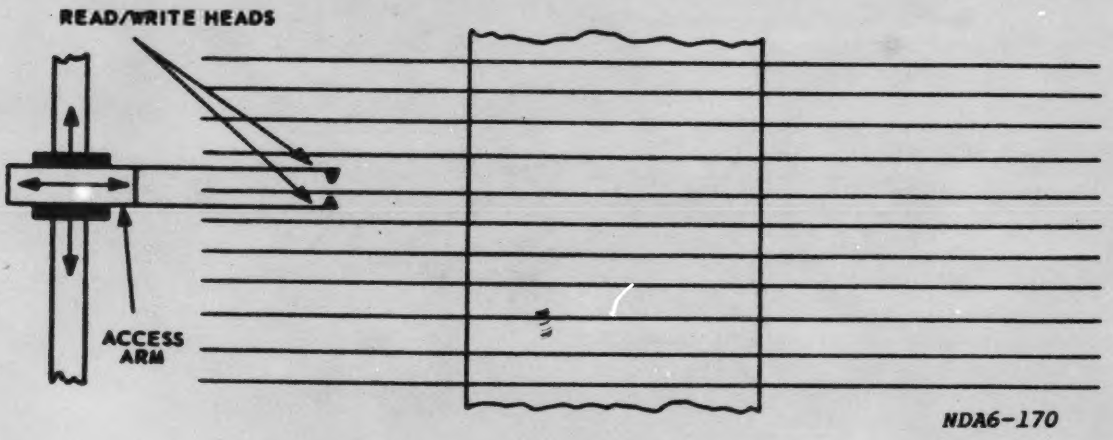


Figure 5-34. Magnetic disk access arm and read/write heads.

were 11 disks in this assembly, only 20 surfaces (top and bottom of a disk) could be written on and read from. This is because a protective plate is used for the upper and lower disk. The disk pack is removable and interchangeable between the modules that house disk packs. A dust cover is provided as an integral part of the removal handle. When inserting a disk pack into a module, the handle locks the disk pack to its spindle which frees the dust cover from the pack. The drawer of the disk pack module must be closed immediately after removing the dust cover in order to prevent dust from getting on the disks.

7-4. *Magnetic disk layout.* A typical disk is illustrated in figure 5-33. Note that this disk contains track numbers 100 through 199. Another disk in the same pack would contain tracks 200 through 299, etc. The actual size of the disks varies from system to system.

7-5. Read/Write Operation. Read/write functions are accomplished by several magnetic heads, each mounted on an arm which is mechanically independent of the disk pack. Figure 5-34 illustrates a set of read/write heads associated with the top and bottom surface of a single disk. Each access arm has access to, and may be directed individually to, any track on its disk. Reading and writing the disk surface is very similar to the reading and writing process on the surface of a magnetic drum.

7-6. The upper read/write head shown in figure 5-34 reads or writes the upper surface of the disk. Access to any of the disks is program controlled. Each of the tracks on the disk contains a circular series of binary information. Access to this information is random by disk and record number. Recall that a record consists of all data treated as an individual unit of information. A record could consist of one machine word or several words. Access to the records is normally accomplished randomly.

7-7. Random Access. Disk storage makes it possible to process information without having the source data in sequence. This is called *random access* processing (as contrasted with *sequential).* For example, if a card or tape record is entered into the system as input, the stored record desired can be located without having to search through all disks. To illustrate further, assume that 10 magnetic disks are used for storing all material (inventory records) by stock number. All stock numbers starting with 0 are placed on one disk, those starting with 1 on another disk, those starting with 2 on a third disk, and so on through stock numbers starting with 9, which are placed on the tenth disk. If an issue card with a stock number starting with a 4 is fed into the system, the disk which has all stock numbers starting with 4 is selected and spun around until the particular stock number which the machine is looking for is reached.

7-8. Random access processing has a decided advantage over sequential processing if master files have to be updated on a continuous basis. Continuous processing usually results in a small percentage of the master records being affected. In sequential processing, each master record must be read and written for each processing cycle, even though only a few records may have to be updated. In random access processing, only those master records affected by transactions need be read and written, thus saving considerable reading and writing time.

7-9. Storage Basket Disk Arrangement. Another disk arrangement has the disks mounted side by side in a storage basket, with each disk in a vertical position. When information is to be written on or read from a disk, a transfer arm selects the proper disk and transports it to the read/write station. A read/write head, mounted on a transport arm, reads or writes as the disk revolves horizontally on a turntable. Reading or writing is performed only on the upper side while the disk is at the read/write station. To read from or write on the reverse side, the disk must be returned to the storage basket and reselected.

CHAPTER 6

Computer Power Supplies

ELECTRONIC computer power supplies are the units that supply the necessary voltage, power, and current for the operation of computers and peripheral equipment. Whether you are working on a solid-state or electron-tube computer, you will find that its reliable operation depends upon a well-regulated source of power.

2. You will receive ample training on the computer's power system during the job-knowledge portion of your on-the-job training. Therefore, we do not intend to expound on any specific computer power system in this chapter. Our objective is to review the operation of the solid-state circuits associated with converting AC power to DC power. After this review, we will present and discuss the operation of a typical computer solid-state power supply. Also, since power supply troubles can cause serious computer malfunctions, we will present typical trouble symptoms and testing procedures associated with DC power supplies.

1. Obtaining DC Power for Computer Circuits

1-1. Think back to your training in basic electronics and recall that there are various methods of generating a DC voltage. For an electronic computer, however, most of the DC voltages are obtained by rectifying AC. Thus, the AC to DC power supply is, and will likely remain, the principal source of DC power for computers.

1-2. **AC to DC Power Supplies.** Let's quickly review the basic units of the AC to DC power supply. In figure 6-1, we have conveniently divided a DC power supply into four basic units: (1) AC source, (2) transformer unit, (3) rectifier unit, and (4) regulator unit.

1-3. Depending on the particular computer, the AC source may be the output of the motor-generator set or 60-Hz commercial power. A DC power supply does not always have an input transformer; the input could be taken directly from the AC source. An obvious advantage of an input transformer is that the AC source can be isolated from the load and either stepped up or down within the transformer secondary.

1-4. You recall that rectification is the process of converting AC to pulsating DC. Therefore, within the rectifier unit there must be some type of rectifying device. Because the output of the rectifier is pulsating DC, you will normally find some type of filtering within this unit. Recall that filtering is the process of removing the pulses (ripple) from the DC output.

1-5. Although the unregulated output of a power supply may be satisfactory for some applications, a regulated output is necessary for the majority of computer circuits. The function of the regulating unit is to prevent output voltage variations.

1-6. **Practical Considerations of Computer Power Supplies.** Although the principles of rectification, filtering, and regulation are relatively simple, many factors deserve consideration regarding the type of circuits and components that go into a DC power supply. The complexity of the power supply depends upon the load requirements, i.e., the demands of the circuits which it is designed to support. Some of the factors to be considered in designing a computer power supply are listed below.

1-7. What voltages must be supplied for the load? This brings up the need for either an input transformer or an output voltage divider or both. How many amperes or milliamperes will the load draw? The rectifying device and other components within the power supply will have to be of the correct type and value to support the required current.

1-8. What percent of ripple and voltage variation can be tolerated in the output? Four factors that affect the quality of the DC output are: the AC input, type of

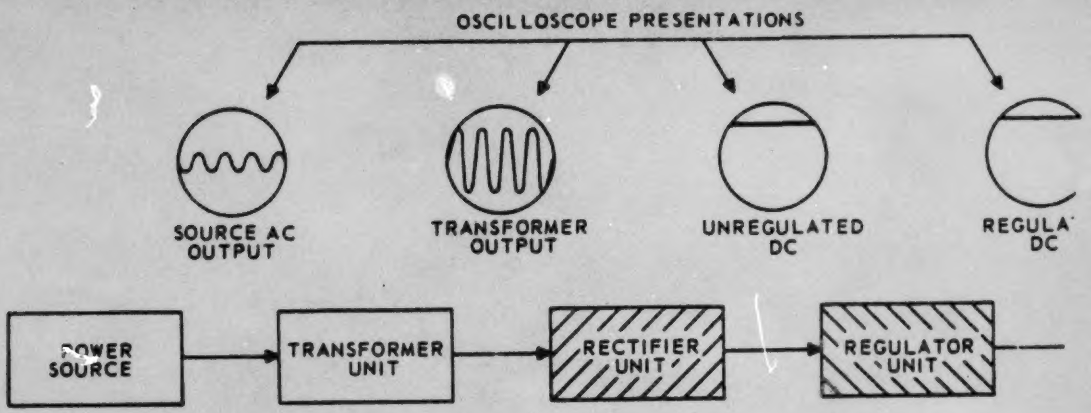

OSCILLOSCOPE PRESENTATIONS
SOURCE AC OUTPUT
TRANSFORMER OUTPUT
UNREGULATED DC
REGULA DC
POWER SOURCE
TRANSFORMER UNIT
RECTIFIER UNIT
REGULATOR UNIT

Figure 6-1. Basic units of a power supply.

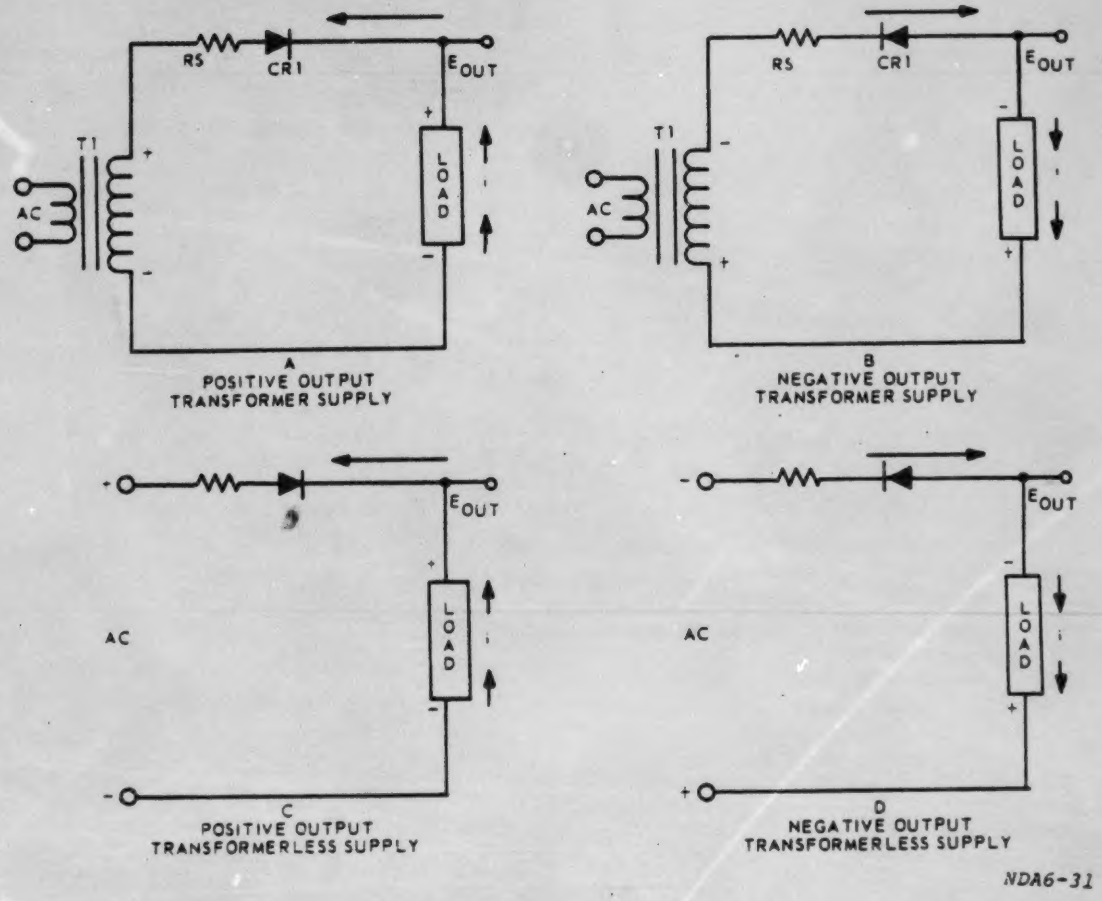

RS
CR1
EOUT
T1
AC
+
-
LOAD
i
A
POSITIVE OUTPUT TRANSFORMER SUPPLY
B
NEGATIVE OUTPUT TRANSFORMER SUPPLY
C
POSITIVE OUTPUT TRANSFORMERLESS SUPPLY
D
NEGATIVE OUTPUT TRANSFORMERLESS SUPPLY
NDA6-31

Figure 6-2. Basic half-wave rectifier circuits.

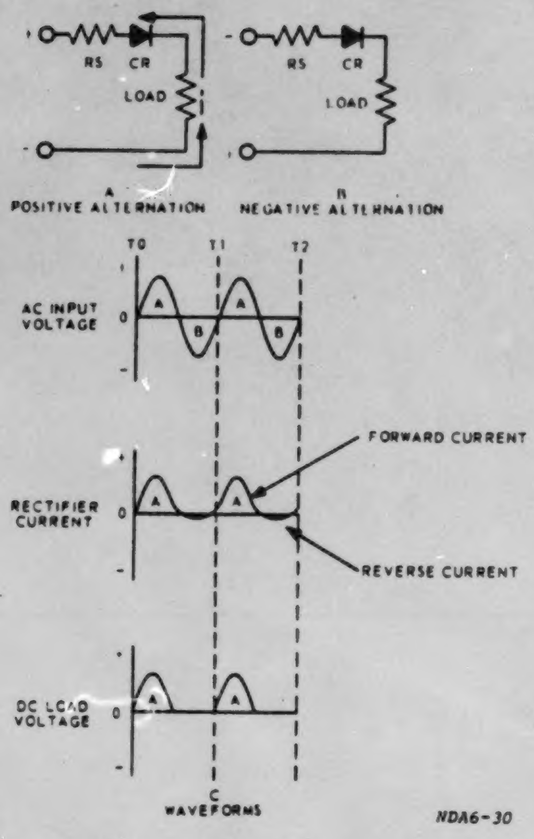


Figure 6-3. Half-wave operation and waveforms.

rectification, type of filtering, and the load requirements. Recall from your previous studies of power supplies that half-wave rectifiers require better low-frequency filtering and better regulation than full-wave rectifiers. Remember that we can reduce the output ripple by either using large inductors in series with the load or large capacitors in parallel with the load. Also, recall that the choke-input filter gives a better regulated output than the capacitor-input filter. Of course, if the load is constant and draws little current, the problems of ripple and regulation are slight. On the other hand, varying loads are troublesome to the extent that they cause fluctuating demands on the power supply. When the load draws more current, the ripple tends to increase and DC output voltage tends to decrease.

1-9. From this discussion, you can see that the types of circuits within a particular computer will dictate the required output from the power supplies. The functions of rectification, filtering, and regulation will be covered further to help you comprehend the operation of the power supplies within your computer's power system.

2. Rectifying AC

2-1. The rectifying circuits that use solid-state devices (crystal or metallic rectifiers) are basically the same as those that use electron tubes. An obvious distinction, however, is the absence of filament or heater circuits within solid-state rectifiers. The simplest type of rectifier is the half-wave rectifier.

2-2. **Half-Wave Rectifier.** The name "half-wave" refers to the operation of this circuit. It operates either on the positive or negative alternation of the applied AC to provide one pulsation of current in the output. This type of rectifier circuit may be used to convert single-phase or polyphase (more than one phase) AC to DC.

2-3. The single-phase half-wave rectifier consists of a rectifying device in series with the alternating source and the load. The manner in which the rectifying device is connected within the circuit will determine whether forward conduction occurs on the positive or negative alternation of the applied AC. This type of rectifier is commonly found in electronic business machines, relay supplies, and test equipment.

2-4. Let's take a look at some basic single-phase half-wave rectifiers. Parts A and B of figure 6-2 illustrate two variations of a half-wave rectifier utilizing an input transformer. The two circuit variations shown in parts C and D operate directly from the AC source. The position of the rectifier diode CR1 in the circuits directs the current flow as indicated by the arrows adjacent to the load. Note that each circuit contains resistor RS in series with the rectifier. This resistor, called the *surge resistor*, limits the peak current through the rectifier to a safe value; its use, as well as its value, depends on circuit design. Normally, it is not used if there is a sufficient

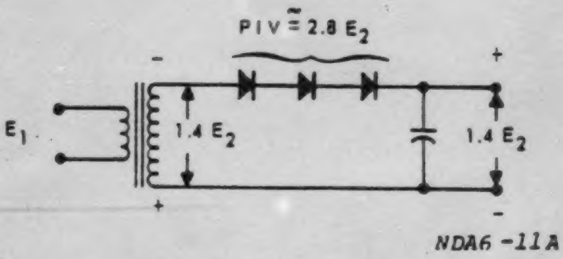


Figure 6-4. Half-wave rectifiers in series.

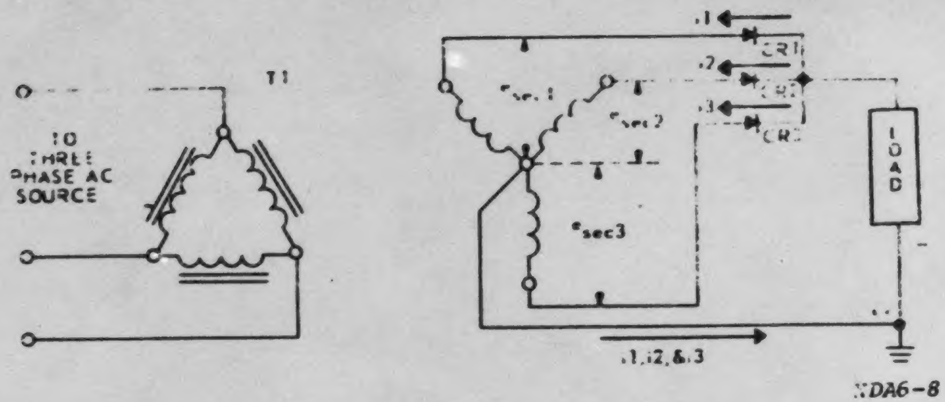


Figure 6-5. Basic three-phase half-wave rectifiers.

amount of resistance within the input source or if a choke-input filter is used as the filtering device.

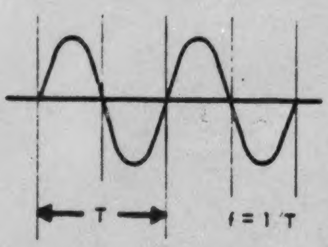
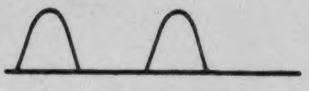
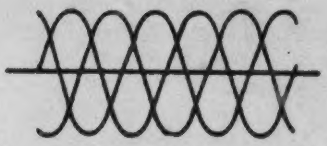
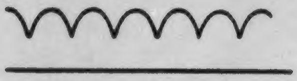
2-5. Operation of the single-phase half-wave rectifier can be understood from the simplified circuits shown in parts A and B of figure 6-3 and the waveforms shown in part C. We will assume that the AC voltage applied to the input terminals during the initial half-cycle has the polarity indicated in part A. Electrons flow in the direction indicated by the arrows. By following these arrows, you can see that current flow is from the lower (negative) input terminal, through the load, through rectifier CR, through surge-resistor RS, and to the upper (positive) input terminal. In other words, when the rectifier diode conducts, electrons pass through the load to develop a corresponding output voltage pulse, as indicated in part C of the figure.

2-6. During the next half-cycle, the polarity of the applied AC is negative. Except for possibly a very small value of reverse current, the rectifier does not conduct, and the small current which flows can be neglected. Normally, the reverse resistance of the rectifier is extremely high as compared with the circuit load resistance; therefore, during the second half-cycle, very little voltage is developed across the comparatively low-load resistance. You can see this in part B of the figure.

2-7. What do you think would happen if the reverse resistance of the rectifier was not high enough to prevent current flow on alternate half-cycles? The rectifier could not convert the AC to DC if this condition existed. Do you remember what PIV represents? Peak inverse voltage (PIV) is the maximum instantaneous voltage in the direction opposite to that in which the rectifier is designed to pass current. Recall that if this voltage is exceeded, the reverse resistance of the rectifier will break down and current will flow within the circuit. How can we prevent the PIV from being exceeded? Couldn't the reverse resistance—therefore, the PIV—of the rectifying device be increased by stacking (placing in series) more than one rectifier? You can see this in figure 6-4. The circuit illustrated shows three rectifiers in series, which triples the reverse resistance. The use of the capacitor input filter shown in the circuit is the reason the rectifiers had to be stacked. Notice that the secondary transformer voltage and the voltage across the capacitor are series-aiding. This is the voltage that will be dropped across the rectifiers in the reverse directions; therefore, the PIV of this circuit is equal to twice the input voltage. What would have happened if only one rectifier had been used in this same circuit?

2-8. The simple half-wave rectifier we have presented does not have high output current capabilities, but you can see in figure 6-4 that it does offer a high-voltage output. The peak secondary voltage is felt at the output terminals. However, this high-voltage output is vulnerable to loading (changes in current requirements within the load). For example, if the load draws more current, the amplitude of the output ripple increases; consequently, the amplitude of the DC output voltage decreases.

2-9. Using a three-phase input greatly increases the quality of the output from a half-wave rectifier. A basic three-phase half-wave rectifier is illustrated in figure 6-5. If you trace out any one phase, you will see the circuit is that of a single-phase half-wave rectifier. Therefore, a three-phase half-wave is

	AC INPUT	UNFILTERED DC OUTPUT	RIPPLE	
			%	FREQ.
1Ø			121	f
3Ø			18	3f

NDA6-14

Figure 6-6. Waveform comparison of single- and three-phase half-wave rectifiers.

nothing more than a combination of three single-phase units, each operating from one phase of a three-phase source. The circuit illustrated uses a three-phase transformer to step up the alternating source voltage to a high value in the wye-connected secondaries (a wye-connected secondary is also referred to as a star-connected). The primary windings of the transformer are shown delta-connected.

2-10. Looking at figure 6-5, you can see that each rectifier is connected to a high-voltage secondary winding, and the load is connected between the junction point of the wye-connected secondary and the common connection of the three rectifiers. Current flow is indicated by the arrows. The voltages induced in the transformer secondary windings differ in phase by 120° . This means that each rectifier section conducts for 120° of the complete input cycle; therefore, each rectifier contributes one-third of the current supplied to the load. The circuit we have illustrated delivers a positive DC output to the load. What changes would be necessary to get a negative DC output from this same circuit? If you answered, "Change the ground to the opposite output terminal," you would be correct; however, the common practice is to keep the junction of the wye-connected secondaries at ground potential and reverse the connections to the rectifiers.

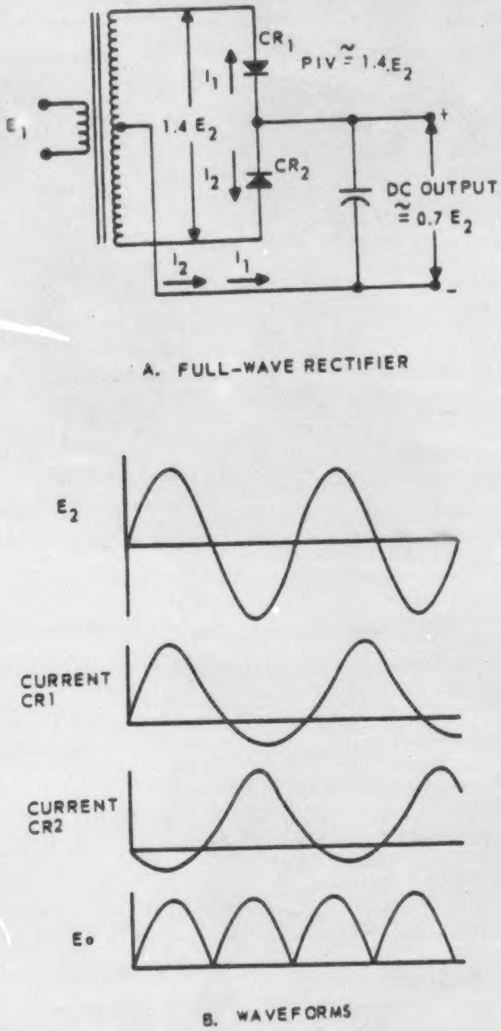
2-11. You can see in figure 6-6 why a three-phase input to a half-wave rectifier greatly increases the quality of the output. Notice that the unfiltered output waveform clearly shows why the amplitude of the ripple is greatly reduced when a three-phase unit is employed. Note the marked decrease in the percent of ripple. Observe also that the ripple frequency is tripled, which makes filtering easier and improves the regulation of the output.

2-12. We have spoken only of a single- and three-phase unit, but a polyphase half-wave rectifier may consist of any number of phases. It stands to reason that the greater the number of phases, the less the percent of ripple and the better the regulation. Regardless of the number of phases, the operation of the polyphase unit is fundamentally that of single-phase units feeding a common load in time sequence.

2-13. In summary, there are many ways of increasing the output capabilities of the half-wave rectifier. Applications within computer systems of today must take into consideration the cost, weight, size, and efficiency of the power supplies, as well as the load requirements. The inclusion of series-limiting resistors to reduce surge currents decreases efficiency. Using choke-input filters will add weight and size to the unit. Increasing the number of phases and rectifiers may be too costly. In other words, half-wave rectification is not likely to be as feasible as full-wave rectification for applications that require high-power output.

2-14. **Full-Wave Rectifiers.** The name "full-wave" identifies the operation of this type of rectifier circuit. It uses both the positive and negative alternations of the applied AC, and it provides two pulsations of current in the output. Because this type of circuit uses a greater percentage of the input cycle, the output ripple amplitude is easier to filter and voltage regulation is easier to attain.

2-15. One way of obtaining full-wave rectification is by using a center-tapped transformer (also called a conventional rectifier), as illustrated in part A of figure 6-7. The circuit arrangement shown is typical of many low-voltage supplies. As shown by the waveforms in part B of the figure, rectifier CR1 conducts I_1 and CR2 conducts I_2 on alternate half-cycles of the input. This results in rectified current being supplied to the filter capacitor twice each cycle. Actually, this arrangement can be thought of as two half-wave rectifiers operating 180° out of phase. It yields a higher ripple frequency (twice the input frequency), which is desirable for filtering. Although the output

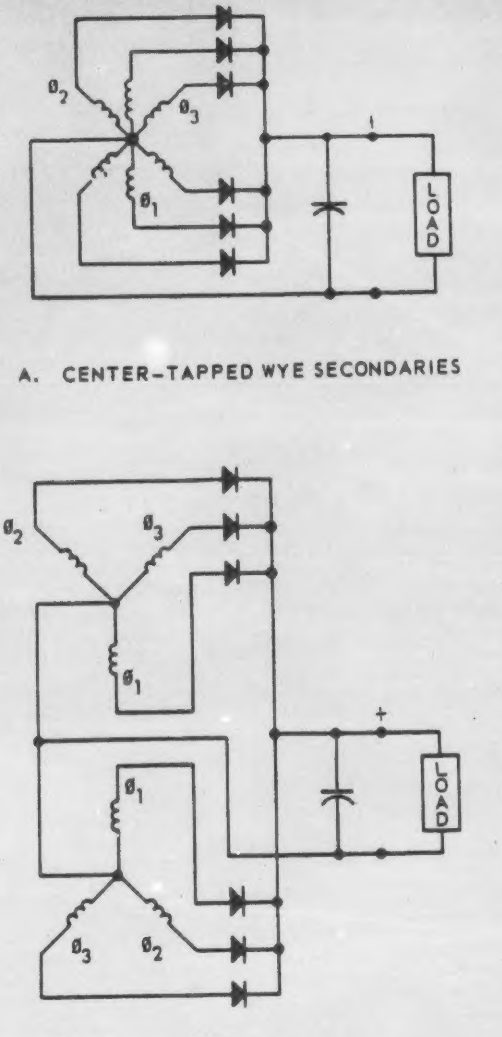


A. FULL-WAVE RECTIFIER

B. WAVEFORMS

NDA6-5

Figure 6-7. Basic full-wave single-phase rectifier.



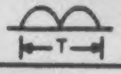
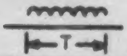
A. CENTER-TAPPED WYE SECONDARIES

B. SEPARATE Y SECONDARIES
(PHASES ARE IN EFFECT CENTER-TAPPED)

NDA6-13

Figure 6-8. Basic full-wave three-phase rectifier.

INPUT FREQUENCY = f = 1 T

AC INPUT	UNFILTERED DC OUTPUT	RIPPLE	
		%	FREQ.
1ø		48	2f
3ø		4	6f

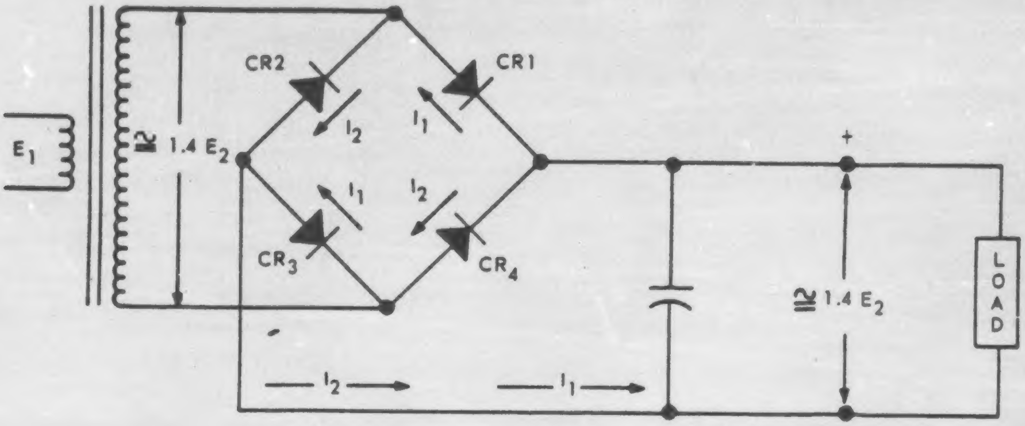
NDA6-11

Figure 6-9. Waveform comparison of single- and three-phase full-wave rectifiers.

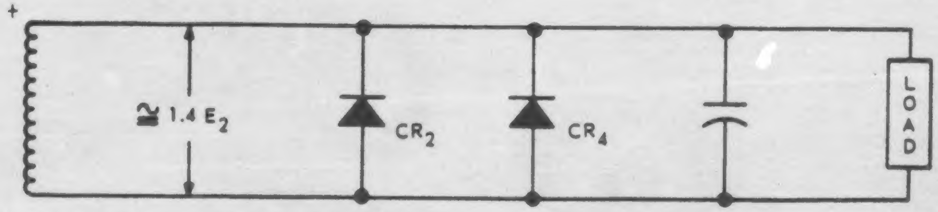
current is doubled, the DC output voltage is only half the secondary peak voltage.

2-16. As with half-wave rectifiers, we can improve the DC output of the full-wave center-tapped rectifier by using a polyphase input. Two three-phase circuits are illustrated in figure 6-8. Notice that any one phase is identical to the single-phase circuit. The improvement realized by using a three-phase input can be seen in figure 6-9. These improvements are similar to those noted for the three-phase half-wave rectifier, i.e., a decrease in the percent of ripple and an increase in the ripple frequency which facilitates filtering and improves regulation.

2-17. For loads that require high voltage and high current, a full-wave bridge rectifier is most often used. This type of rectifier gives full-wave rectification and applies the full secondary peak voltage to the output. The main advantage of this circuit is that the secondary of the transformer does not have to be center-tapped; therefore, the output voltage is twice as great as it would be if the same transformer was used in the center-tap full-wave circuit. Another desirable feature is that the bridge rectifier can be placed directly



A. BRIDGE CIRCUIT



B. PIV AND OUTPUT VOLTAGE REPRESENTATION

NDA6-12

Figure 6-10. Full-wave bridge rectifier, single-phase.

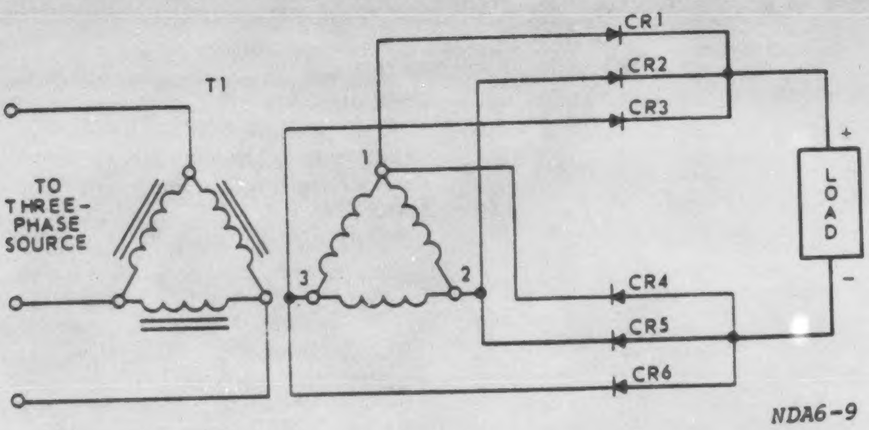


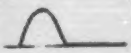
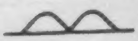
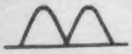
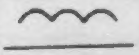
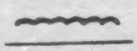
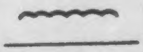
Figure 6-11. Full-wave bridge rectifier, three-phase.

across a single-phase or three-phase line, because it does not require a center-tapped transformer.

2-18. Looking at the full-wave bridge rectifier illustrated in part A of figure 6-10, you can see that the circuit is characterized by having unlike electrodes connected at each end of the input and like electrodes connected at each end of the output. Also, you will note that two rectifiers conduct I_1 during the positive alternation of the secondary, and the other two rectifiers conduct I_2 during the negative alternation. Because both currents, I_1 and I_2, flow in the same direction through the load, the bridge circuit produces full-wave rectification.

2-19. When rectifiers CR1 and CR3 conduct in the forward direction, rectifiers CR2 and CR4 are reverse-biased and in parallel across the transformer secondary. This is shown in part B of figure 6-10, which illustrates that the PIV and the voltage applied across the load are equal to the full secondary peak voltage. When the secondary voltage reverses, CR2 and CR4 will conduct in the forward direction and CR1 and CR3 will be reverse-biased and in parallel across the transformer secondary.

2-20. We can also improve the output of the bridge rectifier by using a three-phase input. A transformer designed for a three-phase bridge rectifier can have its primary and secondary connected wye-wye, delta-wye, wye-delta, or delta-delta. This, plus the fact that the bridge rectifier can be fed directly from a three-phase power line, makes a high degree of flexibility possible. A three-phase full-wave bridge rectifier is illustrated in figure 6-11. Note that the primary and secondary of the input transformer are delta-connected. Each

	SINGLE-PHASE			THREE-PHASE		
		FULL-WAVE			FULL-WAVE	
	HALF-WAVE	CENTER-TAP	BRIDGE	HALF-WAVE	CENTER-TAP	BRIDGE
UNFILTERED DC VOLTAGE OUTPUT WAVEFORM						
% RIPPLE	121	48	48	18	4	4
RIPPLE FREQUENCY	f	2f	2f	3f	6f	6f

NDA6-16

Figure 6-12. Waveform comparison of single- and three-phase rectifiers.

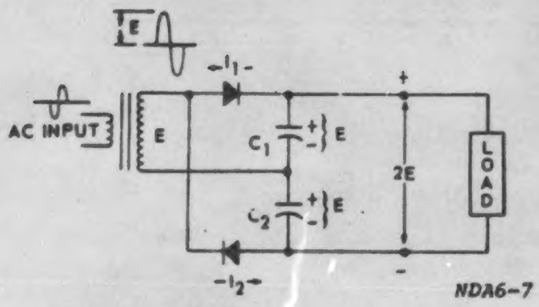


Figure 6-13. Conventional voltage doubler.

secondary winding is connected to the other in proper phase relationship so that the currents through the windings are balanced. The operation of the delta secondary is similar to that of a wye secondary; however, the voltage across an individual delta-connected secondary winding is greater than the voltage across an individual wye connection for equal DC output voltages.

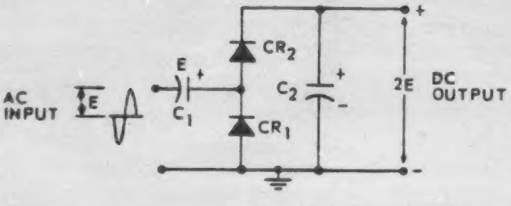
2-21. Each positive and negative peak developed in the three phases produces a current pulse in the output; therefore, at any given instant of time, one rectifier, the load, and a second rectifier are in series across two terminals of the delta-connected secondaries. Each of the six rectifiers conducts for 120° of an input cycle. In figure 6-11, two rectifiers are conducting at any instant of time with conduction occurring in the following order: CR1 and CR6, CR6 and CR2, CR2 and CR4, CR4 and CR3, CR3 and CR5, CR5 and CR1, CR1 and CR6, etc. The improvements realized by using this type of input to the bridge rectifier are similar to those noted for the three-phase half-wave and full-wave center-tapped rectifier circuits i.e., a decrease in the percent of ripple and an increase in the ripple frequency which facilitates filtering and improves regulation.

2-22. When we compare the output of the bridge rectifier with the other types we have discussed, we can see that the bridge rectifier affords the advantages of full-wave rectification at a high DC output. You should refer to figure 6-12 for this comparison.

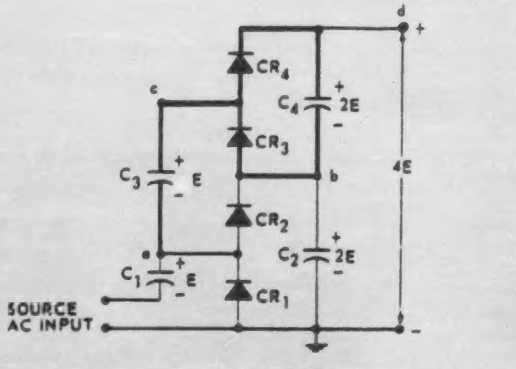
2-23. Voltage Multipliers. We know that one way of obtaining a DC output voltage that is a multiple of the peak AC source voltage is by using a step-up transformer. There are other ways, however, which do not require an increase in the secondary voltage of the transformer. In fact, voltage multiplication can be achieved without a transformer at all. Let's consider two types of rectifying circuits that produce a DC output voltage which is about twice the peak AC input voltage; then we will explain how higher multiples of voltage can be developed from a given source.

2-24. *Conventional voltage doubler.* Referring to figure 6-13, you will find a voltage doubler circuit that is essentially a full-wave rectifier; both the positive and negative alternations feed power to the load. During the positive alternations of the secondary voltage, CR1 conducts I_1 and capacitor C1 charges to the peak secondary voltage E. During the negative alternations of the secondary voltage, CR2 conducts I_2 and C2 also charges to the peak secondary voltage E. Since the polarity of the charge on C2 is series-aiding to the charge on C1, the voltage across the output terminals is twice the value of the peak secondary voltage (2E). Inasmuch as both the charging (via the rectifier) and discharging (via the load) of C1 and C2 constitute the ripple, the ripple frequency of this circuit is twice the frequency of the input AC.

2-25. *Cascade voltage multipliers.* A cascade voltage doubler circuit is illustrated in part A of figure 6-14. We can obtain any desired multiple of voltage by adding sections



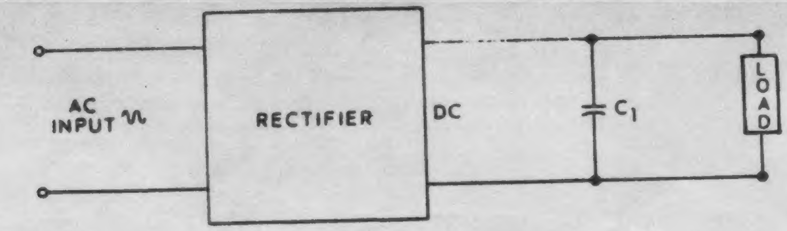
A. DOUBLER



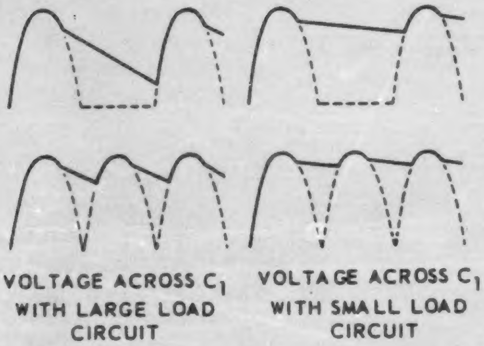
B. QUADRUPLER

NDA6-20

Figure 6-14. Cascade voltage multiplier.



A. RECTIFIER CIRCUIT WITH FILTER CAPACITOR OUTPUT



B. EFFECT OF CAPACITOR ON HALF-WAVE AND FULL-WAVE RECTIFIERS

NDA6-6

Figure 6-15. Capacitor used as a filter.

as illustrated in part B of the figure. After we analyze the operation of the cascade doubler, we can readily explain how higher degrees of multiplication are acquired.

2-26. First, consider the negative alternation of the input. During these alternations, you can see that CR1 keeps C1 charged to E with a polarity as indicated. On the positive alternations, C2 is kept charged by the conduction of CR2. When CR2 conducts in the forward direction, C2 feels the peak AC input voltage which is series-aiding the voltage across C1; therefore, the input peak E plus the voltage E on C1 charges C2 to 2E. Although full-wave rectification occurs, the output capacitor C2 is charged only during the positive half-cycle. Consequently, the ripple frequency of this circuit is that of a half-wave rectifier, equal to the AC input frequency. This means that, like the half-wave rectifier, the cascade doubler is not suited for heavy current loads. Regulation is poor and filtering is difficult.

2-27. For light loads that require a high DC voltage, the cascade circuit is quite popular, since it can be built up to provide the desired level of output. Refer to part B of figure 6-14, and note that the heavily lined circuitry is a replica of the cascade doubler. It is, therefore, possible to increase the DC voltage in multiples of two by adding doubler circuits.

2-28. The lightly lined circuit is identical to that in part A of the figure. The heavily lined circuit differs only in that the voltage across the input capacitor C3 is 2E rather

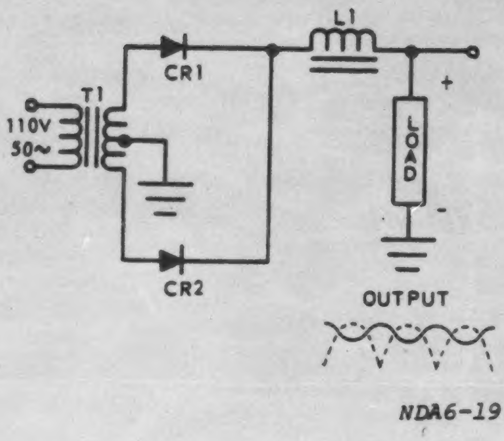


Figure 6-16. Inductor used as a filter.

than E. Capacitor C3 is kept charged to 2E by the action of CR1 and CR3. These two rectifiers effectively place C3 in parallel with C2. Whenever the charge on C3 is less than that of C2, CR3 is forward-biased. So when CR1 becomes forward-biased during the negative half-cycle of the source AC input, C3 is charged by C2. We can see, therefore, that the output capacitor C2 feeds the input capacitor C3. Note that the DC voltage with respect to ground (or common) at point "a" is E; at point "b," it is 2E; and at point "d," it is 4E. Additional sections could give 5E and 6E, and so on.

2-29. The cascade voltage multiplier is particularly useful as a transformerless high-voltage low-current supply. Each rectifier must withstand twice the peak input AC in the reverse direction; therefore, regardless of the amount of multiplication, the maximum PIV on any single rectifier is 2E.

2-30. You have seen that the primary function of a rectifier circuit within an AC to DC power supply is to change AC voltage to DC voltage. However, as we discussed the different types of rectifier circuits, it was pointed out to you that the output voltage was pulsating DC; that is, it has pulses or ripples. We have also pointed out and briefly discussed that removing or reducing the output ripple of the rectifier circuit is accomplished by filters. Now, let's find out about some of the different methods of filtering.

3. Filters

3-1. We know that the variations in the output voltage of a rectifier are called ripple voltage. Do you recall just what this ripple voltage consists of? Let's refresh our memories. Ripple voltage may be thought of as an alternating voltage superimposed upon direct voltage. Actually, the ripple voltage is composed of a fundamental frequency and a number of harmonic frequencies (harmonic frequencies are multiples of the fundamental frequency). The fundamental frequency is equal to the input frequency if the rectifier is half-wave or twice the input frequency if the rectifier is full-wave. For power purposes, this ripple voltage must be removed or reduced to a low percent of the DC output voltage; a

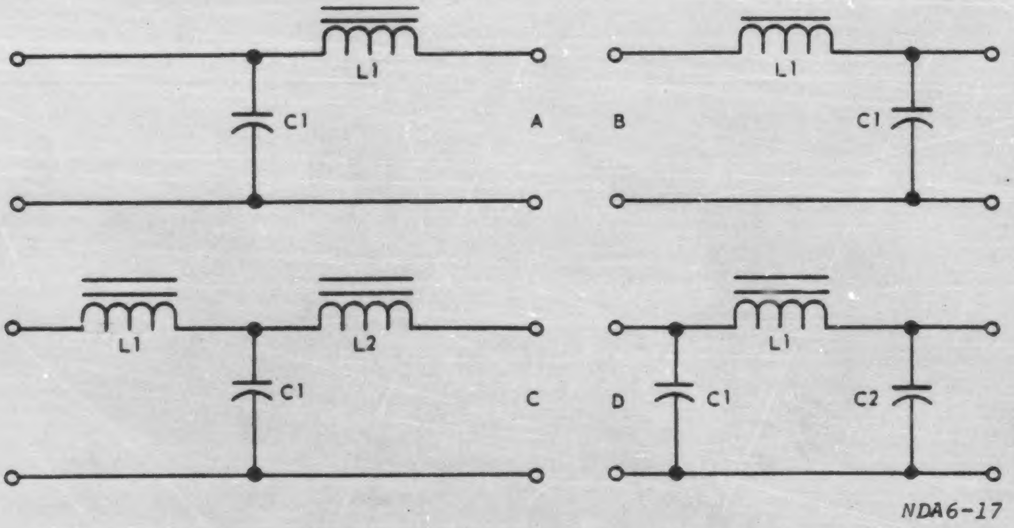


Figure 6-17. LC filter sections.

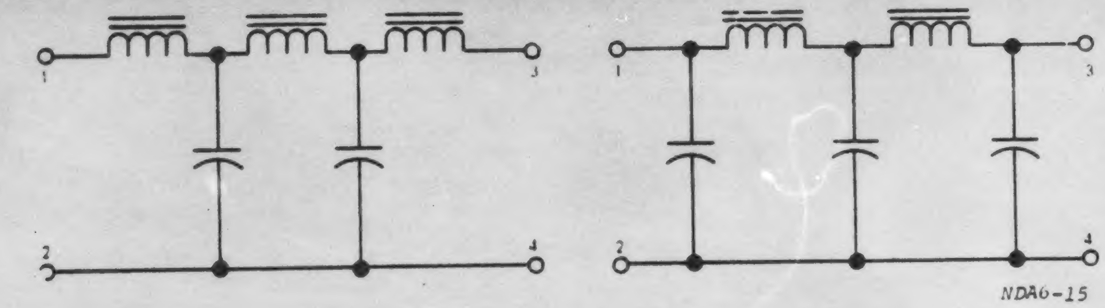


Figure 6-18. Filters of two sections.

device that performs this function is called a filter.

3-2. **Individual Reactance as Filters.** A reactance which opposes a change in voltage (or current) by storing energy and then releasing this energy back to the circuit may be used as a filter.

3-3. **Effect of Capacitance.** Recall that a capacitance opposes a voltage change across its terminals by storing energy in its electrostatic field. Whenever the voltage tends to rise, the capacitor converts this voltage change to stored energy; and when the voltage tends to fall, the capacitor converts its stored energy back to voltage. We have illustrated a capacitor used for filtering the output of a rectifier in part A of figure 6-15. Note that the capacitor C1 is connected in parallel with the load. The value of C1 is such that it offers a very low impedance to the AC ripple frequency and a very high impedance to the DC component. The ripple voltage is therefore bypassed to ground through the low-impedance path, while the DC voltage is applied unchanged to the load. You can see the effect of the capacitor on the output of a half-wave and full-wave rectifier in the waveshapes illustrated in part B of figure 6-15. Dotted lines show the rectifier output; solid lines show the effect of the capacitor. These waveshapes show that the filter capacitor, C1, charges when the rectifier voltage output tends to increase and discharges when the voltage output tends to decrease. In this manner, the voltage across the load is kept fairly constant.

3-4. **Effect of Inductance.** Recall that an inductor opposes a change in current by storing energy in its electromagnetic field whenever the current tends to increase. If the current tends to decrease, it supplies the energy to maintain the flow of current. We have illustrated the use of an inductor for filtering the output of a full-wave rectifier in figure 6-16. Note that the inductor L1 is in series with the load.

3-5. The value of L1 is such that it offers a high impedance to the AC ripple voltage and a low impedance to the DC component. Therefore, for the AC ripple, a very large voltage drop occurs across the inductor and a very small voltage drop across the load. For the DC component, however, a very small voltage drop occurs across the inductor and a very large voltage drop across the load. Note how the ripple has been attenuated in the output voltage shown in the figure.

3-6. **LC Filters.** Capacitors and inductors are combined in various ways to provide more satisfactory filtering than can be obtained with a single capacitor or inductor. Refer to figure 6-17 and you will see several combinations. Because they resemble schematically the letters of the alphabet, part A of the figure is sometimes referred to as an L-type filter section, part B as an inverted L-type, and part C as a T-type filter section. Part D of the figure is called a pi-type filter section, because it resembles schematically the Greek letter pi (π).

3-7. Note that each filter section shown in figure 6-17 is similar in that the inductances are in series and the capacitances in parallel with the load. The inductor must, therefore, offer a very high impedance to the ripple frequency. Since the ripple frequency is comparatively low, the inductances are iron-core coils having large values of inductance (several henries). Because they offer such high impedance to the ripple frequency, these coils are called *chokes.* The capacitors must also be large (several microfarads) to offer very little impedance to the ripple frequency. Because the voltage across the capacitor is DC, electrolytic capacitors are frequently used as filter capacitors. One thing you should remember about electrolytic capacitors is to observe correct polarity when replacing them in a

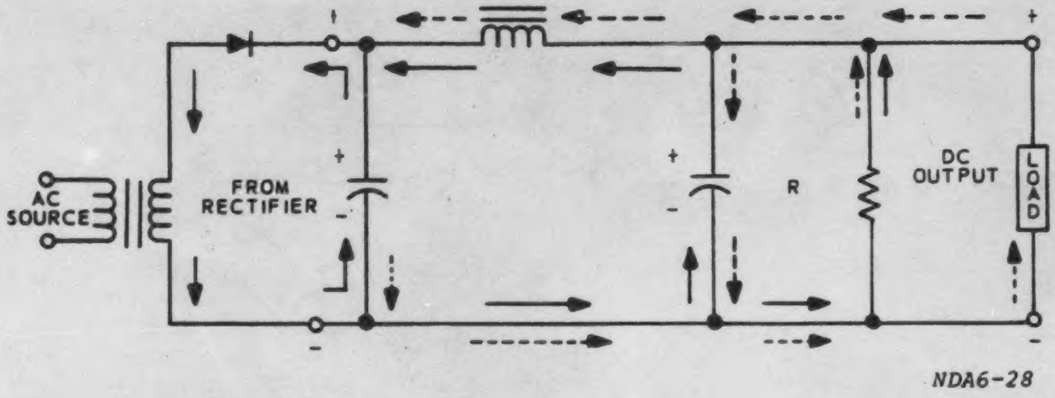


Figure 6-19. Half-wave rectifier with capacitor-input filter.

circuit. More than one section of a given type of filter may be combined to improve the filtering action. Some two-section filters are shown in figure 6-18.

3-8. LC filters are also classified according to the position of the capacitor and inductor. A capacitor-input filter is one in which the capacitor is connected directly across the output terminals of the rectifier. Filter sections A and D of figure 6-17 are examples of capacitor-input filters. A choke-input filter is one in which a choke precedes the filter capacitor. Filter sections B and C of figure 6-17 are examples of choke-input filters.

3-9. **Capacitor-Input Filters.** A capacitor-input filter is characterized by high-output voltage at low-current drain. The most common type of LC filter used with half-wave rectifiers is the capacitor-input pi-type filter that we have illustrated in figure 6-19. When the electrons flow in the path shown by the solid arrows, the capacitors are charged as shown. During the alternation of the input that prevents current flow through the rectifier, the capacitors discharge through the load as shown by the dotted arrows. The extent to which the capacitors discharge depends upon the value of the load. The voltage falls rapidly as the current drain of the load increases.

3-10. An important feature of this filter is the bleeder resistor, which is used chiefly to discharge the capacitors when the equipment is turned off. In figure 6-19, this resistor is represented by R. Normally, this resistor will draw 10 percent or less of the rated current output of the power supply. It could have an adverse effect on power supply operation if it drew more than 10 percent of the current.

3-11. A capacitor-input filter gives poor regulation, because as the load increases, the capacitor is able to discharge more rapidly between cycles. In addition to decreasing the output voltage, this tends to increase the amplitude of the ripple voltage. If a full-wave rectifier is used with this type of filter, there is a slight improvement in the filtering action; however, the voltage regulation is still poor.

3-12. **Choke-Input Filters.** This type of filter is used when we must draw heavy current or when good voltage regulation is demanded. With the same AC input voltage, its output voltage is lower than that of the capacitor-input filter. A choke-input filter requires full-wave rectification in order to keep current supplied to the choke.

3-13. We have illustrated a full-wave rectifier utilizing a choke-input filter in figure 6-20. The pulsating current from the full-wave rectifier flows through the load and the choke. The choke opposes the changes in current and reduces the magnitude of the ripple. The capacitor filters the AC component further. When a small amount of current is drawn, the voltage drops rapidly and then remains fairly constant. This type of filter gives good regulation under changing load conditions or heavy current drain.

3-14. When the current demands of the load vary over a wide range, you will find that a "swinging choke" will be used as the filter. For low values of current, their inductance values are quite high. For high values of current, their inductance values are low since its core has become saturated. The airgap in the swinging choke is much smaller than in the ordinary filter choke; consequently, the total reluctances or opposition to the magnetic lines of force through the core are small. This permits the choke to become saturated for high values of current. Swinging chokes have special applications in circuits where the DC variations are quite large, since it has been found that they give better direct

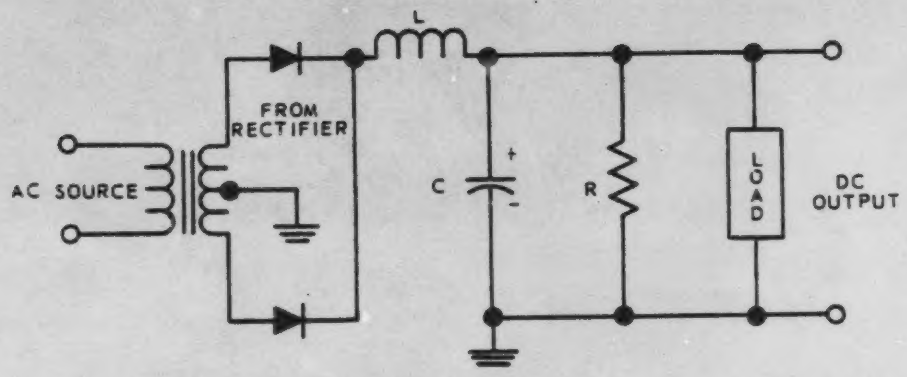


Figure 6-20. Full-wave rectifier with choke-input filter.

voltage regulation with varying amounts of current—i.e., the voltage remains nearly constant even though the amount of current demanded by the load varies over a wide range.

3-15. RC Filters. If a resistor is used in the same location as the inductor in an LC filter, it is called an RC filter. You will see this particular filter being used wherever possible because it is compact in size and low in cost. Two disadvantages of the RC filter are: (1) the resistor offers the same impedance to the DC voltage as to the AC component, which results in a large change in the output voltage when the load current changes; and (2) current flow through the resistor causes power to be dissipated in the form of heat, which results in a loss of power within the filter circuit.

3-16. We have seen that the primary function of the filter is to reduce or eliminate the ripple from the output of the rectifier circuit. Although a certain amount of voltage regulation can be attained with some of these filters, it is not sufficient for the majority of computer circuit applications. Therefore, the computer power supply will require a voltage-regulating circuit as well as the filtering circuit.

4. Regulating DC

4-1. Keeping the output of a DC power supply constant is critically important for the majority of computer circuit applications. Some regulator circuits may be quite simple through the use of a single thermistor or Zener diode. On the other hand, complicated units will use an array of solid-state devices to attain proper regulation for various computer circuit requirements. Although solid-state regulators are functionally similar to electron-tube regulators, they can be utilized in more different ways. The fact that either NPN or PNP transistors can be used permits considerable diversity in design. We will progress from the simple to the more complex regulator circuits by reviewing the operation of representative shunt-type and series-type regulators.

4-2. Shunt Voltage Regulators. This type of regulator consists of a limiting resistor in series with the load and a variable resistance component in parallel (shunt) with the load. You can readily see this in the basic shunt regulator we have illustrated in figure 6-21. The variable resistance component automatically draws more current when the load current decreases and draws less current when the load current increases. Consequently, the current through the series-limiting resistor remains nearly constant, whereas the voltage applied across the variable resistance and the load remains steady even though the load current changes.

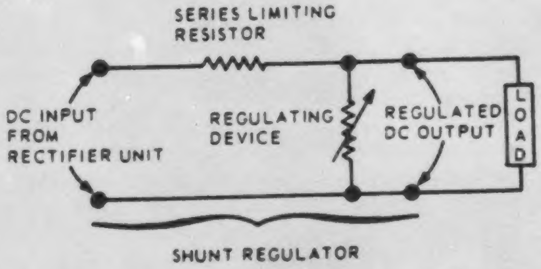


Figure 6-21. Basic shunt regulator.

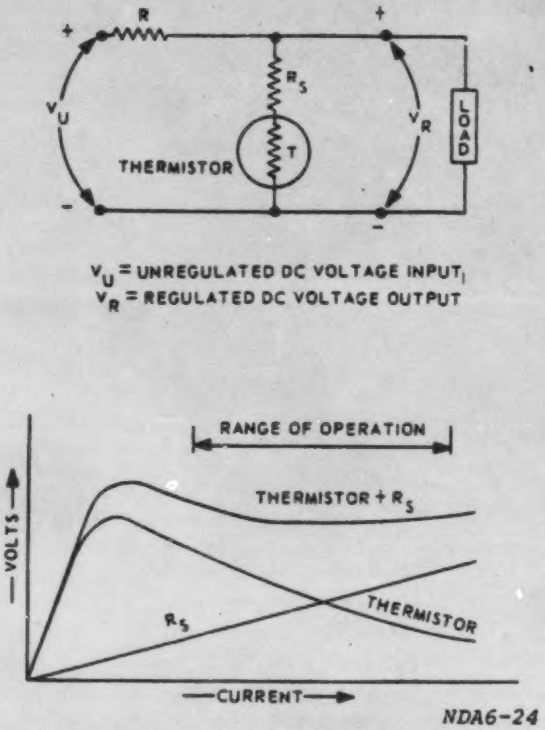


Figure 6-22. Thermistor shunt regulator.

This explains how it regulates under varying load conditions.

4-3. What happens, though, if the input voltage from the rectifier rises or falls? To prevent the output from changing with the input voltage, the variable resistance component must increase or decrease in value so that the entire change appears across the series-limiting resistor. This, of course, means that when the input voltage increases, the variable resistance decreases in value. The result is an increase in current through the variable resistor, causing the voltage drop across the series-limiting resistor to increase. If the decrease in the variable resistance is proper, the product of its adjusted resistance and the increased current will yield the same voltage output as that prior to the input voltage increase. Assuming a decrease in the input voltage, the action of the variable resistor is just the opposite; i.e., it increases in resistance value and less current flows through the series-limiting resistor, causing less voltage drop across it. Again, the voltage drop across the variable resistor (which is the output voltage) is maintained constant. Essentially, then, the shunt regulator circuit functions as a voltage divider that automatically adjusts its ratio to provide the same output voltage under varying input conditions, as well as varying output conditions.

4-4. Now, all we need to find is a device that will automatically adjust its resistance to provide the same output voltage under varying load or input conditions. There are thermistors designed to meet these requirements. A thermistor is a thermally dependent resistor; thus, its name. Its usefulness as a temperature-compensating device stems from the fact that its resistance decreases with heat. In other words, this thermistor has a negative temperature coefficient; i.e., if current through it increases, temperature increases, *but its resistance decreases in a nonlinear manner.* In figure 6-22, you can see the difference in the voltage drop across a thermistor and an ordinary resistor, R_S, with a change in current. By combining the characteristics of both, we can get nearly constant voltage over a desired current range. This is indicated in the figure by the line thermistor + R_S.

4-5. Now let's take a look at a simple shunt regulator circuit that utilizes a thermistor. Refer to figure 6-22 for this observation. In this particular shunt regulator, we are using the combination of resistor R_S and the thermistor as the variable resistance that parallels the load. This circuit is capable of stabilizing the DC output voltage against variations of input voltage and load (current drain) over comparatively wide ranges.

4-6. Another type of shunt regulator utilizes the Zener diode as the regulating device. Recall from your previous studies of the Zener diode that it behaves similar to a regular diode when forward-biased. But let's consider the condition of reverse bias. Only a very small amount of current flows when a normal diode is reverse-biased. What happens

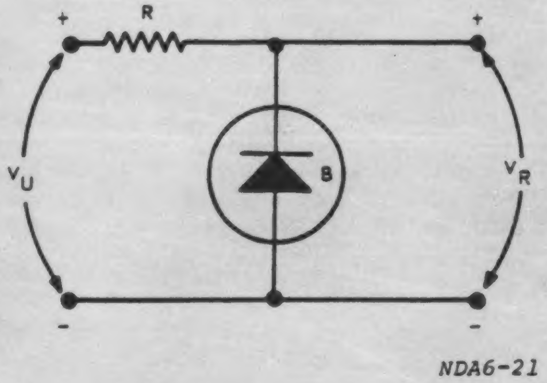


Figure 6-23. Zener diode shunt regulator.

when a Zener is reverse-biased? As the reverse voltage is increased across the Zener, a point is reached where current starts to flow through the Zener. The voltage at which this action occurs is called breakdown or Zener region, and it is at this point that the highback resistance of the Zener vanishes and the current flow is limited only by circuit resistance. The current through the Zener increases proportionately with increasing voltage beyond the breakdown point, *but its junction voltage remains almost constant.* Can you see how this characteristic of the Zener can be used for voltage regulation?

4-7. Figure 6-23 illustrates a Zener diode used as a shunt regulator. This circuit is comparable to a VR (voltage regulator) tube circuit. From our discussion in the preceding paragraph, you know that once the breakdown voltage is reached, the voltage across the Zener is virtually constant and is independent of further changes in current flow. To insure correct breakdown voltage across the diode, series-limiting resistor R is computed for the condition of minimum unregulated input, V_U, and maximum load current. To prevent exceeding the maximum allowable power dissipation of the Zener diode, the computed value of R must also be sufficiently large for the condition of maximum V_U and minimum load current. This latter condition exists when the Zener draws its maximum current. The operation of the circuit is very simple, since the regulated voltage output, V_R, remains practically constant so long as the input and load variations stay within the breakdown region of the Zener diode. Zener diodes are available in numerous voltage and power ratings to meet the different circuit design requirements.

4-8. If the Zener diode regulator is not satisfactory, we can use an arrangement like that shown in figure 6-24. Here, we see an NPN transistor connected across the output to regulate the voltage. The emitter is kept at a constant potential by the Zener diode. Therefore, any voltage variation appearing across the output terminal is detected by the transistor's base as an input signal, and the current through the transistor changes to regulate V_R.

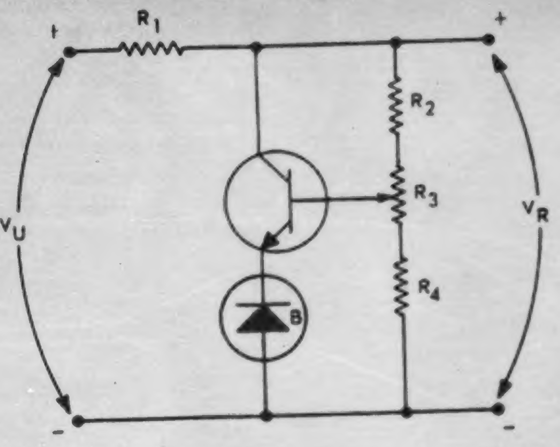


Figure 6-24. NPN transistor shunt regulator.

4-9. An advantage of this circuit is that the output voltage can be adjusted to a desired fixed level. This feature makes it possible to set V_R at a higher or lower value to compensate for aging or different load requirements. Resistors R2 and R4 establish the range of voltage for bias that can be tapped off of R3. The bias determines the transistor's quiescent (operating) point and its DC resistance. In other words, by changing the bias setting, you change the transistor's resistance so that a greater or lesser amount of the input voltage appears across the output terminals. For instance, to increase the DC output voltage, the movable contact to R3 must be moved downward. This will decrease the forward bias on the NPN transistor. Since the transistor conducts less current, less current flows through R1, which means that the voltage drop across R1 is decreased. Consequently, the output voltage is increased. From the viewpoint of voltage division, we have simply increased output resistance by decreasing the transistor's forward bias. Proportionately, more of the applied input voltage is therefore felt at the output terminals. To obtain a lower value of regulated voltage, the movable contact on R3 is moved upward (more positive) to increase the transistor's forward bias.

4-10. One of the more noted advantages of the shunt regulator is that it is self-protected against shorts or overloads. Since the regulating device is in parallel with the output, the current through it decreases as the load draws more current. This accounts for the self-protection. On the other hand, a drawback of any shunt regulator is its small-load inefficiencies. We can appreciate this when we realize that the output power is divided between the load and the shunting circuit; at no-load, the shunting circuit dissipates the full output power. Consequently, proportionately large amounts of output power are wasted, particularly when the loads are small. For this reason, the

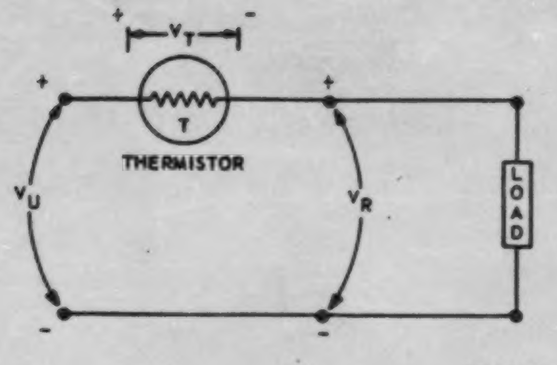


Figure 6-25. Thermistor series regulator.

small-load efficiencies of shunt regulators are notably low.

4-11. **Series Voltage Regulator.** A series-type regulator has comparatively high efficiency under small-load conditions. This is because, as its name implies, the regulating device is in series with the load. When the load draws little current, the current that passes through the regulating device is also small; therefore, the power wasted is not nearly as great as that wasted by a shunt regulator. Full-load efficiencies are about the same for the series and shunt regulators. Unlike the shunt regulator which is self-protected against shorts or overloads, a poorly designed series regulator can have every solid-state device destroyed by even a brief overload. Despite this disadvantage, the series regulator is often used because its small-load efficiency far surpasses that of the shunt regulator.

4-12. In figure 6-25, we have illustrated a thermistor being used as a series regulator to prevent voltage changes caused by variations in load. It acts as a variable resistor in a voltage divider circuit. If the load resistance decreases, tending to lower V_R, the resistance of the thermistor decreases as a result of the additional heating caused by the increased load current. This action keeps the ratio of the thermistor's resistance and load resistance about the same. Since the voltage division of the input is virtually unchanged, V_R is regulated. When a decrease in load occurs, the thermistor's resistance increases to regulate V_R.

4-13. A thermistor used as a series regulator regulates fairly well under changing load conditions, but it will not regulate input variations. In fact, it makes regulation worse instead of better. What would happen if the input voltage, V_U, increased in figure 6-25? Input current would increase, causing the voltage drop across the thermistor to decrease. This is just the opposite of what we want. The drop across the regulating device should increase to prevent a rise in the output voltage. If the series voltage regulator must regulate output voltage under changing input conditions, it is apparent that we will need some type of circuit improvement.

4-14. You can see this improvement in the circuit we have illustrated in figure 6-26. Note that Q1 is a PNP transistor, whereas Q2 is an NPN transistor. Inasmuch as each transistor amplifies, this arrangement is quite sensitive and can give excellent output voltage stability over the designed range. Observe also that the output of this circuit can be adjusted by R3. After we go through one condition of change, you should be able to analyze the circuit to determine its behavior for the other three conditions. We will describe the behavior of the circuit for the condition of increased load. This leaves the conditions of decreased load, increased input, and decreased input for you to go through.

4-15. To prevent V_R from dropping with an increase in load, V_{CE} of Q1 must decrease. Let's keep this in mind and see if it will occur. Any decrease in V_R is fully felt at the emitter of Q2, but it is only partially felt at the base of Q2. Here is why: Since the drop across the Zener diode is constant, any voltage change appears entirely across R1, from the emitter of Q2 to the ground. However, this is not so for the base of Q2. It feels only a fractional amount of the change which is tapped off of R3 in the voltage divider circuit (R2, R3, and

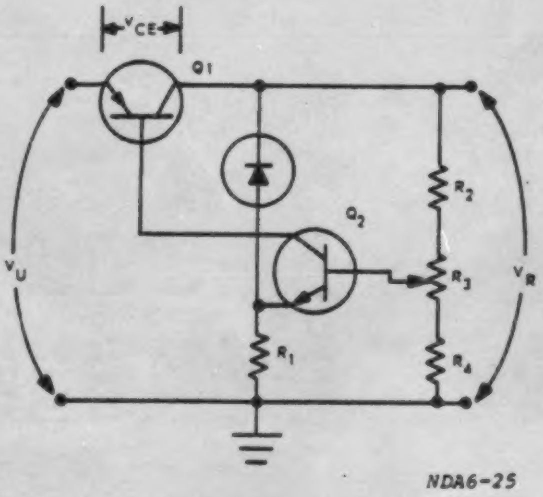


Figure 6-26. PNP transistor series regulator.

R4). Now recall that if the base of an NPN transistor becomes more positive than its emitter, the transistor will conduct more. Therefore, if the emitter of Q2 drops more (becomes less positive) than does the base, the bias increases. Such being the case, Q2 conducts more heavily. Note that the collector current of Q2 is actually the base current, I_B, of Q1. We know then that an increase in I_B of Q1 causes Q1 to conduct more heavily, and its V_{CE} drops accordingly. Isn't this what we wanted to happen?

4-16. From the standpoint of bias on Q1, its base becomes more positive (less negative with respect to its emitter) because Q2 conducts more heavily. Since Q1 is a PNP transistor, the bias decreases and causes the voltage V_{CE} across Q1 to decrease. When you analyze the circuit for the different conditions of changing load and input, you will find that good regulation is the outcome.

4-17. So far in our discussion of regulators, we have only discussed the voltage regulator. However, you will find that within a computer system there are various circuits that require a constant source of current for their operation. Providing this constant source is the job of the constant-current regulator.

4-18. **Constant-Current Regulator.** In contrast with the voltage regulator, the current regulator stabilizes output current, I_R, rather than output voltages, V_R. Its primary function is to supply a constant current to the load. To do this, the regulating device must prevent a change in output current.

4-19. A circuit that can be used for regulating current is illustrated in figure 6-27. Instead of detecting the voltage across the output terminals, the transistor detects the current through R1. Any current change develops a voltage change across R1, which alters the bias of the PNP transistor. The transistor resists the current changes. For example, an increase in current will increase the voltage across R1 and make the emitter of the transistor less positive. This decreases the base-to-emitter forward bias of the PNP transistor and decreases the current flow through it. Therefore, because the transistor action opposes any change in I_R, the output current remains constant.

4-20. Now that we better understand the functions of rectification, filtering, and regulation within the AC to DC power supply, let's take a look at a typical computer solid-state power supply.

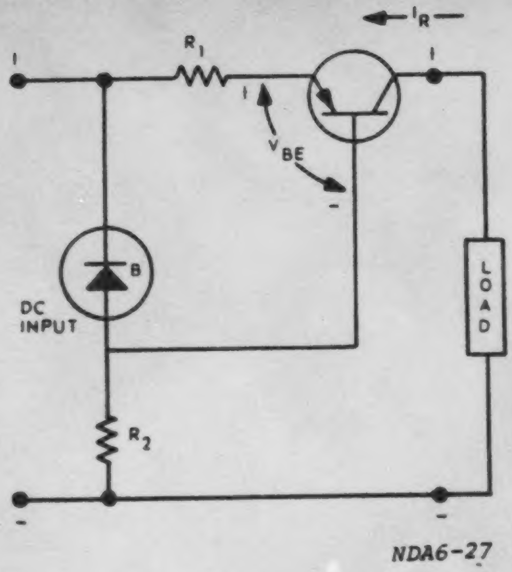
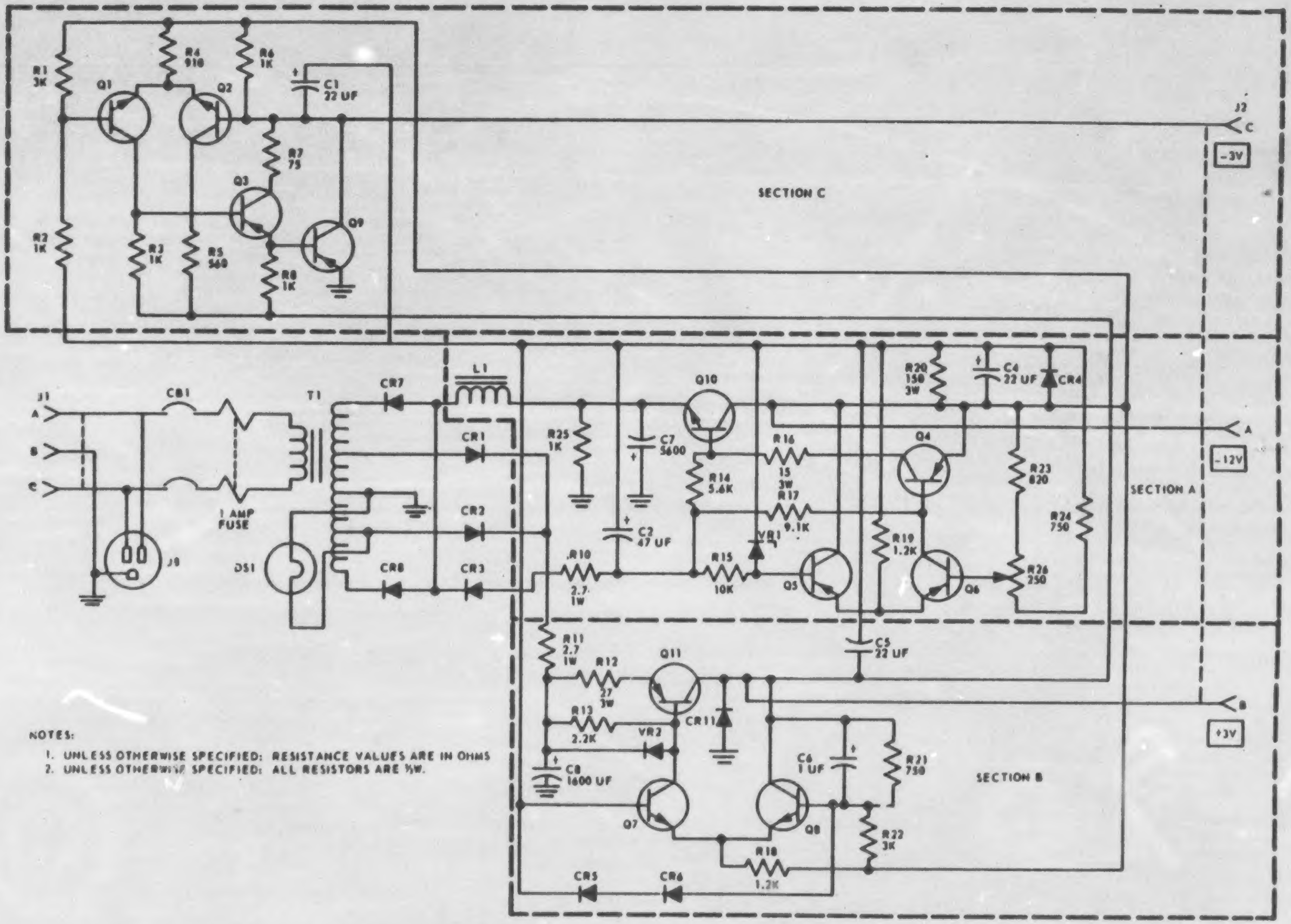


Figure 6-27. Constant-current regulator with PNP transistor.

5. Typical Computer Solid-State Power Supply

5-1. One of the advantages of solid-state power supplies is compactness, which is chiefly important in computers today. As a rule, you will find that a computer module containing a solid-state supply is compact and readily accessible to facilitate maintenance. We have illustrated a schematic of a typical power supply module in figure 6-28. This particular module produces three DC voltages: -12, -3, and +3 volts. These voltages would be utilized within the solid-state logic circuits of the computer. Section A of the schematic contains the circuitry of the -12-volt supply, section B is the +3-volt supply, and section C is the -3-volt supply. Input power is 115 volts ± 10 percent, 60-Hz, single-phase AC.

5-2. The -12-volt portion of the power supply shown in section A is a series-regulated supply. With circuit breaker CB1 turned on, AC power is applied to transformer T1 and power-on light DS1 lights. The AC voltage at the secondary of T1 is full-wave rectified by diodes CR7 and CR8 and filtered by an LC filter circuit consisting of inductor L1 and capacitor C7. Resistor R25 serves mainly to discharge the filter capacitor when power is turned off. A negative DC voltage is also developed by an RC filter circuit consisting of resistor R10, diode CR3, and capacitor C2. This voltage is more negative than that developed by the LC filter; it insures proper


R1 3K
R4 910
R6 1K
C1 22 UF
Q1
Q2
R7 75
Q3
Q9
R2 1K
R3 1K
R5 560
R8 1K
J2
C
-3V
SECTION C
L1
CR7
Q10
R20 150 3W
C4 22 UF
CR4
J1
A
B
C
CB1
T1
CR1
R25 1K
C7 5600
R16 15 3W
Q4
R23 820
A
-12V
SECTION A
R14 5.6K
R17 9.1K
1 AMP FUSE
CR2
C2 47 UF
VR1
R24 750
R19 1.2K
J3
DS1
CR8
CR3
R10 2.7 1W
R15 10K
Q5
Q6
R26 250
R11 2.7 1W
C5 22 UF
R12 27 3W
Q11
B
+3V
R13 2.2K
CR11
VR2
C6 1 UF
R21 750
SECTION B
C8 1600 UF
Q7
Q8
R22 3K
R18 1.2K
CR5
CR6

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS
2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE ½W.

Figure 6-28. Typical solid-state power supply.

biasing within the -12-volt supply. Transistors Q10 and Q4 are the series regulator transistors and may be considered as a single equivalent transistor with a current gain equal to the product of the current gains of both transistors. Transistors Q5 and Q6 form a differential amplifier circuit which compares a sample of the output voltage with a reference voltage set by Zener diode VR1 to provide feedback control of series transistors Q10 and Q4 to insure regulation of the -12-volt output. In other words, if the output voltage increases or decreases, the differential amplifier senses this change and provides feedback to the series-regulating transistors.

5-3. To investigate how the circuit regulates the -12-volt output, let's assume that the voltage changes. If the voltage of the -12-volt line were to go more positive, the base voltage of transistor Q6 would go more positive, since it is derived from the -12 volts through the voltage divider consisting of resistors R23, R26, and R24. (The potentiometer R26 is initially adjusted to set the output voltage at the desired -12 volts.) The base voltage of transistor Q5 is fixed at -5.6 volts by Zener diode VR1 which then fixes the common-emitter voltage of Q5 and Q6 at about -5 volts. Since the base voltage of Q6 went positive for an assumed rise in voltage at the input line and with the emitter voltage of Q6 fixed, the collector voltage of Q6 will go more negative. Transistor Q4 will conduct more heavily due to the increased negative voltage at its base, and the voltage at the emitter of Q4 will go more negative since it must follow the base voltage. Therefore, the effect of the positive-going voltage change is compensated for by an increase in conduction of Q4. Since the base voltage of Q4 went more negative, the collector voltage of Q4 will go more positive, causing Q10 to also conduct more heavily. The voltage drop across Q10 will decrease, thereby bringing the -12-volt line more negative to compensate for the assumed positive increase in voltage.

5-4. The function of diode CR4 is to prevent the -12-volt line from going positive. Capacitor C4 provides filtering of high-frequency line noise. Resistor R20 provides a minimum load for the choke filter when the external load is light so that current is always flowing through the choke.

5-5. A second series regulator circuit which provides +3 volts is shown in section B. Transistor Q11 is the series regulator transistor and transistors Q7 and Q8 form a differential amplifier. A full-wave rectifier consisting of diodes CR1 and CR2 feed into a capacitor filter, C8. Resistor R11 limits the current to protect diodes CR1 and CR2. The base of Q7 is connected to ground. The base voltage of Q8 is set at 0 volts by the voltage dividers R21 and R22 which are between +3 and -12 volts. To analyze the circuit operation under changing output conditions, let's assume that the output voltage goes more positive. The base voltage of Q8 increases, which increases the current through the common-emitter resistor R18, causing Q7 to conduct less. The voltage at the collector of Q7 increases, causing series regulator transistor Q11 to conduct less. The voltage across Q11 increases, causing the output line voltage to go more negative to compensate for the initial positive voltage rise.

5-6. The function of capacitor C6 is to provide greater circuit response to high-frequency line variations. Diodes CR5 and CR6 prevent the base of transistor Q8 from going more positive than about 1 volt; this insures adequate circuit operation when it is initially turned on. Diode CR11 prevents the +3-volt output line from going negative. Capacitor C5 provides filtering of high-frequency noise on the +3-volt line. Resistor R12 provides a short-circuit current limit if the output +3-volt line is shorted. Zener diode VR2 provides the reference voltage for the regulator circuit.

5-7. The third power supply shown in section C provides -3 volts. This circuit employs a shunt regulator circuit consisting of transistors Q3 and Q9. This particular circuit arrangement does not need a filter circuit, because it derives voltage from the -12-volt and +3-volt supplies. The base voltage of transistor Q1 is set at -3 volts by the voltage dividers R1 and R2 which are between -12 volts and ground. Transistors Q1 and Q2 form a differential amplifier. With the emitter voltage of Q1 and Q2 at the same potential, the base voltage of Q2 will be -3 volts, which is the same potential as the base of Q1. If the -3-volt line voltage were to go more positive, transistor Q2 would conduct more and the voltage at the common emitter of Q1 and Q2 would rise, causing Q1 to conduct less and its collector voltage to increase. This increase in Q1's collector voltage would be detected at the base of Q3; therefore, Q3 would conduct less, and the voltage drop across it would increase. The increase in voltage across Q3 would cause the output line voltage to become more negative. The voltage at the base of Q9 would also go more positive, causing it to conduct less. This would allow the -3-volt line to go more negative, thereby compensating for the initial increase in voltage.

5-8. The function of capacitor C1 is to filter the high-frequency noise on the - 3-volt line. Resistor R6 provides a light load between the - 3-volt and - 12-volt lines. The current capacity of this - 3-volt supply is adequate, because it is the type of supply that is normally used to supply a bias or reference voltage for clamping logic circuit outputs (in this case, negative logic). In this particular circuit, the clamp current actually flows from the - 3-volt line through the clamping diode and resistor of the load to the - 12-volt supply; therefore, the - 12-volt supply must handle the current.

6. Analyzing Power Supply Malfunctions

6-1. Regardless of whether you are troubleshooting a solid-state or electron-tube power supply, the troubleshooting procedures are practically the same with regard to circuitry. We will confine our analysis to several common troubles and symptoms that may be caused by defective solid-state devices. We will also briefly discuss the checking of these devices and consider some matters pertinent to their replacement.

6-2. Symptoms and Troubles. Often, the malfunction of a power supply is the fault of the rectifying device. Crystal and metallic rectifier diodes fail, as do electron-tube diodes. Certain faults can be attributed directly to the solid-state rectifier. They are (1) open-circuited rectifier, (2) short-circuited rectifier, (3) high-forward-voltage drop, (4) high-leakage current, and (5) overheated rectifier. The symptoms associated with these faults can be readily detected, since they cause obvious and sometimes serious trouble.

6-3. An open-circuited rectifier causes a lower DC output. If the rectifier unit is a full-wave or polyphase type, the DC output would be reduced when one rectifier is open-circuited. If it is a single-phase half-wave rectifier, there will be no DC output.

6-4. The symptoms just mentioned for the open-circuited rectifier are the same for a short-circuited rectifier. In addition, there will be excessive heating and AC will appear at the output. Unless short-circuit protection is built into the power supply, other circuit components can be permanently damaged.

6-5. Either a high-forward-voltage drop or a high-leakage current will cause lowered DC output and increase heating. A high-forward-voltage drop is caused by an increased forward resistance, whereas a high-leakage current is caused by a decreased reverse resistance. Whichever fault occurs, the rectification ratio is reduced accordingly and likewise the efficiency of the rectifier.

6-6. An overheated rectifier may be caused by faults (2), (3), or (4) mentioned previously, and also can be caused by excessive loading or inadequate cooling. Regardless of the cause, the rectifier that is heated beyond its safe limits will be short-lived or completely destroyed. When the source of the trouble is the rectifier itself, replacement of the rectifier will return the circuit to normal operation. However, when the overheating is the result of loading or improper heat dissipation, the trouble will persist after the rectifier has been replaced, unless corrective measures are taken to insure proper loading and cooling.

6-7. When a power supply has a regulator unit, a defective solid-state device (thermistor, Zener diode, transistor, etc.) may be the source of trouble. The symptoms will range from an increased or reduced DC output (regulated or not) to no DC output. The symptoms and troubles are dependent upon the complexity of the circuitry as well as the type of regulator unit employed. We cannot, therefore, speak on this subject in a general manner. For any particular unit, you will have to depend on your basic knowledges and reasoning ability to determine whether or not a solid-state device could be at fault. If you think that's where the fault is, you will have to test the suspected device.

6-8. Checking and Testing. You can detect symptoms in a number of ways. You will readily discover overheating that produces smoke or an odor. A faulty selenium rectifier, for instance, smells like rotten eggs. You can quickly find abnormal voltages and currents by taking voltmeter and ammeter readings. You can see ripple in the output with an oscilloscope or perhaps even hear it in an audio system. The frequency of the ripple may reveal the trouble; for example, a 60-Hz ripple from a single-phase full-wave unit indicates that you are getting only half-wave rectification. More likely than not, a rectifier is defective.

6-9. You can detect some troubles by a visual inspection. Broken connections and damaged components are usually very obvious. Over-heating often causes discoloration of circuit components. You may see dark spots on the plates of a faulty metallic rectifier. A dark spot indicates a physical rupture of the barrier layer caused by high temperature. If the spot is small, there is probably no permanent damage, because the plates of the metallic rectifier are self-healing. Nevertheless, the effective rectifying area is reduced, and further heating will ultimately cause failure. Although a spot covering less than 20 percent of the plate area is considered within allowable limits, replacement of the rectifier is recommended whenever spotting appears. A faulty metallic rectifier may show burned spots around its contact washer and surrounding area as a result of poor contact with the front electrode. Solder-like blotches seen beneath a rectifier stack are also caused by excessive heating. In this case, the alloy of which the rectifier is made has melted and run off the bottom edge of the cells. Thus, faulty metallic rectifiers can frequently be detected by visual means. This is not true, however, for crystal rectifiers; tests must be made to check their electrical characteristics.

6-10. Checking with an ohmmeter is an easy and practical way of testing a crystal or metallic rectifier to determine whether it is open or shorted. A high resistance (several thousand ohms) measured in both directions indicates that the rectifier is open; a relatively low resistance (a few hundred ohms) measured in both directions indicates that it is shorted. A good rectifier has a low-forward resistance and a high-reverse resistance. Since an ohmmeter applies voltage to the rectifier under test, it is not a reliable instrument for testing quality. Remember that the forward resistance of a solid-state rectifier is not linear but varies as a function of the applied voltage. Therefore, the rectifier must be checked under rated conditions to obtain a conclusive indication of its quality.

6-11. There are many test sets available for testing solid-state devices. Instructions are provided with the set to enable you to test properly. Solid-state devices are identified by prefix letter(s) and a number on the device. Common prefixes are as follows: 1N for crystal diodes, MR or SR for metallic rectifiers, Z (also HZ or MZ) for Zener diodes, and 2N for transistors. Once you've identified the device, you can find its specifications in a booklet or manual. Knowing the rated parameters, you can tell from the readings of the test set whether the device is substandard.

6-12. It is quite possible that the solid-state device may test good and yet be the source of trouble. The only way to find out is by replacing it. As for electron tubes, you can use an identical device that is known to operate properly in place of the questionable one. The time required to change a tube is normally small when compared to the time required to replace a defective solid-state device.

6-13. **Replacements.** You should always replace a faulty circuit component with one exactly like it. When this is not possible, *and you have been authorized to substitute an unlike item*, it might be necessary to make some circuit modifications to protect the circuit or device itself.

6-14. Since solid-state devices can be instantly damaged and are adversely affected by overheating, a casual approach to replacement of circuit components can be costly. Give particular attention to inserting limiting resistors when it is necessary to prevent excess current flow or surges. For example, if you use a larger input-filter capacitor in place of a defective one, turn-on and recurrent surge currents may increase beyond rated limits.

6-15. Stacking and paralleling solid-state rectifiers is a common practice which makes it possible to rectify high voltages and high currents, respectively. Although we showed stacking in only one circuit (fig. 6-4), you should understand that rectifiers can be series-connected in all the rectifier circuits discussed and illustrated in this chapter. The rated PIV of the stack is the sum of the rated PIVs of the individual rectifiers. To get a desired current-handling capacity, you can use crystal or metallic rectifiers in parallel. You can use a combination of series or parallel rectifiers to replace a rectifier of almost any rating.

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TABLE OF CONTENTS

Study Reference Guide

Chapter Review Exercises

Answers for Chapter Review Exercises

Volume Review Exercise

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STUDY REFERENCE GUIDE

1. *Use this Guide as a Study Aid.* It emphasizes all important study areas of this volume. Use the Guide for review before you take the closed-book Course Examination.

2. *Use the Guide for Follow-up after you complete the Course Examination.* The CE results will be sent to you on a postcard, which will indicate "Satisfactory" or "Unsatisfactory" completion. The card will list *Guide Numbers* relating to the items missed. Locate these numbers in the Guide and draw a line under the Guide Number, topic, and reference. Review these areas to insure your mastery of the course.

Guide
Numbers

Guide Numbers 001 through 020

001 Introduction to Number Systems; Number System Features; Basic Numbering System; pages 1-6

002 Number System Conversions; Binary Arithmetic; pages 6-10

003 Introduction to Computer Circuits; Waveshaping and Referencing Circuits; Basic Amplifier Circuits; pages 11-18

004 Oscillator Circuits: Functional Parts of an Oscillator, Inductance-Capacitance (LC), Nonsinusoidal Oscillators; pages 19-23

005 Oscillator Circuits: Blocking Oscillator, Miller Integrator; pages 23-33

006 Boolean Algebra; pages 33-39

007 Logic Gates; pages 39-53

008 Introduction to Computer Components; Counters; pages 54-66

009 Storage Registers; pages 66-75

010 Decoders; Digital and Analog Converters; Encoder; Comparator; pages 75-83

Guide
Numbers

011 Introduction to Computer Units; Typical Computer Systems; Memory: Types of Data Stored, . . . Ferrite Core Memory; pages 84-94

012 Memory: Four-Plane Ferrite Core Memory, Thin-Film Memory, Solid-State Memories; pages 94-99

013 Arithmetic Unit; pages 100-106

014 Control Unit; pages 106-113

015 Introduction to Input-Output Units; Input and Output Components; Tape-Handling Devices; Card-Handling Devices; pages 114-122

016 Keyboard; Printers; pages 122-133

017 Magnetic Drums; Magnetic Disks; pages 133-141

018 Introduction to Computer Power Supplies; Obtaining DC Power for Computer Circuits; Rectifying AC; pages 142-152

019 Filters; Regulating DC; pages 152-159

020 Typical Computer Solid-State Power Supply; Analyzing Power Supply Malfunctions; pages 159-163

CHAPTER REVIEW EXERCISES

The following ecercises are study aids. Write your answers in pencil in the space provided after each exercise. Immediately after completing each set of exercises, check your responses against the answers for that set. Do not submit your answers to ECI for grading.

CHAPTER 1

Objectives: To convert numbers from one system to another and to calculate the sum, difference, product, or quotient of given numbers.

1. What is the place-value of the two (2) in the following number? 1,246.789 (1-2)

2. What was the primary purpose of developing the zero (0) for use in the decimal number system? (1-3)

3. What does the radix or base of a number system indicate? (1-4)

4. Which of the following number systems use alpha characters as symbols? (1) decimal (2) binary (3) octal (4) hexadecimal (1-7)

5. What is the purpose of the point as used in number systems? (1-8)

6. The least significant digit (LSD) of a number is normally located on which side of the number? (1-9)

7. In the following decimal number, which number is the most significant digit (MSD)? $2,876_{10}$ (1-10)

8. What is the decimal value of the three (3) in the decimal number 28731? (2-2)

9. What is the radix of the binary number system? (2-3)

10. List two variations of the binary number system. (2-4)

11. Name an application of the gray code. (2-5)

12. What is another name for the binary-coded decimal system? (2-8)

13. Write the decimal number 22 in binary-coded decimal form. (2-9)

14. What is the radix of the octal number system? (2-10)

15. What is the radix of the hexadecimal system? (2-11)

16. Convert the decimal number 246 to binary, octal, and hexadecimal. (3-2-5)

17. Using the double-dabble method, convert the following numbers to a decimal number. $1011_{(2)}$ $2{,}264_{(8)}$ $142A_{(16)}$ (3-7-9)

18. Convert the following decimal fractions to the specified system: $.625_{(10)}$ to binary, $.384_{(10)}$ to octal, and $.275825_{(10)}$ to hex. (3-10-14)

19. Using the inspection method, convert the following numbers to a specified equivalent number: $4227_{(8)}$ to binary, $111011100110_{(2)}$ to octal, and $3ACF_{(16)}$ to (BCD). (3-15-18)

20. Solve the following binary arithmetic problems. (4-1-12)

a. $\begin{array}{r} 1011_{(2)} \\ +1101_{(2)} \\ \hline \end{array}$ *b.* $\begin{array}{r} 1111_{(2)} \\ +1111_{(2)} \\ \hline \end{array}$ *c.* $\begin{array}{r} 111.111_{(2)} \\ +101.101_{(2)} \\ \hline \end{array}$

d. $\begin{array}{r} 110_{(2)} \\ -01_{(2)} \\ \hline \end{array}$ *e.* $\begin{array}{r} 1011_{(2)} \\ -110_{(2)} \\ \hline \end{array}$ *f.* $\begin{array}{r} 111.111_{(2)} \\ -101.101_{(2)} \\ \hline \end{array}$

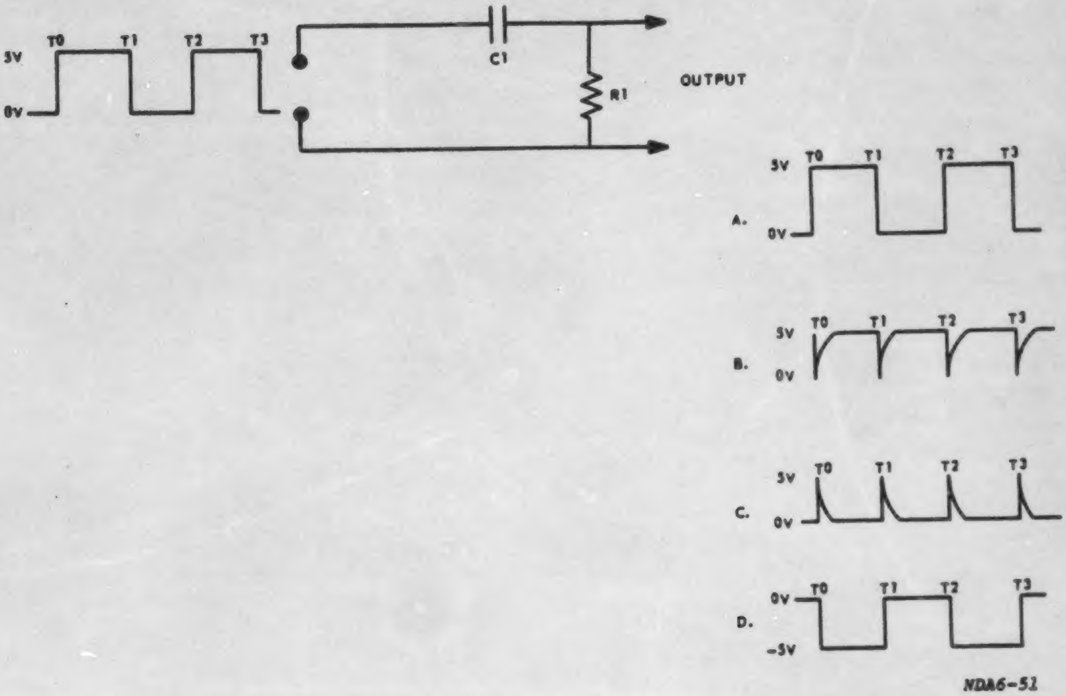
g. $\begin{array}{r} 111001_{(2)} \\ \times \quad 11_{(2)} \\ \hline \end{array}$ *h.* $\begin{array}{r} 11011_{(2)} \\ \times\, 01100_{(2)} \\ \hline \end{array}$ *i.* $\begin{array}{r} 1101111_{(2)} \\ \times \quad 1100_{(2)} \\ \hline \end{array}$

j. $11_{(2)}/\overline{111001_{(2)}}$ *k.* $1100_{(2)}/\overline{11011_{(2)}}$ *l.* $1100_{(2)}/\overline{1101111_{(2)}}$

CHAPTER 2

Objectives: To identify circuits, circuit outputs with specified inputs, and circuit outputs when given specified faulty components; to determine truth tables from given logic gates and write Boolean equations to represent given logic diagrams.

1. In the following circuit, C1 is shorted. Select the output of the circuit. (1-2)

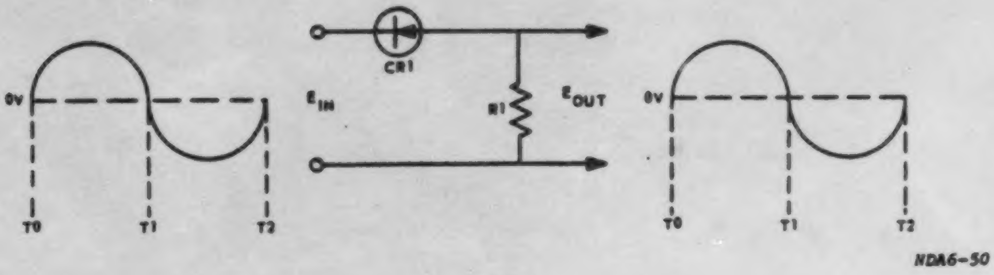


CRE figure 1. For exercise 1, Chapter 2

2. Why are differentiators used as part of the input circuitry of flip-flops? (1-2)

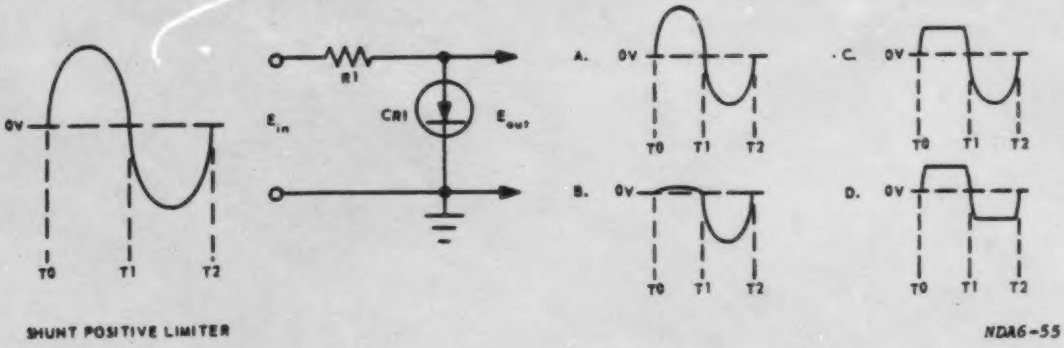
3. List one use for an integrating circuit. (1-4)

4. **In the following circuit, the output is incorrect. What is the most probable cause for the incorrect output? (1-7)**


0V
T0
T1
T2
CR1
E_{IN}
R1
E_{OUT}
0V
T0
T1
T2
NDA6-50

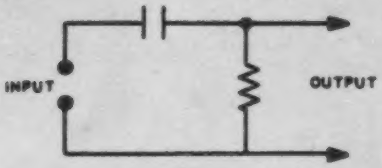
CRE figure 2. For exercise 4, Chapter 2

5. Circle the correct output for the following circuit. (1-7-9)

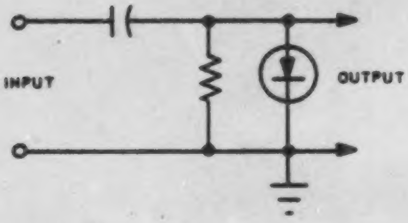

0V
T0
T1
T2
SHUNT POSITIVE LIMITER
R1
E_{in}
CR1
E_{out}
A.
0V
T0
T1
T2
B.
0V
T0
T1
T2
C.
0V
T0
T1
T2
D.
0V
T0
T1
T2
NDA6-55

CRE figure 3. For exercise 5, Chapter 2

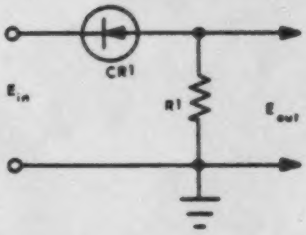
6. **Label the following circuits. (1-1-11)**


INPUT
OUTPUT

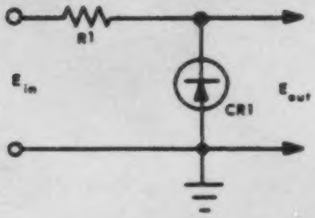
A. ____________________


INPUT
OUTPUT

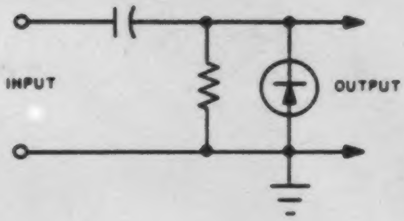
B. ____________________


CR1
E in
R1
E out

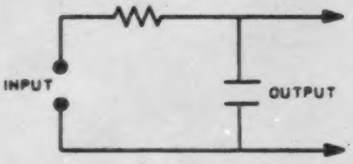
C. ____________________


R1
E in
CR1
E out

D. ____________________


INPUT
OUTPUT

E. ____________________


INPUT
OUTPUT

F. ____________________

NDA6-58

CRE figure 4. For exercise 6, Chapter 2

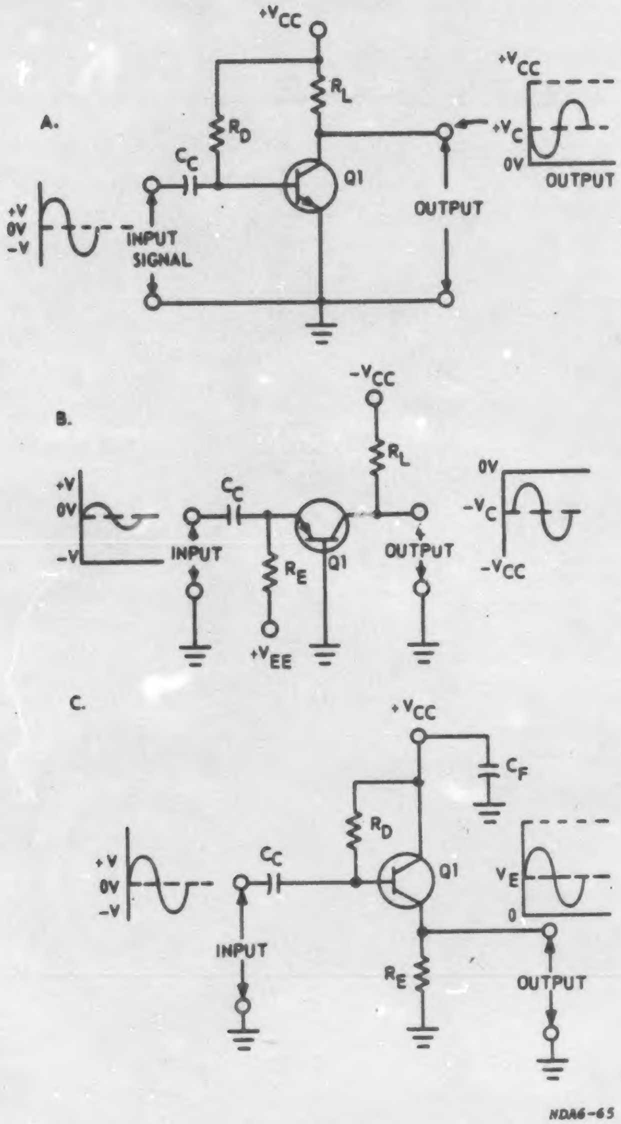
7. What is the identifying feature of a negative clamper? (1-12)

8. List three basic amplifier circuits. (2-1)

9. What is the primary difference between an NPN and a PNP amplifier configuration? (2-5)

10. What is another name for the common-collector amplifier? (2-6)

11. Label the following circuits as CB, CC, or CE. (2-1-10)


A.
+VCC
RL
RD
CC
Q1
+V
0V
-V
INPUT SIGNAL
OUTPUT
+VCC
+VC
0V
OUTPUT
B.
-VCC
RL
+V
0V
-V
CC
INPUT
RE
Q1
+VEE
OUTPUT
0V
-VC
-VCC
C.
+VCC
CF
RD
CC
+V
0V
-V
Q1
VE
0
INPUT
RE
OUTPUT
NDA6-65

CRE figure 5. For exercise 11, Chapter 2

12. Which of the following amplifier circuits has a current gain of less than one: a common emitter, a common collector, or a common base? (Table 2-1)

13. The common-collector amplifier has a large current gain and a large voltage gain. True/False (Table 2-1)

14. What are the basic requirements for oscillation within an oscillator? (3-2)

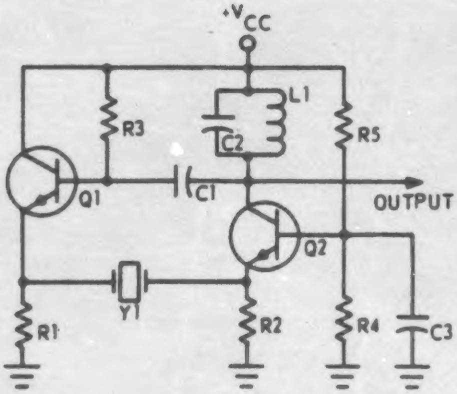
15. What is the identifying feature of a Colpitts oscillator? (3-13)

16. Refer to figure 2-15, A. What is the purpose of C2? (3-14; fig. 2-15)

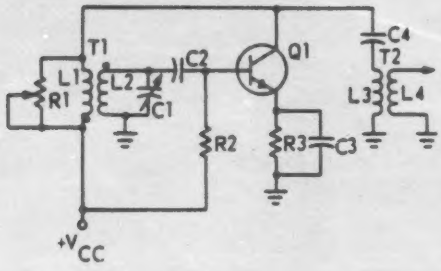
17. What is one desirable characteristic of a crystal-controlled oscillator? (3-15)

18. What is the function of C1 in figure 2-16? (3-16; fig. 2-16)

19. Label the following circuits. (3-1-17)


+VCC
L1
C2
R3
R5
Q1
C1
OUTPUT
Q2
Y1
R1
R2
R4
C3

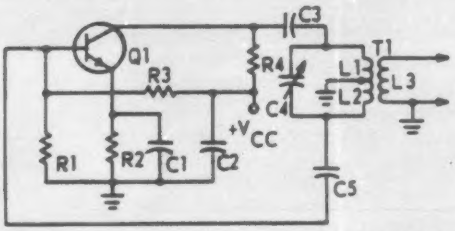
REP4-1424


T1
L1
L2
R1
C1
C2
Q1
C4
T2
L3
L4
R2
R3
C3
+VCC

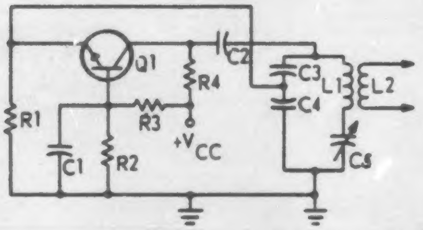
REP4-1416

B ______________________________

A ______________________________


Q1
C3
T1
R3
R4
L1
L2
L3
C4
+VCC
R1
R2
C1
C2
C5

REP4-1420


Q1
C2
C3
R4
L1
L2
C4
R1
R3
+VCC
C1
R2
C5

REP4-1423

C ______________________________

D ______________________________

CRE figure 6. For exercise 19, Chapter 2

20. Another name for the relaxation oscillator is ______________________________ . (3-18)

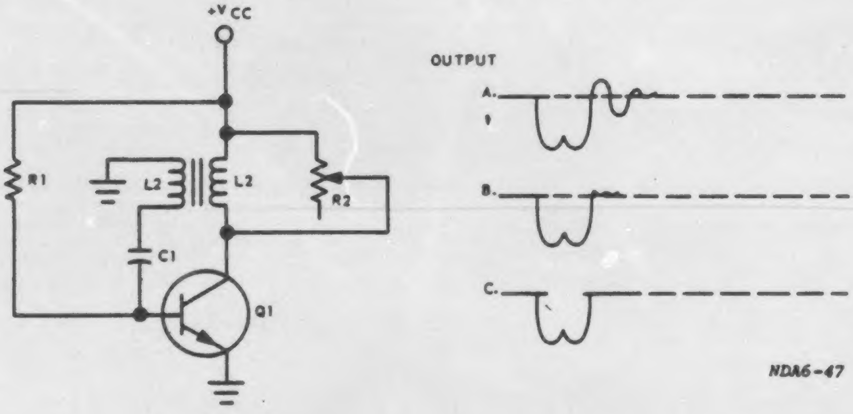
21. List two uses for blocking oscillators. (3-19)

22. List three basic requirements of pulses used within computer systems. (3-20)

23. Refer to figure 2-20, A. Which component provides forward bias for Q1? (3-24; fig. 2-20)

24. Refer to figure 2-20. What controls the PRT of the circuit? (3-25; fig. 2-20)

25. R2 is open in the following circuit. Which of the outputs is likely to occur? (3-26)

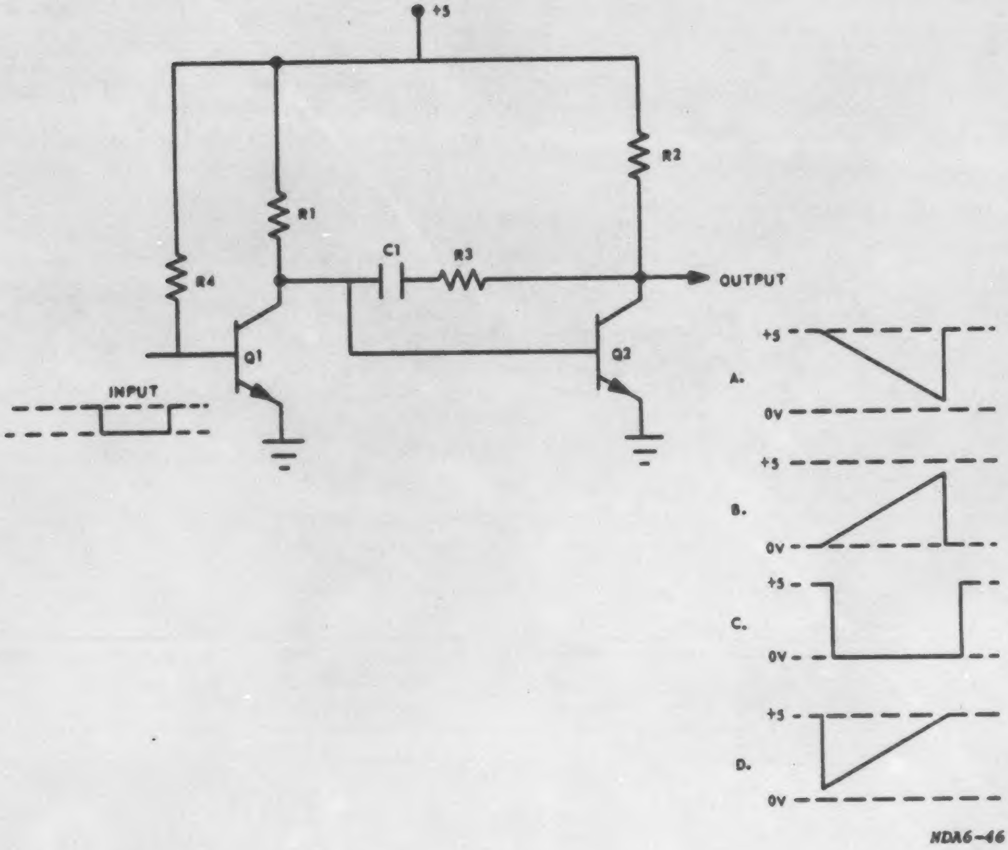


CRE figure 7. For exercise 25, Chapter 2

26. In a synchronized blocking oscillator, the sync pulse (input trigger) frequency will be slightly lower than the free-running frequency of the oscillator. True/False (3-27)

27. What is a common use for the Miller integrator? (3-28)

28. Label the following circuit and select the proper output. (3-28; fig. 2-22)


+5
R2
R1
C1
R3
R4
OUTPUT
Q1
Q2
INPUT
A.
B.
C.
D.
+5
0V
NDA6-46

CRE figure 8. For exercise 28, Chapter 2

29. Why is the flip-flop a valuable circuit for computer use? (3-29)

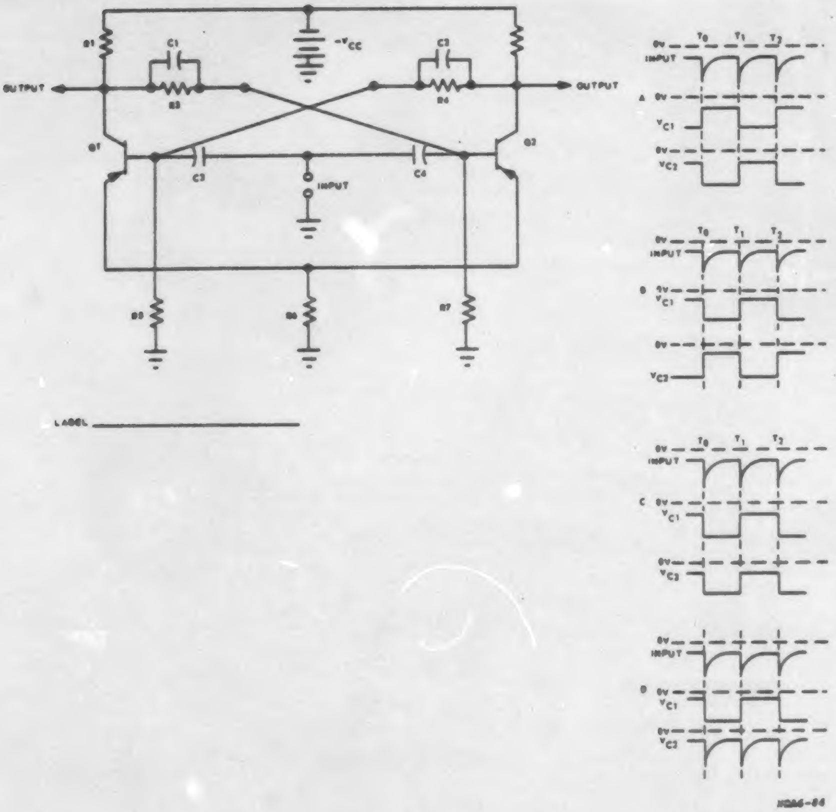
30. What determines the output frequency of the one-shot multivibrator? (3-30)

31. Refer to figure 3-23. Assume that the multivibrator is in the quiescent state. Q2 is cut off, Q3 is conducting, and Q1 is conducting. True/False (3-30)

32. Refer to figure 2-23. There is no output, V_C Q1 is low, and V_C Q2 is low. What is the probable cause? (3-30; fig. 2-23)

33. Refer to figure 2-25. What is the function of C3 and C4? (3-34; fig. 2-25)

34. Label the following circuits and select the circuits' output. (3-33-36; fig. 2-25)


R1
C1
-VCC
C2
OUTPUT
R3
R4
OUTPUT
Q1
Q2
C3
C4
INPUT
R5
R6
R7
LABEL
0V
INPUT
T0
T1
T2
A
VC1
VC2
B
C
D

7

CRE figure 9. For exercise 34, Chapter 2

35. Refer to figure 2-26. What is the function of CR5, CR6, and CR7? (3-37; fig. 2-26)

36. Refer to figure 2-26. What is the function of CR1, CR2, CR3, and CR4? (3-38; fig. 2-26)

37. What is the basic application of Boolean algebra? (4-1)

38. What are the basic functions used in Boolean algebra? (4-3)

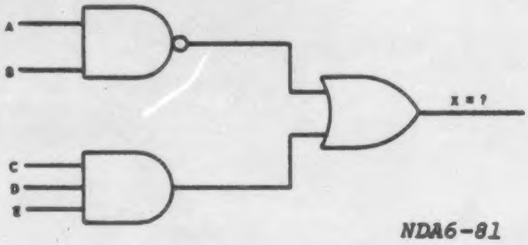
39. What does the sign (+) mean in Boolean algebra? (4-9)

40. What does the sign (·) mean in Boolean algebra? (4-13)

41. What does the sign (−) mean in Boolean algebra? (4-16)

42. What is a truth table? (4-21)

43. *a.* Write the Boolean equation for the circuit in CRE figure 10.
b. Simplify the expression found in step *a.*
c. Draw the logic diagram for the expression found in step *b.*
(4-23-28)



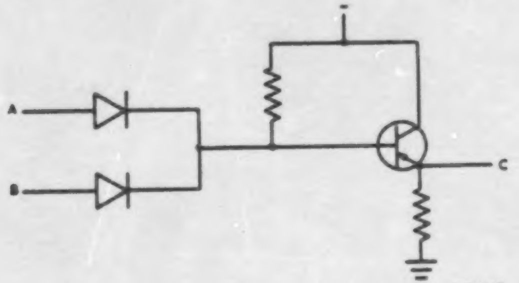
CRE figure 10. For exercise 43, Chapter 2

44. *a.* Draw the logic diagram for the expression X = (A + B) (A + C).
b. Expand the expression (A + B) (A + C) = X.
c. Simplify the result obtained when the expression (A + B) (A + C) was expanded.
d. Draw the logic diagram for the result obtained in step *c*.
(4-29-33)

45. Draw a three-input diode logic gate that performs the positive AND or the negative OR function. (5-6)

46. Draw a three-input diode logic gate that performs the negative AND or the positive OR function. (5-22)

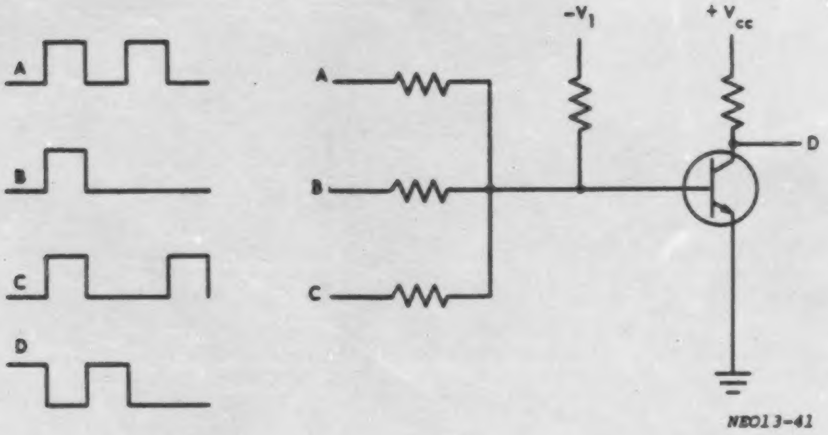
47. Draw the logic symbol or symbols for the circuit in CRE figure 11. (5-35-39)



NDA6-66

CRE figure 11. For exercise 47, Chapter 2

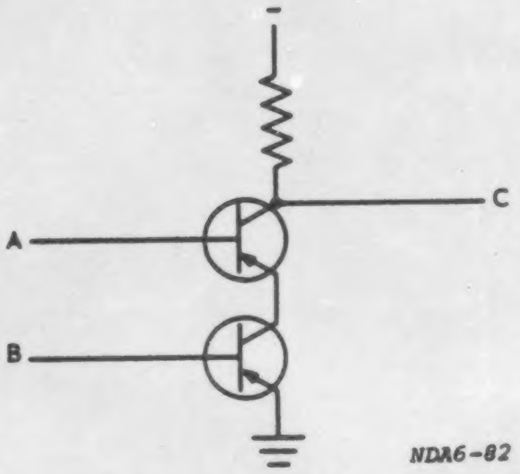
48. Draw the logic symbol or symbols for the circuit in CRE figure 12. (5-40-42)


A
B
C
D
-V$_1$
+V$_{cc}$
A
B
C
D
NEO13-41

CRE figure 12. For exercise 48, Chapter 2

49. Draw the logic symbol or symbols for a three-input parallel DCTL gate. (5-44, 45)

50. Draw the logic symbol or symbols for the circuit in CRE figure 13. (5-46-48)



CRE figure 13. For exercise 50, Chapter 2

51. Draw the logic symbol for an inverter or NOT circuit. (5-49, 50)

52. Draw the logic symbol for an exclusive OR-gate. (5-51-53)

CHAPTER 3

Objective: To identify different types of counting circuits and determine their outputs.

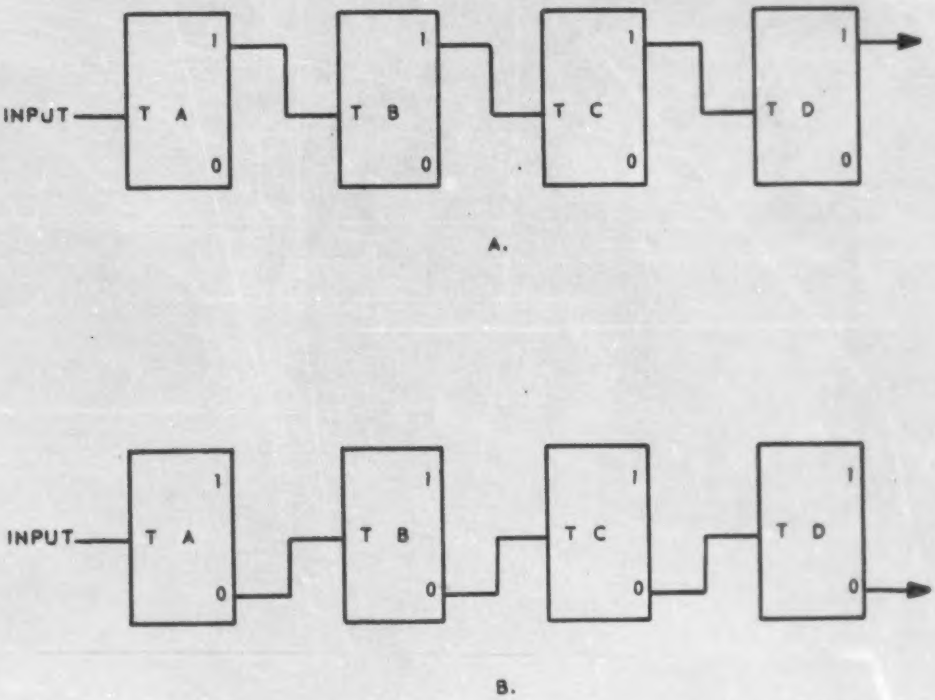
1. What is the basic function of a binary counter? (1-1)

2. How are counters classified? (1-2)

3. Define the term "modulus." (1-2)

4. Compare a serial counter to a parallel counter as to advantage and disadvantage. (1-3)

NOTE: Refer to CRE figure 14, A, to answer questions 5 through 9. (1-10, 21)


INPUT
T A
1
0
T B
1
0
T C
1
0
T D
1
0
A.
INPUT
T A
1
0
T B
1
0
T C
1
0
T D
1
0
B.

NDA6-117

CRE figure 14. For exercises 5 through 11, Chapter 3

5. Identify the circuit shown.

6. What is the maximum count the counter can hold?

7. What is the modulus of the counter?

8. With a count of 12 in the counter, which F/Fs are set?

9. With a count of 8 in the counter and 11 more input pulses applied, what will be the final count in the counter?

NOTE: Refer to CRE figure 14, B, to answer questions 10 and 11. (1-20, 21)

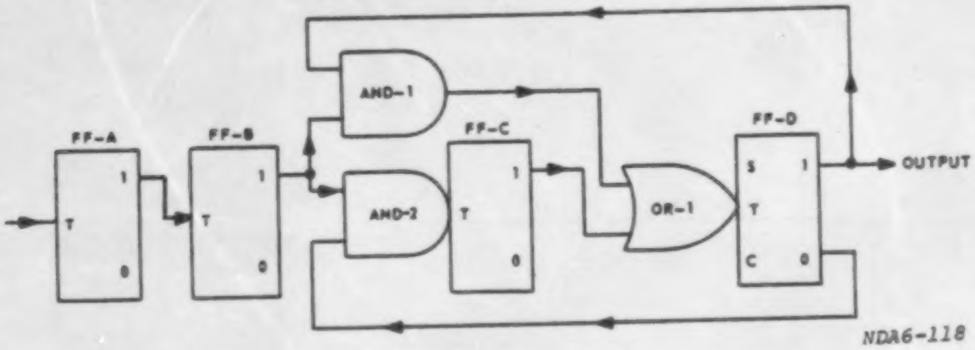
10. Identify the circuit shown.

11. With a count of 8 in the counter and 37 more input pulses applied, determine the final count.

12. A four-stage up-counter is made up of flip-flops A, B, C, and D, with A representing the LSD. Flip-flops A, C, and D are in the ONE state, and flip-flop B is in the ZERO state. What is the count in the counter? (1-20, 21)

13. A down-counter is made up of four flip-flops—A, B, C, and D, with A representing the LSD. Flip-flops A and B are in the ONE state, and flip-flops C and D are in the ZERO state. On the next input pulse, which flip-flop(s) will change states? (1-20, 21)

NOTE: Refer to CRE figure 15 to answer questions 14 through 17. (1-23, 24, 25)



CRE figure 15. For exercises 14 through 17 in Chapter 3

14. Identify the circuit shown.

15. Is this circuit count blocking or count adding?

16. At what count is AND-gate 2 disabled?

17. Flip-flops A, B, and D are in the ONE state and flip-flop C is in the ZERO state. After the next input pulse, what would be the count in the counter if the output of AND-gate 1 is opened?

18. What characteristic of a ring counter separates it from any other type counter? (1-38)

19. What is the maximum count that a four-stage ring counter can count? (1-41)

NOTE: Refer to figure 3-14 of the text for questions 20 through 22.

20. Identify the circuit shown. (2-8)

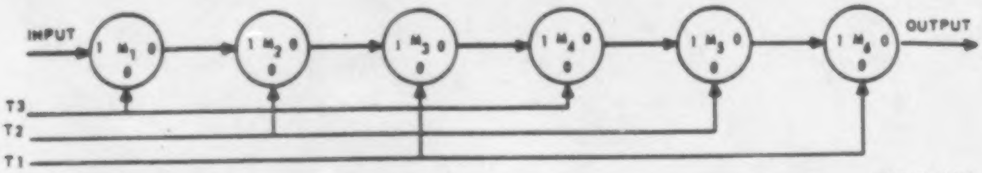
21. Which AND-gates would have a high output with a count of $101_{(2)}$? (2-10, 11)

22. How many shift pulses does it take to shift out a counter of $101_{(2)}$? (2-10, 11)

23. Which state would a bimag core be in if the current entered the dot side of the input winding? The nondot side? (2-19)

24. Refer to figure 3-18 in the text. What is the purpose of the diode? (2-22)

NOTE: Refer to CRE figure 16 for questions 25 through 27.



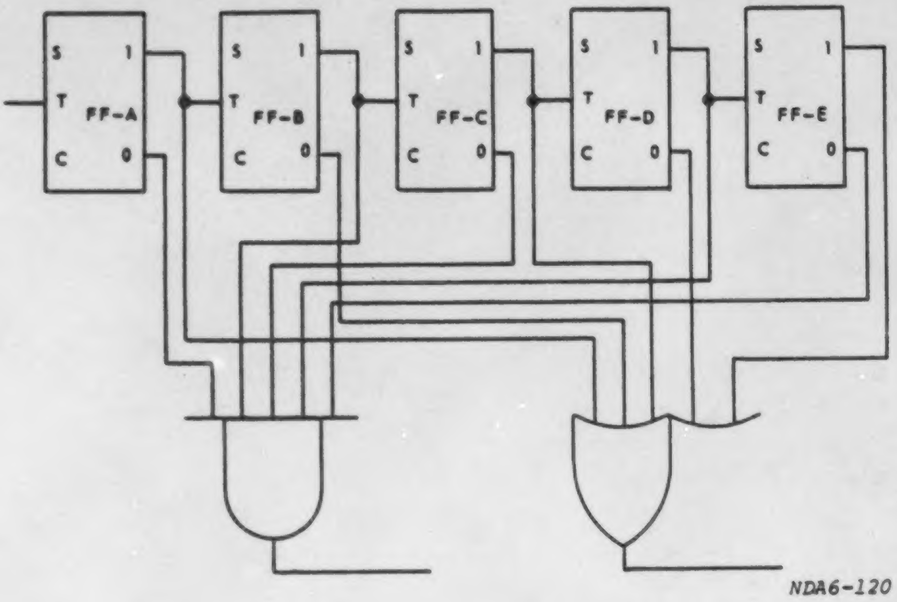
CRE figure 16. For exercises 25 through 27 in Chapter 3

25. Identify the circuit shown. (2-24)

26. What is the binary configuration of the shift register when full? (2-25-28)

27. Starting at time T1, how many shift pulses are required to shift a bit from core M1 to M6? (2-25-28)

NOTE: Refer to CRE figure 17 for questions 28 and 29.

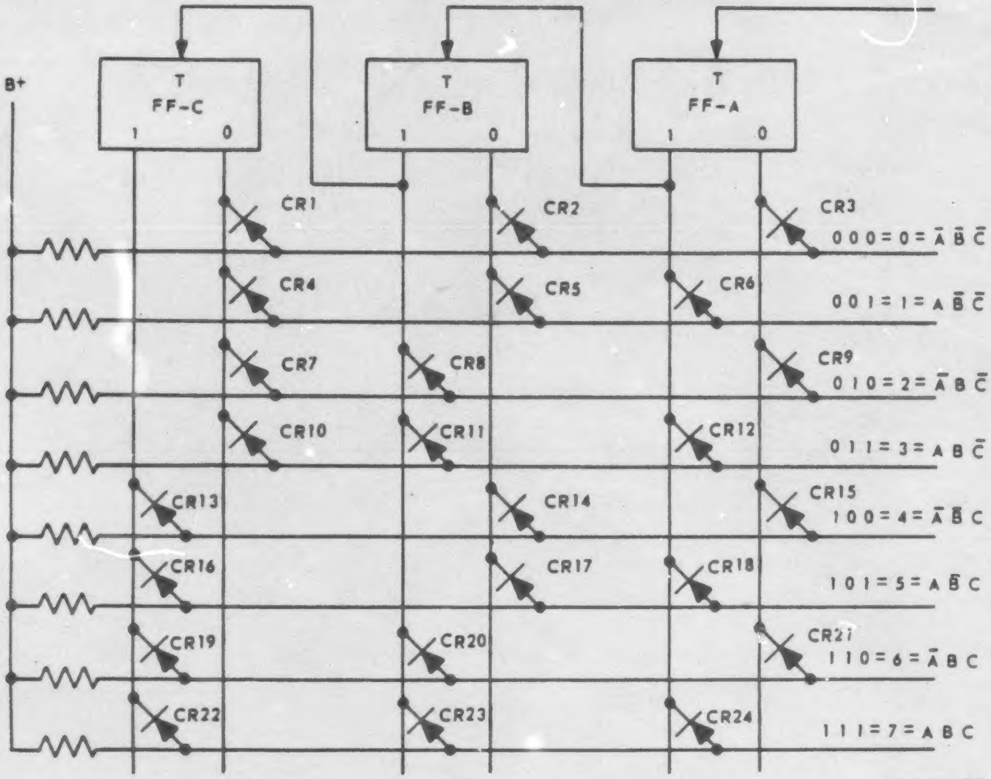


CRE figure 17. For exercises 28 and 29 in Chapter 3

28. Identify the circuit shown. (3-2)

29. Write the Boolean equation for the AND-gate output and the OR-gate output. (3-2)

NOTE: Refer to CRE figure 18 for question 30.


B+
T
FF-C
1
0
T
FF-B
1
0
T
FF-A
1
0
CR1
CR2
CR3
$000 = 0 = \bar{A}\bar{B}\bar{C}$
CR4
CR5
CR6
$001 = 1 = A\bar{B}\bar{C}$
CR7
CR8
CR9
$010 = 2 = \bar{A}B\bar{C}$
CR10
CR11
CR12
$011 = 3 = AB\bar{C}$
CR13
CR14
CR15
$100 = 4 = \bar{A}\bar{B}C$
CR16
CR17
CR18
$101 = 5 = A\bar{B}C$
CR19
CR20
CR21
$110 = 6 = \bar{A}BC$
CR22
CR23
CR24
$111 = 7 = ABC$

NDA6-121

CRE figure 18. For exercise 30 in Chapter 3

30. If CR24 opened, what count would be detected? (3-4)

NOTE: Refer to figure 3-24 in the text for questions 31 and 32.

31. With a count of 27 in the counter, what is the output voltage? (4-4)

32. With an E_{out} of 105 volts, what is the count in the counter? (4-4)

33. Refer to figure 3-26 in the text. What do the dark areas of the converter represent? Light areas? (4-7)

34. Refer to figure 3-27 in the text. If the key that represents 8 is depressed, what resistors have current through them? (5-2)

NOTE: Refer to figure 3-28 in the text for question 35.

35. With a minus (−) stored in F/F-A (F/F cleared) and a plus (+) stored in F/F-B (F/F set), which AND-gates and OR-gates are activated? (6-2)

CHAPTER 4

Objective: To recognize different types of memory, arithmetic, and control unit operations.

1. List the basic units that make up a computer. (1-1)

2. The control unit has control of all computer units. True/False (1-2-3)

3. Give an example of variable data. (2-5, 6)

4. What are the controlling factors that limit the amount of data that can be stored in the magnetostrictive delay line memory? (2-20)

5. How many data bits can be stored in a 15-millisecond delay line memory if the clock rate is 30 kHz? (2-20)

6. List two disadvantages of the delay line memory. (2-26-27)

7. How many cores per plane and how many planes are necessary for a system that must store all the following data? (2-33-62)
   a. 550 nine-bit words of raw data.
   b. 450 nine-bit words of processed data.
   c. 24 nine-bit instruction words.

8. How many X, Y, inhibit, and sense lines are necessary for the core array of question 7? (2-33-62)

9. When reading a core memory location, the sense windings and amplifier sense the flux change of the core as it switches from the ____________ to the ____________ state. (2-40)

NOTE: Refer to foldout 1 for questions 10 and 11. Note that the cores are numbered 0-15 on plane No. 1 (LSD), starting at the top left.

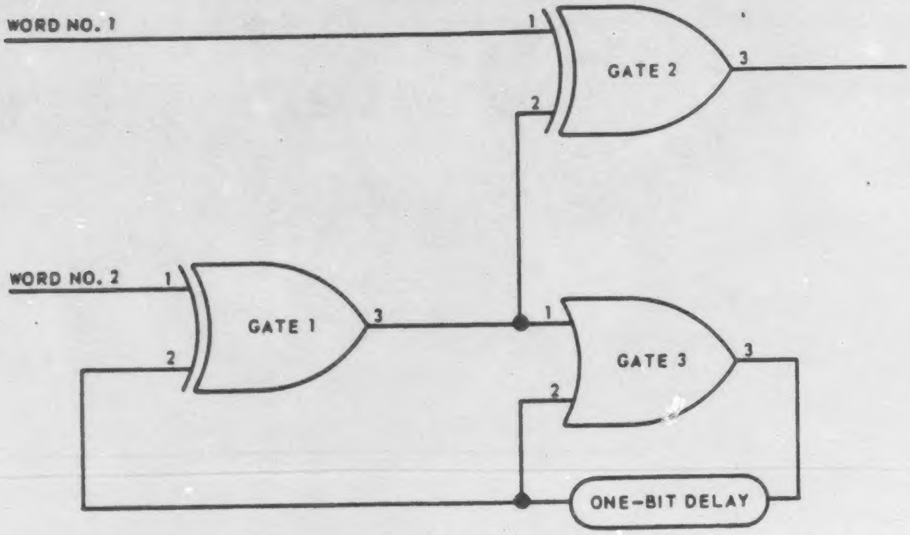
10. The memory illustrated stores ________ bits per plane, ________ bits total, or ________ bit words. (2-46)

11. A data word 1011 (LSD) is to be stored in address 12 $_{(8)}$ of the memory. (2-53-62)
    a. What is the X and Y count in binary?
    b. What cores are fully selected?
    c. What will be the state of the selected cores in each plane?

12. A thin film memory has a state known as a (hard/zero) direction. (2-64)

13. The ________________________, once programmed, cannot be changed. (2-73-75)

14. Refer to CRE figure 19. Word No. 1 is 0101, and word No. 2 is 0011. Identify the circuit and give the output of gate 2. (3-7)



NDA6-130

CRE figure 19. For exercise 14 in Chapter 4

15. The operation performed by the following steps is a/an ____________________ operation. (3-25-31)
    1. Clear all registers.
    2. Enter word in X-register.
    3. Transfer C-register to adding register.
    4. Transfer adding register to accumulator.
    5. Clear X- and adding registers.
    6. Transfer second word to X-register.
    7. Add X-register and accumulator.
    8. Store result in the adding register.

16. The subunit within the control unit responsible for keeping track of the instruction address is the ____________ ____ ______________. (4-7)

17. Of the two types of control units studied in this chapter, which is faster? Why? (4-17-19)

18. A control unit operating at a fixed clock rate is said to be ____________________. (4-17)

CHAPTER 5

Objective: To identify the characteristics, functions, and methods of reading and writing specified input-output devices.

1. What are the two primary functions of the input and output control circuitry? (1-1)

2. What device writes into and reads from the input buffer? (1-3)

3. Name the two types of tapes used in a computer system. (2-1)

4. What tape system would be used to sense a pattern of holes with a photoelectric system? (2-3)

5. What is the common method of recording on magnetic tape? (2-5)

6. Writing occurs on magnetic tape while tape is stopped. True/False (2-9)

7. What is the function of the file protection ring used with a tape reel? (2-12)

8. Describe the computer entry punch operations. (3-2)

9. What letter does a 12-zone punch and a numeric punch 2 represent in Hollerith code? (3-9)

10. What type of device (input or output) is a keyboard? (4-1)

11. How is a character selected for typing on a typehead ball? (4-7)

12. Refer to figure 5-9 of the text. Describe the different positions of the typehead ball when the word AND is typed. (4-12, 14, 15; fig. 5-9)

13. Describe the difference between the D6 and D7 bit used in the field data code. (4-20)

14. Sometimes the impact printer is referred to as a line printer. What does the term "line" mean? (5-2)

15. Describe the function of the synchronizing pulse generator that is used in the impact printer. (5-8)

16. What is another name for the electrographic printer, and why was it given this name? (5-22)

17. What is the purpose of the drum when used as a buffer storage device? (6-3)

18. Why is aluminum used instead of some other material in making magnetic drums? (6-4)

19. How are the read/write heads usually adjusted in reference to the magnetic drum's surface? (6-9)

20. The area of the drum's surface that passes under one read/write head is called a ________________. (6-10, 11)

21. Name two ways in which binary digits can be represented on the drum surface. (6-14)

22. What are the two modes of access used with magnetic drums? (6-23, 24)

23. Refer to figure 5-30 of the text. How is the address counter reset to zero? (6-25; fig. 5-30)

24. Refer to figure 5-32 of the text. If the disk pack illustrated had 15 disks, how many disk surfaces would be available for writing and reading? (7-3; fig. 5-32)

25. What type of access is normally used with magnetic disks? (7-7)

CHAPTER 6

Objectives: To identify the types of rectification, the devices used in voltage regulating, and the filtering systems used in power supplies; to calculate circuit outputs when given specific inputs.

1. Give the function of each of the units shown in figure 6-1. (1-1-5)

2. Name some practical considerations that should be given to an AC to DC power supply that is to be utilized within a computer. (1-6-9)

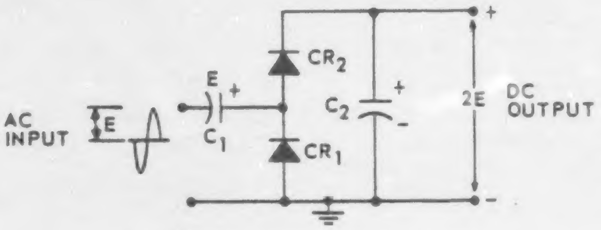
3. If the ripple frequency of a three-phase half-wave rectifier is 120 Hz for an input of 60 Hz, what is likely to be the trouble? Why? (2-10)

4. What are the advantages and disadvantages of half-wave rectifiers? (2-1-13)

5. Why is a polyphase input to a DC supply used instead of a single-phase input? (2-16)

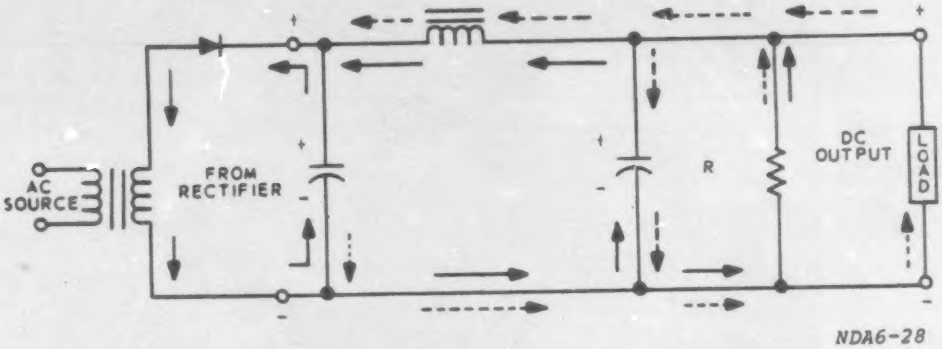
6. For applications requiring high voltage and high current, what type of rectifier circuit should be used? (2-17)

7. What would be the DC output of the circuit shown in CRE figure 20 with a 12-volt peak-to-peak AC input? (2-26)



CRE figure 20. For exercise 7 in Chapter 6

8. **What type of filtering is used in the half-wave rectifier shown in CRE figure 21? (3-9-11)**



CRE figure 21. For exercise 8 in Chapter 6

9. **What type of filter should be used for a power supply if the current requirements of the load are high and voltage regulation is critical? (3-12)**

10. From the following list of electronic devices, select those that can be used for voltage regulating. (4-4-7)
    a. Capacitor.
    b. Coil.
    c. Thermistor.
    d. Zener diode.

11. Why is a shunt voltage regulator self-protecting? Why is its small-load efficiency low? (4-10)

12. Name two types of voltage regulations. (4-2, 11)

13. Describe the sequence of events when there is an increase in DC voltage input, V_U, to the regulator circuit shown in figure 6-26. (4-14-16)

14. What is the basic operational difference between a voltage regulator and a constant-current regulator? (4-18)

15. Refer to figure 6-28. What is the purpose of R10, CR3, and C2? (5-2; fig. 6-28)

16. Refer to figure 6-28. If the voltage of the − 12-volt line goes more positive, what will happen to the voltage drop across Q10? (5-3; fig. 6-28)

17. Refer to figure 6-28. What is the purpose of R12? (5-6; fig. 6-28)

18. Refer to figure 6-28. What type of regulating circuit is used in the − 3-volt portion of the power supply? (5-7; fig. 6-28)

19. The output of a DC power supply is low and the temperature of the power supply is normal. What is the most probable cause? (6-3)

20. A very high resistance is measured in both directions across a metallic rectifier. What is the trouble? (6-10)

21. What is the rated peak-inverse-voltage of a stack of rectifiers? (6-15)

ANSWERS FOR CHAPTER REVIEW EXERCISES

CHAPTER 1

1. Hundreds.
2. For use as a place-holder.
3. The number of different digits used in a number system.
4. Hexadecimal.
5. The point is used to separate the fractional part of a number from the whole part.
6. The extreme right.
7. The two (2) is the MSD.
8. 30.
9. 2.
10. Gray code and binary coded decimal.
11. The code is used in some types of analog-to-digital and digital-to-analog conversion equipment.
12. The 8421 code.
13. 0010 0010.
14. 8.
15. 16.
16. $11110110_{(2)}$, $366_{(8)}$, $F6_{(16)}$.
17. $11_{(10)}$ $1204_{(10)}$ $5162_{(10)}$
18. $.101_{(2)}$ $.3044_{(8)}$ $469C_{(16)}$
19. $4227_{(8)} = 100010010111_{(2)}$
    $111011100110_{(2)} = 7346_{(8)}$
    $3ACF_{(16)} =$ 0011 1010 1100 1111 (BCD)
20. *a.* $11000_{(2)}$
    b. $11110_{(2)}$
    c. $1101.1_{(2)}$
    d. $101_{(2)}$
    e. $101_{(2)}$
    f. $10.01_{(2)}$
    g. $10101011_{(2)}$
    h. $101000100_{(2)}$
    i. $10100110100_{(2)}$
    j. $10011_{(2)}$
    k. $10.01_{(2)}$
    l. $1001.01_{(2)}$

CHAPTER 2

1. The correct choice is A.

2. To produce a sharp spike.

3. Used as an input to a Schmitt trigger.

4. CR1 is shorted, allowing the positive portion of the input signal to be developed across R1.

5. Choice B is the correct output.

6. *a.* Differentiator.
   b. Shunt negative limiter.
   c. Negative clamper.
   d. Positive clamper.
   e. Series positive limiter.
   f. Integrator.

7. The diode's anode is connected to the capacitor.

8. Common emitter (CE), common base (CB), and common collector (CC).

9. The primary difference is the polarity of V_{CC}.

10. Another name is emitter follower.

11. *a.* CE.
    b. CB.
    c. CC.

12. The common-base amplifier has a current gain of less than one.

13. False. The common-collector amplifier has a large current gain and less than one voltage gain. It also has the lowest power gain.

14. The basic requirements are a frequency-determining device, amplification, and regenerative feedback.

15. The identifying feature is split capacitors in the tank circuit.

16. C2 is a decoupling capacitor for the power source.

17. The crystal-controlled oscillator has very good frequency stability.

18. Coupling capacitor.

19. *a.* Crystal-controlled Butler oscillator.
    b. Armstrong oscillator.
    c. Shunt-fed Hartley oscillator.
    d. Colpitts oscillator.

20. Nonsinusoidal oscillator.

21. Some uses of blocking oscillators are frequency dividers, counter circuits, and switching of other circuits.

22. The requirements are fast rise time, flat top, fast fall time, and accurately controllable frequency.

23. R1 provides forward bias for Q1.

24. The time constant of R1 and C1 controls the PRT of the circuit.

25. A is the correct option.

26. False. The frequency is slightly higher.

27. The Miller integrator is commonly used as a sawtooth generator.

28. Miller integrator. Output is A.

29. Because it has two stable states, it can be used to represent binary 1 and 0.

30. Output frequency is determined by the input frequency (one pulse in, one pulse out).

31. False. Note that Q1 is a switching transistor and conducts only when an input is applied.

32. R1 is open, C1 shorted, or Q2 shorted.

33. C3 and C4 are coupling capacitors.

34. The circuit is a bistable multivibrator, and the proper output is represented in option A.

35. The diodes form an input AND-gate.

36. To maintain the logic levels at 0 volts and - 10 volts.

37. The basic application of Boolean algebra is to express logic functions mathematically.

38. The basic functions are the OR function, the AND function, and the NOT function.

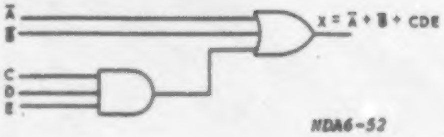
39. The sign (+) in Boolean algebra indicates logical addition or OR.

40. The sign (·) in Boolean algebra indicates multiplication or AND.

41. The sign (−) in Boolean algebra indicates the NOT function as is used to indicate the complement of a term.

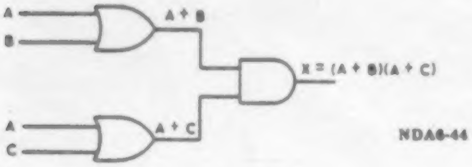
42. The truth table is a tabulation of the possible values of the variables in a specific Boolean expression.

43. *a.* $X = \overline{AB} + CDE$
 b. $\overline{AB} + CDE = \overline{A} + \overline{B} + CDE$
 c.


$\overline{A}$
$\overline{B}$
C
D
E
$X = \overline{A} + \overline{B} + CDE$
NDA6-52

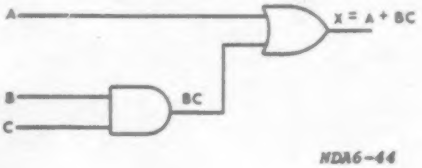
ACRE figure 1. Answer to exercise 43c, Chapter 2.

44. *a.*


A
B
A + B
X = (A + B)(A + C)
A
C
A + C
NDA6-44

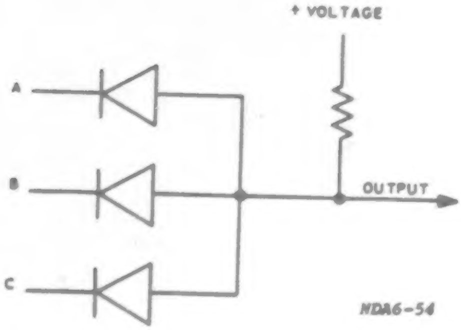
ACRE figure 2. Answer to exercise 44a, Chapter 2.

 b. $(A + B)(A + C) = A \cdot A + A \cdot C + A \cdot B + B \cdot C.$
 c. $AA + AC + AB + BC = A + BC$
 d.


A
X = A + BC
B
C
BC
NDA6-44

ACRE figure 3. Answer to exercise 44d, Chapter 2

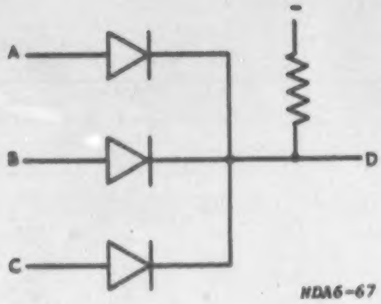
45.


+ VOLTAGE
A
B
OUTPUT
C
NDA6-54

ACRE figure 4. Answer to exercise 45, Chapter 2

371

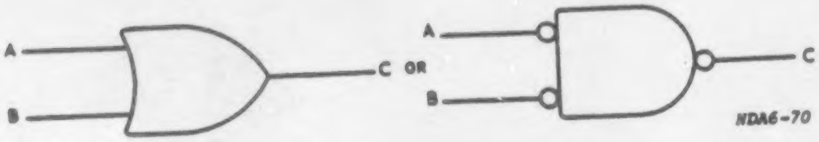
46.



A
B
C
D
NDA6-67

ACRE figure 5. Answer to exercise 46, Chapter 2

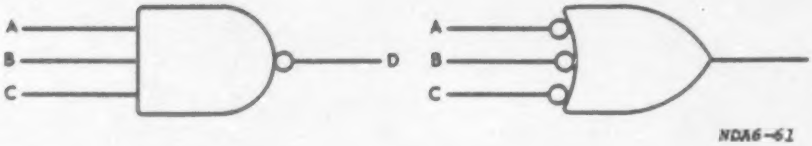
47.



A
B
C
OR
A
B
C
NDA6-70

ACRE figure 6. Answer to exercise 47, Chapter 2

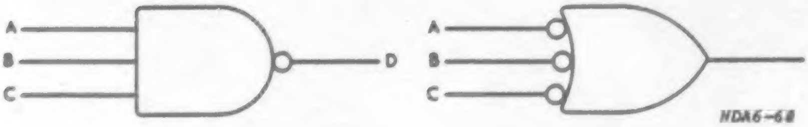
48.



A
B
C
D
A
B
C
NDA6-61

ACRE figure 7. Answer to exercise 48, Chapter 2

49.

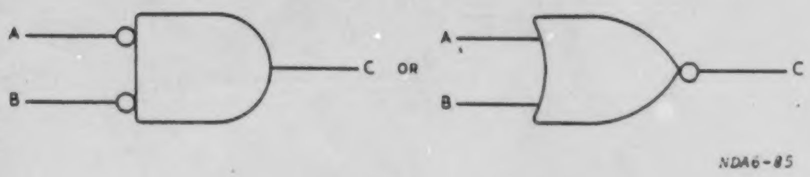


A
B
C
D
A
B
C
NDA6-68

ACRE figure 8. Answer to exercise 49, Chapter 2

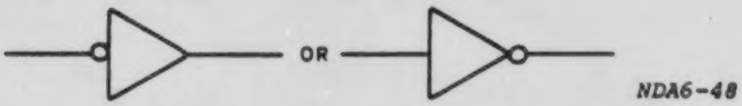
383

50.



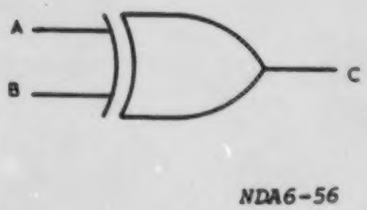
ACRE figure 9. Answer to exercise 50, Chapter 2

51.



ACRE figure 10. Answer to exercise 51, Chapter 2

52.



ACRE figure 11. Answer to exercise 52, Chapter 2

CHAPTER 3

1. Counts according to the binary system and records the number of events which have occurred.
2. Circuit design and function.
3. The number of pulses required to recycle a counter.
4. Advantage is: serial counters require less circuitry; disadvantage is: they are slow.
5. Serial up-counter.
6. 15.
7. 16.
8. F/Fs A, C, D.
9. CC would be 3 (1 cycle and remainder of 3).
10. Serial down-counter.

11. CC would be 13 (1 cycle and remainder of 13).

12. $1101_{(2)}$ or 13 decimal.

13. A.

14. Mod-12 counter.

15. Count blocking.

16. 8.

17. 8.

18. Only one stage can be in the ONE state at any given time.

19. Four.

20. Parallel-in/serial-out.

21. AND-gates 2, 4, and 6.

22. 3.

23. The ONE state; ZERO state.

24. The diode provides a back resistance when M1 switches to the ONE state, preventing M2 from prematurely switching to the ONE state.

25. Three-core-per-two-bit magnetic shift register.

26. $011011_{(2)}$.

27. 11.

28. Count detection circuit.

29. The Boolean equation for the AND-gate output is $\overline{A}B\overline{C}D\overline{E}$. For the OR-gate output it is $A+\overline{B}+C+\overline{D}+E$.

30. 6 and 7.

31. 135V.

32. $10101_{(2)}$.

33. Conducting material; nonconducting material.

34. R8, R5, R3, and R1.

35. They are unlike signs, so AND-gate 4 and OR-gate 6 are activated.

CHAPTER 4

1. Arithmetic, control, memory, input, and output.

2. True.

3. An intercept point, or information for an account number in a supply system's computer.

4. The physical length of the delay line and the clock rate.

5. 450 bits.

6. Volatile storage and serial data.

7. 1024 cores per plane, 9 planes.

8. 32 X, 32 Y, 9 inhibit, and 9 sense lines.

9. ONE; ZERO.

10. 16; 64; 16, 4.

11. *a.* 01(Y), 10(X).
    b. Core 13 in each plane.
    c. Core 13 in planes 1, 2, and 4 are in the ONE state; core 13 in plane 3 is ZERO.

12. Hard.

13. Solid-state ROM.

14. Full-adder, $1000_{(2)}$.

15. ADD.

16. Program control.

17. The asynchronous control. It is faster because one pulse sent into the delay line will generate a number of commands from the one pulse, and the timing is not locked as it is in the synchronous control unit. The pulses in the synchronous control are at a set rate with each step following the last.

18. Synchronous.

CHAPTER 5

1. Decrease computer waiting time, and translate incoming and outgoing data to a usable form.

2. Input device writes into the buffer; the computer reads the buffer.

3. Paper tape and magnetic tape.

4. Paper tape system.

5. 1's and 0's are both written.

6. False. The tape is moving.

7. To prevent writing when removed and allow writing when installed in the tape reel.

8. Punches a card; reads the card, and converts information read to voltages that are fed to the computer.

9. B.

10. Input and output.

11. The typehead ball is tilted and rotated.

12. A = tilt 1, rotate -5; N = tilt 0, rotate 2; D = tilt 2, rotate 1.

13. D6 is the control bit; D7 is the parity bit.

14. It means that when printing, the printer prints a line at a time.

15. To produce pulses that are synchronized tc the rows of characters on the print row and identify these characters.

16. Wire matrix printer; it is given this name because it burns the imprint of a wire matrix character onto a specially prepared paper.

17. It acts as a time buffer between slow-speed equipment and the high-speed computer.

18. Because it is paramagnetic and dissipates heat rapidly.

19. At operating temperature, to within 0.001 to 0.002 inches of the drum surface.

20. Channel.

21. Return-to-zero (RZ) and nonreturn-to-zero (NRZ).

22. Random and sequential.

23. By the index pulse for the drum's index channel.

24. 28.

25. Random access.

CHAPTER 6

1. The power source provides the AC input to the transformer unit. The function of the transformer unit is to step up or step down the AC to the desired level for rectification. The rectifier unit converts the AC into raw (unregulated) DC and filters out the ripple frequency. The function of the regulator unit is to maintain a constant DC output to the load.

2. Some practical considerations that should be given to an AC to DC power supply are: voltage and current requirements of the computer circuits; source and load variations; and percent of regulation required in the output.

3. If the ripple frequency of a three-phase half-wave rectifier is 120 Hz with a 60-Hz input, one of its rectifiers is most probably open-circuited. Since the filter is designed for 180 kHz, a 120-Hz ripple may appear in the output when one phase is not being rectified.

4. The principal advantages of the half-wave rectifiers are simplicity and high DC output voltage (nearly peak secondary AC voltage). Because its ripple frequency is comparatively low (same as input frequency), its output has poor quality for heavy or varying loads. Another disadvantage is that the rectifier must withstand twice the peak AC voltage as PIV when a capacitor-input filter is used.

5. A polyphase input yields higher ripple frequencies and a lower percent of ripple in the output. This facilitates filtering and regulation.

6. The full-wave bridge rectifier should be used for applications requiring high voltage and high current.

7. 12 volts DC.

8. Capacitor input filtering.

9. When the current requirements of the load are high and the output regulation is critical, a choke-input filter should be used.

10. Thermistor and Zener diode.

11. Since the regulating device is in parallel with the output, any load short or overload cannot damage a shunt regulator. For a shunt regulator, current through the regulating device decreases as the load current increases. This accounts for the self-protection and also for its low small-load efficiency. Since the current through the regulating device increases as load decreases to maintain the input current constant, the ratio of output power to input power necessarily decreases. Thus, its small-load efficiency is low.

12. Shunt and series.

13. In the circuit in figure 6-26, if V_U increases, the voltage across R1 increases more than the increase from R3 to ground. Thus, the base-emitter forward bias decreases and current through Q2 decreases. Since the current through Q2 is the base current of Q1, when it decreases, Q1 conducts less. Consequently, the drop across Q1 increases by almost the full amount of the input rise, which means V_R stays practically the same.

14. A constant-current regulator is designed to sense current changes and to automatically oppose the change, thereby maintaining a steady current flow. It differs from a voltage regulator which senses voltage changes and acts to keep its DC voltage output constant.

15. They form a filter network which develops a negative DC voltage.

16. It will decrease.

17. Provides current limiting for the +3-volt output line.

18. Shunt regulation.

19. An open-circuited rectifier is the most probable cause.

20. The rectifier is open.

21. It is the sum of the rated PIVs of the individual rectifiers.

STOP–

1. MATCH ANSWER SHEET TO THIS EXERCISE NUMBER.
2. USE NUMBER 1 OR NUMBER 2 PENCIL.

30554 01A 21

EXTENSION COURSE INSTITUTE
VOLUME REVIEW EXERCISE

Carefully read the following:

DO'S:

1. Check the "course," "volume," and "form" numbers from the answer sheet address tab against the "VRE answer sheet identification number" in the righthand column of the shipping list. If numbers do not match, take action to return the answer sheet and the shipping list to ECI immediately with a note of explanation.
2. Note that numerical sequence on answer sheet alternates across from column to column.
3. Use a medium sharp #1 or #2 black lead pencil for marking answer sheet.
4. Circle the correct answer in this test booklet. After you are sure of your answers, transfer them to the answer sheet. If you *have* to change an answer on the answer sheet, be sure that the erasure is complete. Use a clean eraser. But try to avoid any erasure on the answer sheet if at all possible.
5. Take action to return entire answer sheet to ECI.
6. Keep Volume Review Exercise booklet for review and reference.
7. If *mandatorily* enrolled student, process questions or comments through your unit trainer or OJT supervisor.
   If *voluntarily* enrolled student, send questions or comments to ECI on ECI Form 17.

DON'TS:

1. Don't use answer sheets other than one furnished specifically for each review exercise.
2. Don't mark on the answer sheet except to fill in marking blocks. Double marks or excessive markings which overflow marking blocks will register as errors.
3. Don't fold, spindle, staple, tape, or mutilate the answer sheet.
4. Don't use ink or any marking other than a #1 or #2 black lead pencil.

NOTE: TEXT PAGE REFERENCES ARE USED ON THE VOLUME REVIEW EXERCISE. In parenthesis after each item number on the VRE is the *Text Page Number* where the answer to that item can be located. When answering the items on the VRE, refer to the *Text Pages* indicated by these *Numbers*. The VRE results will be sent to you on a postcard which will list the *actual VRE items you missed*. Go to the VRE booklet and locate the *Text Page Numbers* for the items missed. Go to the text and carefully review the areas covered by these references. Review the entire VRE again before you take the closed-book Course Examination.

Multiple Choice

1. (001) The radix of the octal number system is

a. 2.
b. 8.
c. 10.
d. 16.

2. (003) In the decimal number 42,671, which digit is the MSD?

a. 2.
b. 1.
c. 7.
d. 4.

3. (007) The octal equivalent of 12_{10} is

a. 17.
b. 14.
c. 11.
d. 7.

4. (007) The decimal equivalent of $139B_{(16)}$ is

a. 5017.
b. 5018.
c. 5019.
d. 5000.

5. (008) The octal equivalent of $.750_{(10)}$ is

a. 0.2.
b. 0.3.
c. 0.5.
d. 0.6.

6. (008) The binary equivalent of $5672_{(8)}$ is

a. 101110111010.
b. 110110111010.
c. 111110101111.
d. 101110101010.

7. (009) The sum of $1101_{(2)}$ and $1011_{(2)}$ is

a. 10110.
b. 11000.
c. 10111.
d. 11100.

8. (010) Multiply $11101_{(2)}$ by $10_{(2)}$. The answer is

a. 111011.
b. 111010.
c. 1001011.
d. 1010001.

9. (011) In computer circuits, a differentiator produces an output signal that is a

a. negative-going square wave.
b. positive-going square wave.
c. pulse with slow rise time.
d. sharp spike.

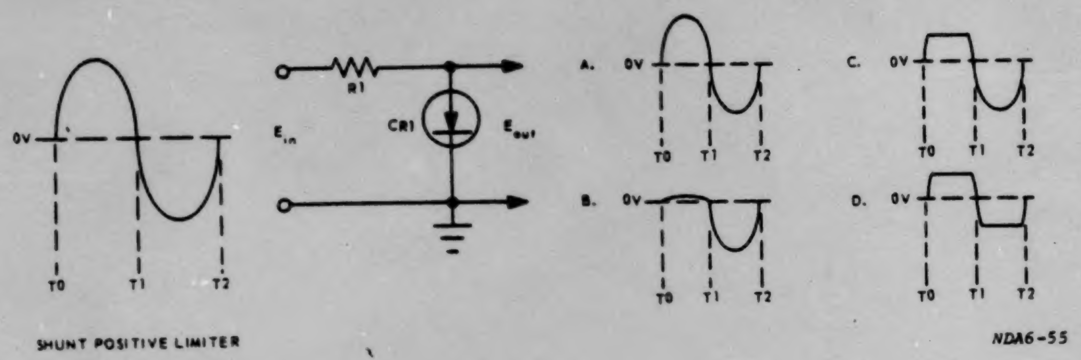


Figure 1 for Volume Review Exercise Question 10

10. (013) Refer to the circuit and options illustrated in VRE Figure 1. Select the option that represents the correct output waveform for the input illustrated.

    a. c.
    b. d.

11. (016) In a common emitter amplifier circuit, the

    a. input is applied between the base and collector.
    b. input is applied between the base and emitter.
    c. output is taken between the collector and base.
    d. output is taken between the emitter and ground.

12. (017) The emitter follower uses the

    a. common emitter configuration.
    b. grounded emitter configuration.
    c. common base configuration.
    d. common collector configuration.

13. (018) In a PNP common base amplifier circuit, a positive input signal will cause

    a. a negative-going output signal.
    b. the voltage drop across the load resistor to decrease.
    c. emitter and collector current to decrease.
    d. a positive-going output signal.

14. (018) The common emitter amplifier has

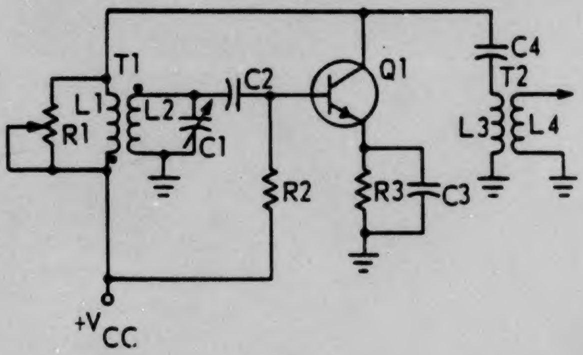
    a. low-current gain, high-voltage gain.
    b. high-current gain, low-voltage gain.
    c. high-current gain, high-voltage gain.
    d. low-current gain, low-voltage gain.

15. (019) Some uses for oscillators in computer systems include

a. clock-pulse generation, timing generation, and gating.
b. timing generation, gating, and signal generation.
c. timing generation, clock-pulse generation, and signal generation.
d. clock-pulse generation, signal generation, and decoding.

16. (019) The frequency of an LC oscillator is determined by the

a. physical size of the components.
b. V_{cc} voltage of the oscillator.
c. swamping resistor.
d. resonant frequency of the tuned circuit.



REP4-1416

Figure 2 for Volume Review Exercise Question 17

17. (019) Refer to VRE Figure 2. Select the components that make up the frequency determining device.

a. L1 and L2 of T1.
b. L1 of T1, C2, and C1.
c. L2 of T1 and C1.
d. L3 and L4 of T2.

18. (020) The regenerative feedback in an Armstrong oscillator is controlled by the variable

a. capacitor.
b. indicator.
c. V_{cc}.
d. resistor.

19. (021) Which of the following oscillator circuits is most commonly used in computer circuits?

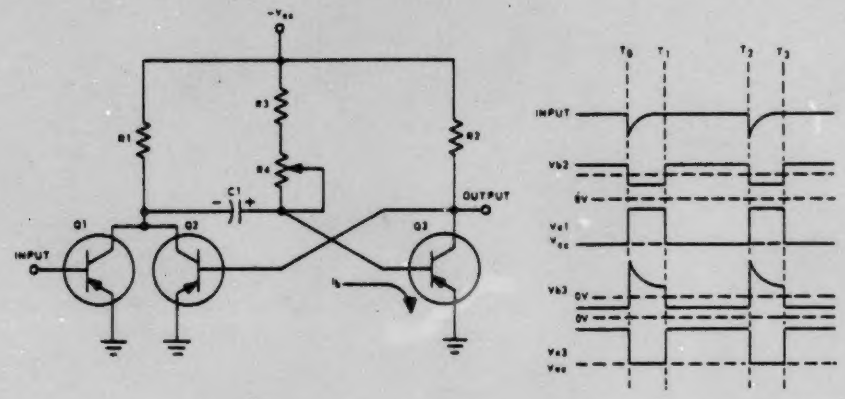
a. Colpitts.
b. Armstrong.
c. Hartley.
d. Butler.

20. (023) A blocking oscillator is normally used to produce a

a. square wave.
b. sine wave.
c. narrow pulse.
d. wide pulse.

21. (023) Some basic requirements for pulses used within computer systems are

a. fast rise time, flat top, and slow fall time.
b. fast rise time, flat top, and fast fall time.
c. slow rise time, rounded top, and fast fall time.
d. fast rise time, rounded top, and slow fall time.


-Vcc
R3
R1
R2
R4
C1
- +
OUTPUT
Q1
Q2
Q3
INPUT
Ib
T0
T1
T2
T3
INPUT
Vb2
0V
Vc1
Vcc
Vb3
0V
0V
Vc3
Vcc

NDA6-69

Figure 3 for Volume Review Exercise Question 22 and 23

22. (028) Refer to VRE Figure 3. The circuit represented in the illustration is a

a. single-shot multivibrator.
b. relaxation oscillator.
c. flip-flop circuit.
d. Miller integrator.

23. (028) Refer to VRE Figure 3. With power applied and no input signal applied,

a. Q2 is conducting, Q3 is cut off.
b. Q1 is conducting, Q2 is cut off.
c. Q3 is conducting, Q2 is cut off.
d. Q1 is conducting, Q2 is conducting.

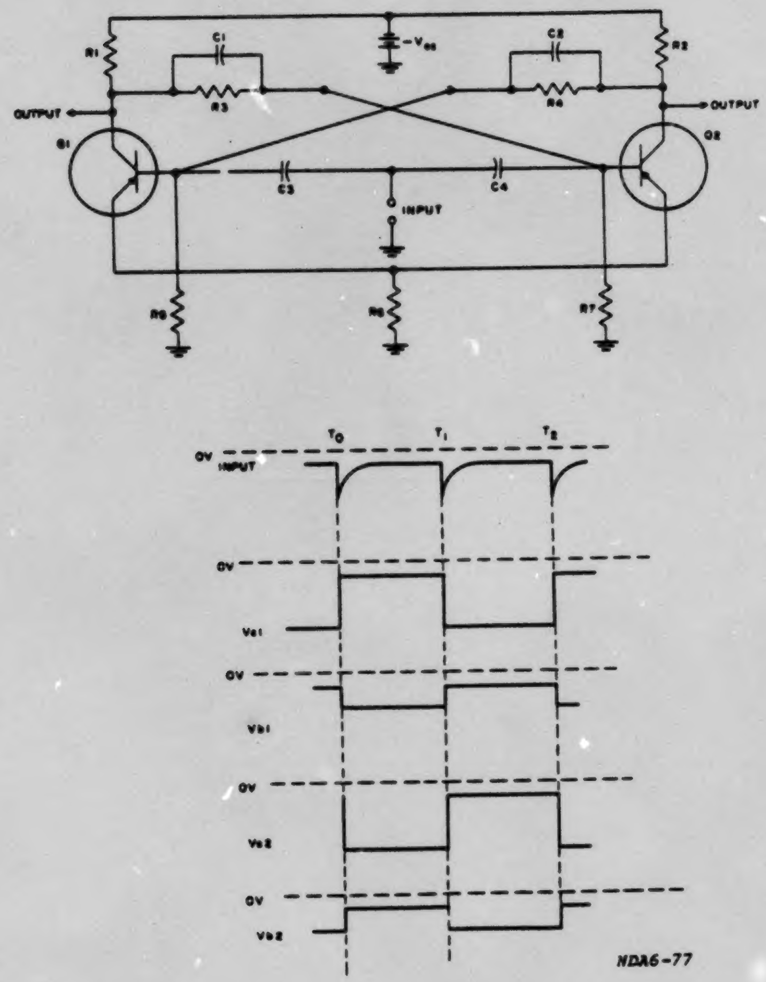

C1
-Vcc
C2
R1
R2
R3
R4
OUTPUT
OUTPUT
Q1
Q2
C3
C4
INPUT
R5
R6
R7
T0
T1
T2
0V
INPUT
0V
Vc1
0V
Vb1
0V
Vc2
0V
Vb2
NDA6-77

Figure 4 for Volume Review Exercise Question 24

24. (029-030) Refer to VRE Figure 4. The circuit in the illustration is a

a. monostable multivibrator.
b. Miller integrator.
c. single-shot multivibrator.
d. bistable multivibrator.

25. (030-032) A neon indicator usually represents the output of

a. a flip-flop.
b. a NOR-gate.
c. an OR-gate.
d. an AND-gate.

26. (033) Three basic functions of Boolean algebra are

a. addition, subtraction, multiplication.
b. AND, OR, EXCLUSIVE OR.
c. ONE, ZERO, NOT.
d. AND, OR, NOT.

27. (033) Boolean algebra differs from algebra in that it

a. uses only two values.
b. is used by computers.
c. has two states, TRUE and HIGH.
d. can be used with a number of variables.

28. (037) In Boolean algebra, the writing of an equation for a logic diagram is begun by writing the output for

a. the total diagram.
b. the input gate or gates.
c. one branch from the output gate.
d. either the output or input gate (or gates).

29. (038) Which of the following is the basic reason for applying ordinary algebra theorems to Boolean algebra equations?

a. Complementation.
b. Logical addition.
c. Simplification.
d. Rearrangement.

30. (039) The basic purpose of the logic diagram is to

a. illustrate the interconnection of indicated circuits.
b. aid in the simplification of the Boolean equation.
c. aid in construction of the truth table.
d. illustrate the Boolean equation.

31. (040) The output of a logic circuit is an electrical signal which represents a

a. logical conclusion.
b. complement.
c. 0.
d. 1.

32. (043) In computer terminology, a HIGH is always

a. true.
b. equal to ONE.
c. the more positive voltage.
d. subject to change with positive or negative logic.

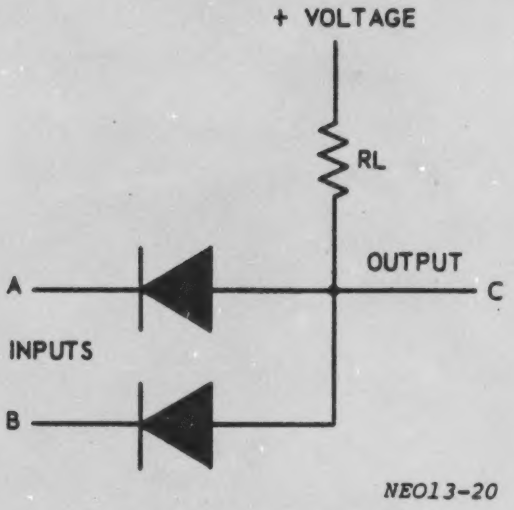


Figure 5 for Volume Review Exercise Question 33.

33. (043-044) Refer to VRE Figure 5. The Boolean equation for this circuit is

a. $\overline{AB} = \overline{C}$.	c. $\overline{A} + \overline{B} = \overline{C}$.
b. $A + B = C$.	d. $\overline{A}\,\overline{B} = C$.

34. (044) The small circle at the input to any symbol indicates a

a. relatively LOW is required to activate the circuit.
b. HIGH is required in negative logic.
c. LOW required in positive logic only.
d. signal must be noted.

35. (048) The Boolean equation for a three input negative AND-gate is

a. $A + B + C = D$.	c. $AB = C$.
b. $A + BC = D$.	d. $ABC = D$.

36. (049) An OR-gate whose output signal is inverted with respect to the input signal is

a. a NOR circuit.	c. an EXCLUSIVE OR circuit.
b. A NAND circuit.	d. an INCLUSIVE OR circuit.

37. (054) What is the basic circuit used in most counters?

a. Schmitt trigger.	c. Eccles-Jordan bistable multivibrator.
b. EXCLUSIVE OR.	d. Monostable multivibrator.

38. (055-056) In a four-stage serial up-counter made up of flip-flops A, B, C, and D with F/F-A as the LSD,

a. flip-flop C changes state on every other input pulse.
b. flip-flop C changes state when flip-flop B changes from the one to the zero state.
c. flip-flop B changes state when flip-flop A changes from the zero to the one state.
d. flip-flop D changes state when flip-flop C changes state.

39. (055) In an up-counter, the output from each F/F is taken off

a. the one side.
b. the zero side.
c. both one and zero side.
d. reset side.

40. (059) What is a disadvantage of connecting too many flip-flops in series?

a. A count may be missed when the flip-flops are changing states.
b. It would involve too much wiring.
c. Short propagation time.
d. Delay in operation.

41. (059) As opposed to serial counters, parallel counters

a. use less circuitry.
b. consume more power.
c. use less wiring.
d. are slower.

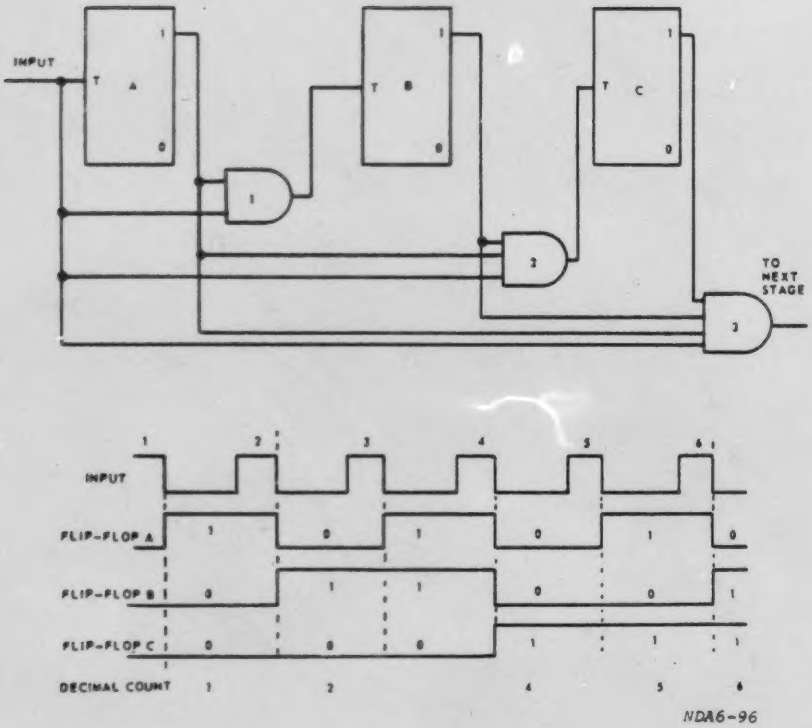

INPUT
T
A
1
0
T
B
1
0
T
C
1
0
1
2
3
TO NEXT STAGE
1
2
3
4
5
6
INPUT
FLIP-FLOP A
1
0
1
0
1
0
FLIP-FLOP B
0
1
1
0
0
1
FLIP-FLOP C
0
0
0
1
1
1
DECIMAL COUNT
1
2
4
5
6
NDA6-96

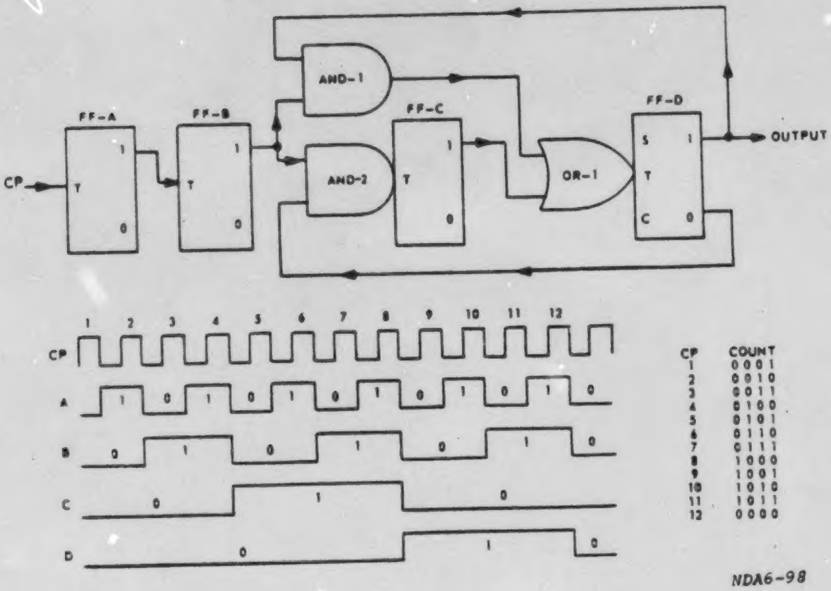
Figure 6 for Volume Review Exercise Question 42

42. (059) Refer to VRE Figure 6. The conditioning levels to activate AND-gate 3 are

a. F/F-A set, F/F-B reset, F/F-C set.	c. F/F-A set, F/F-B set, F/F-C set.
b. F/F-A reset, F/F-B set, F/F-C reset.	d. F/F-A set, F/F-B set, F/F-C reset.

43. (061) A four-stage up-counter contains a binary count of $1101_{(2)}$. What count is in the counter after five additional pulses?

a. 0000.	c. 1111.
b. 0001.	d. 0010.



CP	COUNT
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	0000

NDA6-98

Figure 7 for Volume Review Exercise Question 44

44. (061-062) Refer to VRE Figure 7. Which gate(s) block(s) counts of 13, 14, and 15 to make this a modulus 12 counter?

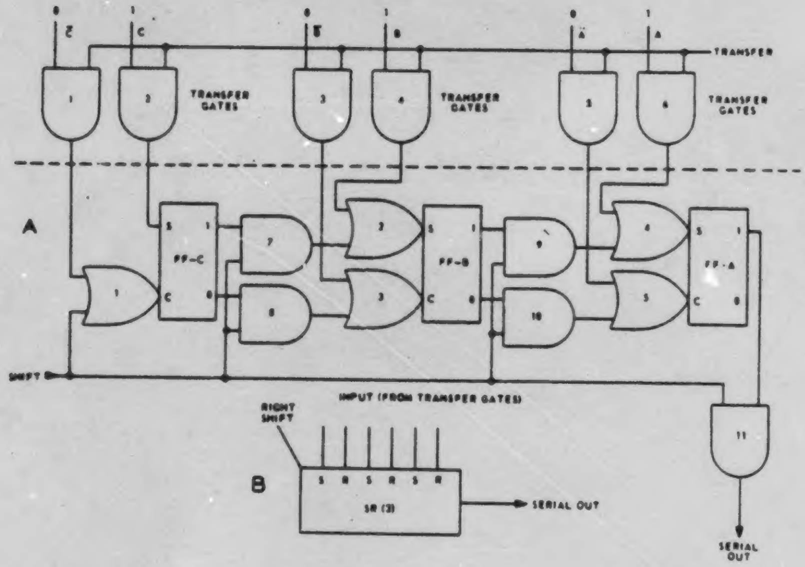
a. OR-1.
b. AND-1.
c. AND-2.
d. AND-1 and AND-2.

45. (063) In a four-stage mod-10 counter (count blocking), what would be the count in the counter after 13 clock pulses?

a. 0.
b. 1.
c. 2.
d. 3.

46. (066) Which of the following is a function of a storage register?

a. Temporary storage of multiple units of information.
b. Conversion of binary data to octal data.
c. Temporary storage of one unit of information.
d. Conversion of octal data to binary data.


TRANSFER
TRANSFER GATES
TRANSFER GATES
TRANSFER GATES
A
FF-C
FF-B
FF-A
SHIFT
INPUT (FROM TRANSFER GATES)
RIGHT SHIFT
B
SR (3)
SERIAL OUT
SERIAL OUT

NDA6-103

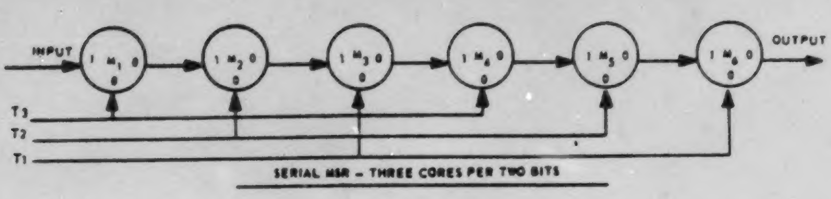
Figure 8 for Volume Review Exercise Question 47

47. (068-069) Refer to VRE Figure 8. With a binary configuration of 101 at the transfer gate inputs, which of the following is true?

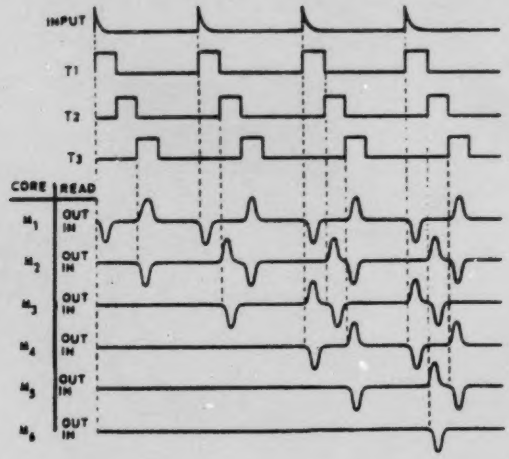
   a. Transfer gate inputs A, B, and $\overline{C}$ are high.
   b. Transfer gate inputs A, $\overline{B}$, and C are high.
   c. Transfer gate inputs $\overline{A}$, $\overline{B}$, and C are high.
   d. Transfer gate inputs A, $\overline{B}$, and $\overline{C}$ are high.

48. (068-069) What type of storage register is usually used to transfer data to a telephone line?

   a. Serial-in/parallel-out register.
   b. Serial-in/serial-out register.
   c. Parallel-in/parallel-out register.
   d. Parallel-in/serial-out register.


INPUT
1 M1 0
1 M2 0
1 M3 0
1 M4 0
1 M5 0
1 M6 0
OUTPUT
T3
T2
T1

SERIAL MSR – THREE CORES PER TWO BITS


INPUT
T1
T2
T3
CORE
READ
M1
M2
M3
M4
M5
M6
OUT
IN

NDA6-108

Figure 9 for Volume Review Exercise Question 49

49. (073-074) Refer to VRE Figure 9. What is the configuration of the register when it is full?

a. 011011.
b. 100100.
c. 111111.
d. 110110.

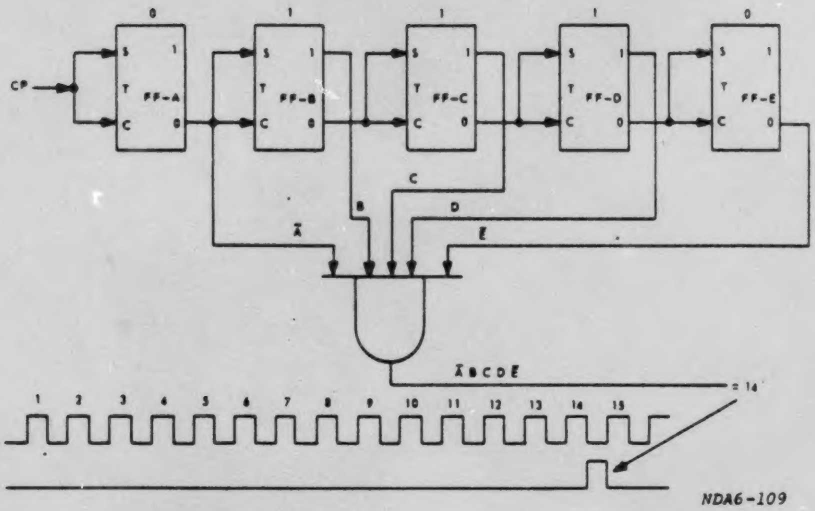


Figure 10 for Volume Review Exercise Question 50

50. (075) Refer to VRE Figure 10. What count is detected by the circuit?

a. 01101.	c. 10000.
b. 01110.	d. 10001.

51. (078-079) A resistive ladder digital-to-analog converter is connected to a six-stage counter, and the voltage applied to the ladder is 126 volts. What is the output voltage of the network when the count in the counter is 47?

a. 95.	c. 102.
b. 94.	d. 101.

52. (080) An encoder is most commonly found at the

a. input to a computer.	c. input to a card reader.
b. output to a computer.	d. output of a card reader.

53. (084) Control voltages are transferred from the control unit to

a. all units.	c. the storage unit.
b. the input unit.	d. the arithmetic unit.

54. (084) Three basic units *normally* located in the computer main frame are

a. input, control, and memory.	c. control, memory, and arithmetic units.
b. input, output, and control units.	d. control, memory, and input/output units.

55. (085) Data most likely to be stored in main memory would be

a. instructions and input data.
b. reference and variable data.
c. reference data and instructions.
d. data to be processed and reference data.

56. (086) In real-time applications of a digital computer, a fast access time is essential to the

a. input unit.
b. output unit.
c. control unit.
d. storage unit.

57. (086) Two important requirements of memory are

a. low capacity and high access time.
b. large capacity and low access time.
c. nonvolatile and rugged construction.
d. ferromagnetic core and high capacity.

58. (089) Two disadvantages of the delay line memory are

a. temperature stability and long delay.
b. the adjustments and standing waves.
c. energy loss and construction cost.
d. access time and volatile storage.

59. (089) A magnetic core makes a good bistable device for storing binary information because it

a. has low retentivity.
b. has a slow switching time.
c. can be magnetized in either of two directions.
d. takes two half-currents to change its state.

60. (089) The memory *least* likely to lose data during a power failure would be the

a. volatile memory.
b. delay line memory.
c. solid-state memory.
d. magnetic core memory.

61. (090) If a ferrite core memory is in the ONE state, and a second ONE is written in the core, the flux will

a. remain the same.
b. increase to maximum.
c. increase to a point just below maximum.
d. increase to maximum and return to the residual point.

62. (090-091) When a Y line in a core memory plane is selected, it will supply

a. all cores with half-current.
b. only one core per plane with half-current.
c. only the cores through which it passes with half-current.
d. only the cores through which it passes on the selected plane with half-current.

63. (090-093) A 4^2 ferrite core memory array has

a one sense winding and one amplifier.
b. one sense amplifier and one sense line per plane.
c. one sense amplifier and four sense lines per plane.
d. four sense amplifiers and 16 sense windings per plane.

64. (093) The process of putting information into a storage location is referred to as

a. writing ONEs.
b. a memory cycle.
c. a program cycle.
d. executing address.

65. (098) The solid-state RAM is addressed by

a. bit and word lines.
b. X and Y lines and no current drivers.
c. X and Y lines and current drivers.
d. current drivers and bit and word lines.

66. (098) One advantage of the solid-state RAM is

a. size.
b. high-bit capacity.
c. small current drivers.
d. small sense amplifiers.

67. (099) To program a solid-state ROM, the first step is to

a. clear all locations.
b. construct a truth table.
c. set all locations to ZERO.
d. apply an excessive current or voltage.

68. (100) The computer main frame unit that performs most logical operations is the

a. control unit.
b. memory unit.
c. program unit.
d. arithmetic unit.

69. (102) Data from memory is received in the arithmetic unit by the

a. X register.
b. accumulator.
c. M-Q register.
d. adding register.

70. (106) The computer unit which determines the sequence of operations within the computer is the

a. control unit.
b. arithmetic unit.
c. input/output unit.
d. message selection unit.

71. (108) A high-speed computer would most likely use

a. synchronous control.
b. asynchronous control.
c. a fixed clock and jump program.
d. synchronous clock and hexadecimal counters.

72. (114) In I/O components, the device which decreases computer waiting time is the

a. printer.
b. transmitter.
c. keyboard.
d. buffer.

73. (116) What is the primary advantage of tape storage over internal computer storage?

a. Speed.
b. Cost.
c. Access time.
d. Large capacity.

74. (117) In reference to magnetic tape reading, what is the advantage of having a two-gap head as opposed to a one-gap head?

a. It decreases the hysteresis loss.
b. It can read data immediately after it is written.
c. It makes reading easier.
d. It induces smaller pulses in the head.

75. (119) A complete card-handling system includes

a. tape unit, card punch, and card reader.
b. tape unit, keyboard, and card reader.
c. card punch, card reader, and printer.
d. printer, card punch, and keyboard.

76. (120) Punched cards which are to be used with mechanical computing equipment are coded in

a. Hollerith code.
b. gray code.
c. binary code.
d. decimal code.

77. (122) Which of the following is the reason some card readers have two sets of reading brushes?

a. In case one set fails to function, the other set can take over.
b. To check the validity of the reading process.
c. To permit faster reading.
d. One is used to stack cards.

78. (122) As an input device, the keyboard can function as

a. a parity generator.
b. an analog-to-digital converter.
c. a digital encoder.
d. a digital decoder.

79. (125) The tilt latches on a computer keyboard act as mechanical

a. adders.
b. links.
c. stops.
d. subtractors.

80. (127) In the computer keyboard, what determines the character to be printed?

a. Cycle clutch release lug.
b. Position of the cycle shaft.
c. Position of the filter shaft.
d. Presence or absence of the interposer lugs.

81. (130) In the impact printer, providing pulses that are synchronized to the rows of characters on the print roll is a function of the

a. character pulse generator.
b. synchronizing pulse generator.
c. electronic distributor.
d. storage matrix.

82. (130) In an impact printer, what is the primary function of the electronic distributor during the print cycle?

    a. To produce pulses that are synchronized to the rows of characters on the print roll.
    b. To produce a pulse that generates the paper-feed mechanism.
    c. To initiate the first timing pulse.
    d. To channel individual pulses into separate lines that connect to the storage matrix.

83. (133) When used as buffer storage, the magnetic drum is effectively

    a. a time buffer between high-speed equipment and the low-speed central processor.
    b. a timing generator for central processor.
    c. used to store information permanently.
    d. a time buffer between slow-speed equipment and the high-speed control processor.

84. (134) Magnetic drum head adjustment must be performed when the drum is

    a. at operating temperature.
    b. in low-speed operation.
    c. not running and cold.
    d. running at not more than 150 RPM.

85. (136) Random addressing of a magnetic drum means

    a. the system provides access to addresses in sequence.
    b. the system provides access to an address without regard to sequence.
    c. combination read-write heads must be used.
    d. separate read-write heads must be used.

86. (140) A disk pack with 13 disks would have

    a. 11 recording surfaces.
    b. 13 recording surfaces.
    c. 24 recording surfaces.
    d. 20 recording surfaces.

87. (144) What is the primary function of a surge resistor in a rectifier circuit?

    a. To protect the input transformer.
    b. To provide filtering in the output.
    c. To limit the peak current through the rectifying device.
    d. To increase the peak current through the rectifying device.

88. (145) A simple half-wave rectifier normally provides a

    a. high current and low-voltage output.
    b. high current and high-voltage output.
    c. low current and low-voltage output.
    d. low current and high-voltage output.

89. (147) The ripple frequency of a basic full-wave rectifier is

    a. equal to the input frequency.
    b. twice the input frequency.
    c. three times the input frequency.
    d. four times the input frequency.

90. (148) The main advantage of a full-wave bridge-type rectifier is that it

a. has high current and low voltage.
b. has low voltage and low current.
c. is center tapped for better rectification.
d. does not have a center-tapped transformer.

91. (152-153) When an inductor is used for filtering the output of a rectifier circuit, it

a. is connected in series with the load.
b. is connected in parallel with the load.
c. offers a low impedance to the AC component.
d. offers a high impedance to the DC component.

92. (154) A capacitor-input filter in a rectifier circuit normally provides a

a. high-output voltage at low-current drain.
b. low-output voltage at low-current drain.
c. high-output voltage at high-current drain.
d. low-output voltage at medium-current drain.

93. (153) One advantage of the RC filter is that

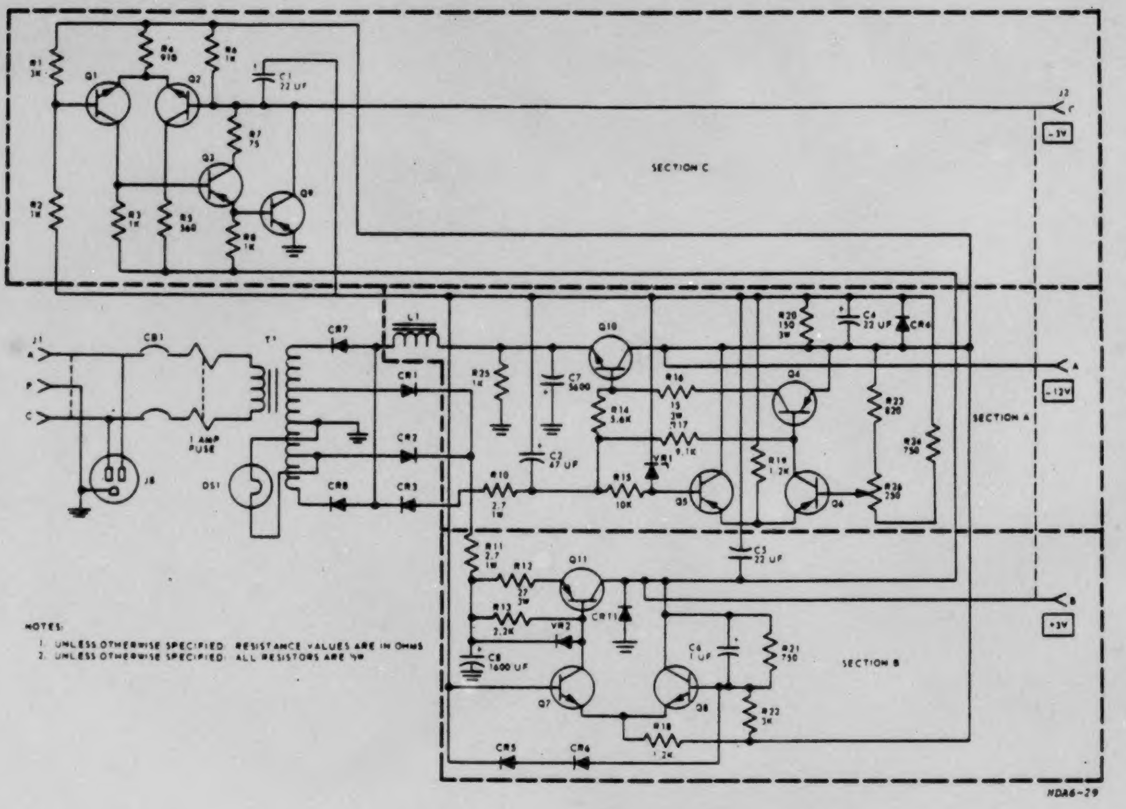
a. the resistor offers the same impedance to the DC voltage as to the AC voltage.
b. current flow through the resistor causes power to be dissipated in the form of heat.
c. it is compact in size.
d. the resistor offers better voltage regulation than a choke.

94. (157) One advantage of a shunt voltage regulator is

a. its small-load efficiency.
b. that it wastes very little power with small loads.
c. that it is self-protecting against shorts or overloads.
d. that the output power is divided between the load and the shunting circuit.

95. (158) In a DC power supply, a series voltage regulator is often used because of its

a. high-load efficiency.
b. small-load efficiency.
c. self-protecting capability against shorts or overloads.
d. current limiting capability.


R1 3K
R4 910
R6 1K
C1 22 UF
Q1
Q2
R7 75
Q3
Q9
R2 1K
R3 1K
R5 560
R8 1K
SECTION C
J2
C
-3V
J1
A
P
C
CB1
1 AMP FUSE
T1
J8
DS1
CR7
L1
CR1
CR2
CR8
CR3
R25 1K
C7 5600
C2 47 UF
R10 2.7 1W
Q10
R14 5.6K
R16 15 3W
R17 9.1K
VR1
R15 10K
Q5
Q4
R19 1.2K
Q6
R20 150 3W
C4 22 UF
CR4
R23 820
R24 750
R26 250
A
-12V
SECTION A
C3 22 UF
R11 2.7 1W
R12 27 3W
R13 2.2K
VR2
Q11
CR11
C8 1600 UF
Q7
Q8
C6 1 UF
R21 750
R22 3K
R18 1.2K
CR5
CR6
B
+3V
SECTION B
NDA6-29

NOTES:
1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS
2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE ½W

Figure 11 for Volume Review Exercise Question 96 and 97

96. (159-160) Refer to VRE Figure 11. The AC voltage from the secondary of T1 is

a. filtered by L1 and R25.
b. is regulated by Q10 and C7.
c. full-wave rectified by diodes CR7 and CR8.
d. full-wave rectified by diodes CR3 and CR7.

97. (161) Refer to VRE Figure 11. Transistors Q7 and Q8 form a part of a

a. series regulator.
b. differential amplifier.
c. voltage divider network.
d. filter network for the +3V power supply.

98. (162) An open-circuited rectifier in a single-phase half-wave rectifier circuit will cause

a. no output voltage.
b. increased AC ripple voltage.
c. increased DC output voltage.
d. no effect on the output voltage.

99. (162) A 60-Hz ripple frequency from a single-phase full-wave rectifier unit indicates

a. no trouble with the unit.
b. a zener diode is weak.
c. a rectifier diode is defective.
d. a voltage increase.

100. (163) In solid-state devices, the prefix for a metallic rectifier number is

a. MR or SR.
b. IN.
c. Z.
d. Hz or Mz.

Preface

THIS SECOND VOLUME of CDC 30554, *Electronic Computer Systems Repairman*, includes analysis of the tasks of operational performance checking, adjustments, alignments, programming, and troubleshooting. During each study, the analysis exposes the requirements to identify all aspects or parts of each task, and explains how to place these parts in their proper positions.

The explanations provided in the studies about the different parts of a computer system are designed to show that the task is used many times in many places. It also explains that the principle of the task is the same even though its application may be different. Your objective in each case is to correlate the principles with various applications explained in the text, and then to relate these studies to your present duty assignment and computer.

For your convenience in studying this volume we have placed in the workbook figures and a chart to which there is extended or frequent reference. Also an index to key elements has been included in this volume for quick reference.

If you have questions on the accuracy or currency of the subject matter of this text, or recommendations for its improvement, send them to: Tech Tng Cen (TTOC), Keesler AFB, MS 39534.

If you have questions on course enrollment or administration, or on any of ECI's instructional aids (Your Key to Career Development, Study Reference Guides, Chapter Review Exercises, Volume Review Exercise, and Course Examination), consult your education officer, training officer, or NCO, as appropriate. If he can't answer your questions, send them to ECI, Gunter AFB, AL 36118, preferably on ECI Form 17, Student Request for Assistance.

This volume is valued at 33 hours (11 points).

Material in this volume is technically accurate, adequate, and current as of March 1972.

Contents

Page

Preface ... *iii*

Chapter

1 Performance Checks ... 1

2 Adjustments ... 20

3 Alignments ... 39

4 Programming ... 62

5 Troubleshooting ... 75

Index ... 99

412

Performance Checks

THIS CHAPTER presents an analysis of tasks associated with the performance of checks on equipment operation. Reliability of equipment, as we are learning, is becoming better. Components are being manufactured with greater skill because of major breakthroughs in engineering. The adoption of solid-state devices, using crystal structures, silicons and quartz, thin films, and doping, together with the techniques used in the manufacturing of these devices, have led to the development of maintenance techniques which you must understand so you can maintain the equipment properly. Early maintenance techniques which were applicable but which have been deemphasized or eliminated are:

- Checking the equipment frequently to discover weak links.
- Aligning the circuits on a close interval basis even though no indications of malalignment exist.
- Checking the operational capability by excessive substitution of test problems.
- Interrupting the power stability with marginal checks, power run down and up, and conversion to other power units, to name a few.

2. These practices led to the following problems:

- Decrease in operational availability.
- Increase in chance for human error, such as shorting components.
- Great temperature variations in environmentally controlled cabinets.
- Just plain tinkering.

3. However, these maintenance techniques did have their good points. The primary ones were that training was maintained at a fairly high level and engineering data of significant value was collected on MDC documentation. Analysis of this data resulted in the present concept which, as we stated, is elimination of all but essential maintenance tasks. We covered the service tasks in Chapter 2 of Volume 1. Here we are more concerned with the operational tasks, which are the tasks related to data movement.

4. Operational/performance checks are performed by various methods. Some of these methods are:

- With various meters.
- With an oscilloscope.
- By use of display CRTs.
- By use of printouts.
- By interpretation of lamps, audio alarms, and internal tests.
- By visual examination of mechanical assemblies.

5. A basic technical order series applies to this type of task. This TO is the preventive maintenance TO, the -WC6 series technical order. The phase period of the task may range from daily to annually. The time interval is based upon statistical data accumulated through MDC and engineering data.

6. During the analysis of tasks related to performance:

- Preferred methods of doing the task are identified.
- The reason that a check is made at certain specific points in equipment is determined.
- Technical data about the task or circuit being tested is examined.

7. To make this text more meaningful, the tasks which are analyzed are further identified as pertaining to:

- System input (I).
- Output (O).
- Both (I/O).
- System central (C).

In the following discussion, these alpha characters identify the unit in which the task will likely be found. But first we shall look at some of the sources of data we will be checking.

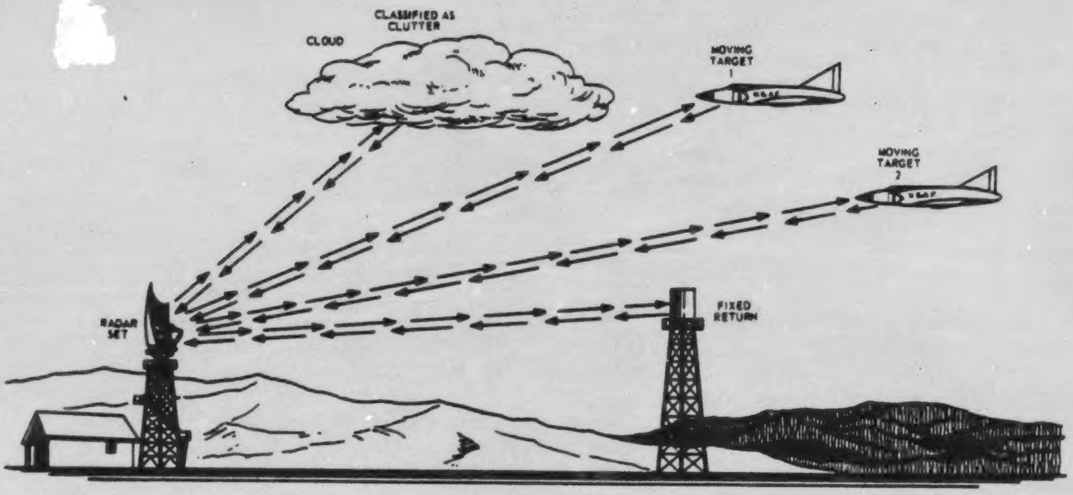


Figure 1. Radar.

1. Sources of Data Affecting Operational Checks

1-1. In this section we identify most of the sources which supply data to a computer weapons system. Their principal use is defined. Their operational checks are centered around the use of the data and its input circuitry. The first of these sources is radar and beacon.

1-2. Radar and Beacon. The operational checks normally associated with this type of system input require the use of hands-on methods and test equipment. These tasks must determine the validity of the return and the quality and accuracy of the return. What return? Let's examine a few of the basic principles of radar and beacon so that we can appreciate why operational checks are needed and performed. *Radar* means *radio direction and ranging* and came into being during World War II (1939-1945). Its concepts are related to an echo in sound. When you have heard your voice echo back to you, the delayed response of your voice repeated your original statement. The echo is called the *return*. The delay encountered is measurable in time and distance. Since sound waves travel at 1100 feet per second, and since the time you say a word until it comes back as an echo return is measurable, the distance to the resounding backdrop, usually a cliff, can be determined.

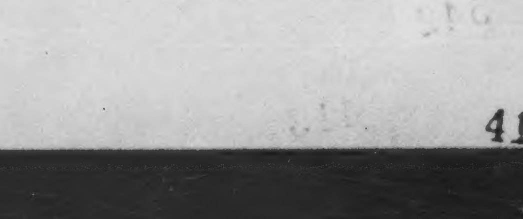


Figure 2. Radar return.

1-3. *Radio wave reflection.* All radar sets work on a principle very much like that described for sound waves. In radar sets, however, a radio wave or signal of an extremely-high frequency is used instead of a sound wave. The words *wave* and *signal* have the same meaning. The energy sent out by a radar set is similar to that sent out by an ordinary radio transmitter. The radar set, however, has one outstanding difference in that it picks up its own signals. It transmits a short pulse, and receives its echoes, then transmits another pulse and receives its echoes. This out-and-back cycle is repeated from 60 to 4000 times per second, depending upon the design of the set. If the outgoing signal is sent into clear space, no energy is reflected back to the receiver. The signal and the energy which it carries simply travel out into space and are lost for all practical purposes.

1-4. By referring to figures 1 and 2, you can see that if the signal strikes an object such as an airplane, a ship, a building, or a hill, some of the energy is sent back as a reflected signal. If the object is a good conductor of electricity and is large, a strong echo is returned to the antenna. If the object is a poor conductor or is small, the reflected energy is small and the echo is weak.

1-5. Radio waves/signals travel in straight lines at a speed of approximately 186,000 (light) miles per second as compared to 1100 feet per second for sound waves. Accordingly, there is an extremely short time interval between the sending of the pulse and the reception of its echo. It is possible to measure the interval of elapsed time between the transmitted and received pulse with great accuracy—even to one ten-millionth of a second.

1-6. The directional antennas used by radar transmit and receive the energy in a more or less sharply defined beam. Therefore, when a signal is picked up, the antenna can be rotated until the received signal is maximum. The direction of the target is then determined by the position of the antenna.

1-7. The radar return is fed to the input unit of certain electronic data processors in the forms of raw or normal video and processed video after each has been amplified by the radar receiver. The returns may be raw/normal video or processed video. Raw or normal video is that type of return which is merely amplified along with the noise returns. Processed video, however, may be in various forms. One such form is MTI (moving target indicator) video. This form is obtained by measuring a return with the last return for the same target and, if the return shows a change in position (representing velocity), the circuit performing the comparison generates a pulse. Another type of processed video is MLI (main lobe indicator) video. This type of presentation is generated by a circuit which processes the strongest return from a target (main lobe) and suppresses the weaker returns (side lobes) from the same target. Then there are other types of video which are processed to be used in jamming situations and to eliminate clutter such as clouds and electrical disturbances.

1-8. *Beacon.* Just as radar scans the skies for aircraft, beacon scans the skies for aircraft which are fitted with transmitters or transponders, as they are called, which transmit coded beacon replies to ground stations. Where radar only locates an object in the sky, beacon, through its processing, is capable of identifying what type of aircraft is in the sky. These aircraft may be friend or foe. They may be civilian airlines fitted with IFF (identification, friend of foe) transmitters which allow ground stations to identify them, or they may be military aircraft or missiles fitted with SIF (selective identification feature) transmitters which allow ground stations to identify which type of military aircraft is in the air.

1-9. Beacon replies differ from radar returns. In beacon, a pair of pulses (bracket) are generated 20.3 μsec apart. Between these two pulses is room for 13 additional pulses, and these pulses are formed into codes. To help you distinguish which type of beacon reply your equipment is processing, the term MODE is used. Each mode is associated with particular types of replies such as IFF, SIF, or special military codes. Each return or reply is stored within a half-mile range block in memory. Since a code is bracketed, a detection circuit must be designed to sample the first and last (15th) pulse and the intervening pulses must be temporarily stored. To do this effectively, a delay line in conjunction with an AND gate is used (refer to fig. 3). With detection of both the first and last pulse a parallel shift is generated, causing data bits 2 through 13 and parity bit 14 to be loaded into a decoder unit.

1-10. *Height-finder returns.* Although we have not discussed height-finder radar returns, data acquisition systems employ this type of radar. The returns are similar to search video, and the processing and amplification of returns are similar to those described in Chapters 2 and 3, of this text. Therefore, operational/performance checks usually are the same. Now let's examine another part of radar where we must be concerned with operational checks.

1-11. **Radar Antenna.** Search radar and beacon radar usually scan the skies by rotating an antenna assembly upon a fixed pedestal. Height-finder radars usually scan the skies by having the antenna nod up and down in much the same way that you shake your head when you agree with a statement. The height-finder radar also is capable of horizontal movement, but this movement is usually controlled and exercised only upon demand of an operator or automatic machine operation.

1-12. *Determining proper orientation of radar rotation.* This means "Does the radar always maintain its proper orientation with respect to north?" To obtain this answer, an automatic change pulse (ACP) counter is inserted in data processors which counts ACPs from the time that a main pulse labeled NORTH pulse is received. Many search radars use this north pulse as an orientation signal and, when the radar personnel orient the radar to north, the pulse is allowed to be generated. Since the pulse is generated at

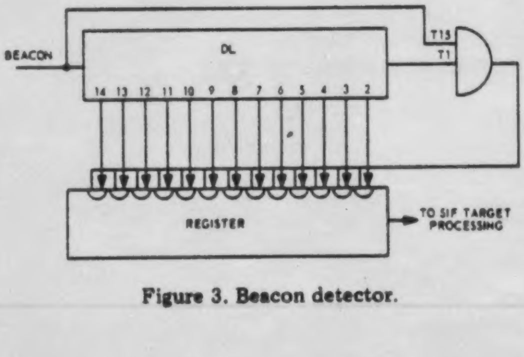


Figure 3. Beacon detector.

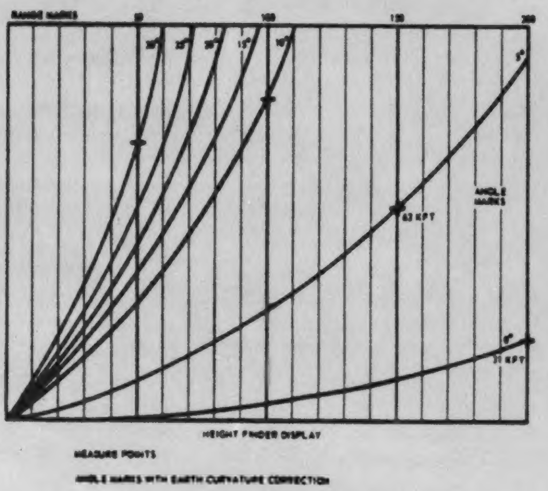


Figure 4. Height-finder angle mark display.

north, it may be at *true north* or *magnetic north*. The EDP may use either north direction for determining position; therefore, an ACP counter is installed to count the positional changes of a search radar starting with north pulses. The increment of change is often established at .088° per change and a total of 4096 pulses equals one revolution of a radar antenna scan. The increments may be larger or smaller depending upon circuit design and antenna rotation speed. The operational check is to measure the output of the counter with *north* mark pulse for coincidence. If coincidence does not occur, a problem may be identified. If the EDP uses *true north* and the radar uses *magnetic north* as references, then a preset number of ACPs equivalent to the angular difference between true and magnetic north must be programmed into the ACP counter. Either a switch or a series of switches will provide this capability.

1-13. *Determining proper orientation of height-finder nod.* This means you must perform a check, usually with an oscilloscope at the input unit, which determines that the nod voltage change is the proper amplitude, phase, and angle, and that it is coincident with the nod positions at, for instance, 0°, 5°, 10°, and 30°. Radar personnel will provide certain signals to your system which will aid you. A circuit in the radar generates a pulse each time that the antenna increases or decreases its nod by 5°. This signal is called "*angle mark.*" Its occurrence, through circuit design and compensation circuit variations, is measurable at selected ranges and altitudes. For instance (refer to fig. 4), if the angle mark at 0° with earth curvature correction (ECC) does not intersect the 200-mile range mark at 31,000 feet, plus or minus a specified amount, then operationally the system is malfunctioning and alignment is required. If coincidence occurs at some points but not at others, nonlinearity is evident and alignment is required. In the operational checks of these areas, data processing system and radar positioning are examined and, if errors are discovered, then alignment must be performed.

1-14. **Keyboards.** A keyboard is basically a typewriter with a digital encoder attached that converts the action of depressing a key to a digital code. By this means it is possible to insert data into a digital machine in its language—digital code. In this case, the keyboard and its encoder function as an interpreter between man and machine. Figure 5 shows the function of a typical keyboard when it is used as an input device. Each time that a key is depressed, an 8-bit binary code is inserted into the transmitter. The transmitter converts this parallel data to a serial message that is transmitted over a telephone line. At the other end, a receiver converts the serial data back to parallel and applies it to a printer. The printer decodes the digital data and prints out the character that was inserted by the keyboard.

1-15. Notice that there are eight parallel lines leading from the keyboard to the transmitter and that each line shows a voltage level that represents a ZERO or a ONE. Also notice that each line is labeled with a bit number (DO through D7). The binary configuration generated in this example is:

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	1	0
Parity bit	Control bit			Character Code			

1-16. This Fieldata code is used with the Strategic Air Command Communications System (SACCS). It uses an 8-bit binary number to represent letters, numbers, punctuation marks, and other selected symbols. To enable you to understand more of the keyboard operation, we shall explain it in terms of the code it generates.

1-17. Now let us see how the mechanical movement of a typewriter key produces an 8-bit binary code. Look at figure 6. There are eight 2-position switches mechanically connected to the typewriter. In the figure, it is assumed that the M key has been depressed. The mechanical analog-to-digital converter has positioned the switches so that their voltage outputs represent the binary code for the letter M. The voltage at the output of a switch is either - 12 volts (logic ONE) or 0 volt (logic

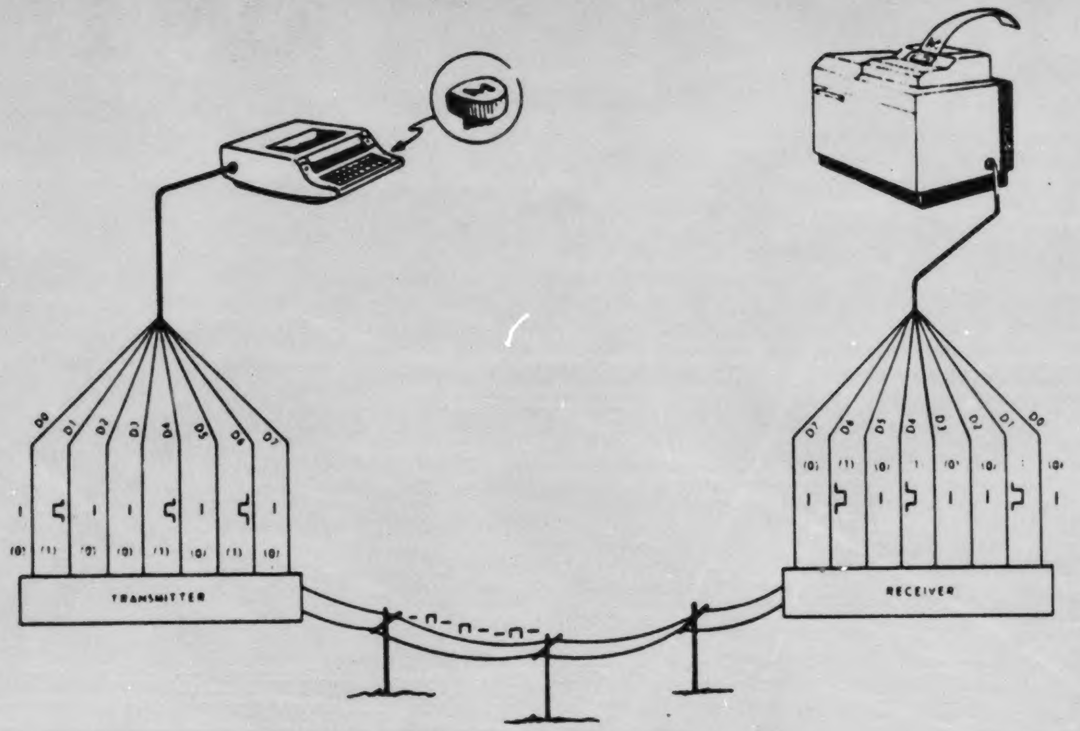

D0
D1
D2
D3
D4
D5
D6
D7
(0)
(1)
TRANSMITTER
RECEIVER

Figure 5. Keyboard operation.

ZERO). In figure 6, switches S1, S3, S4, S6, and S8 are switched to their 0-volt positions; therefore, the output code is D0—0 1 0 0 1 0 1 0—D7, which is the Fieldata code for M.

1-18. As the operator depresses each key, the keyboard prints each character just as a typewriter does and, at the same time, generates the Fieldata code. Operational accuracy requires that the letter "M" be typed on the paper by the letter "M" on the ball in the typewriter. If the character is not printed, the keyboard must be aligned or adjusted, and you must use appropriate technical order reference instructions to adjust or align the unit properly. If an incorrect Fieldata code is developed by the switches and/or electronic logic packages which are a part of the keyboard unit, very likely a parity error will be generated. Each parity error is visually indicated by a light. Backspacing will erase the Fieldata code, but will not correct the problem. Troubleshooting with special test equipment in an off-line mode (bench) is indicated.

1-19. Since the keyboard we are using in our example is used in SACCS, we might mention here that this keyboard is also used to write data onto magnetic tape. When programmed by an external control unit (fig. 7), the electronic package places the Fieldata code for each character onto the tape in the sequence in which it is typed. Operational checks of this keyboard also require that compatibility with the tape unit be checked. If data cannot be loaded properly, then the control signals fed to the machine, the timing of the machine, or the development of data from the machine may be incorrect, and corrective repair action is indicated.

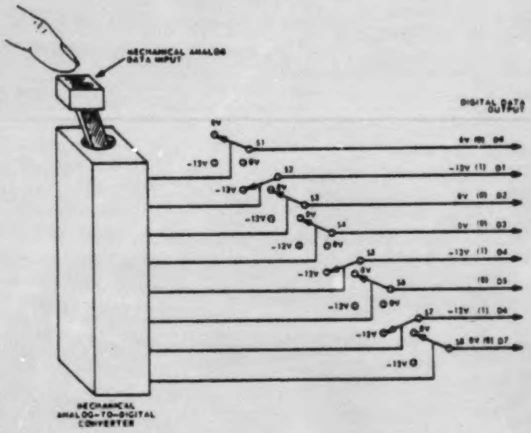
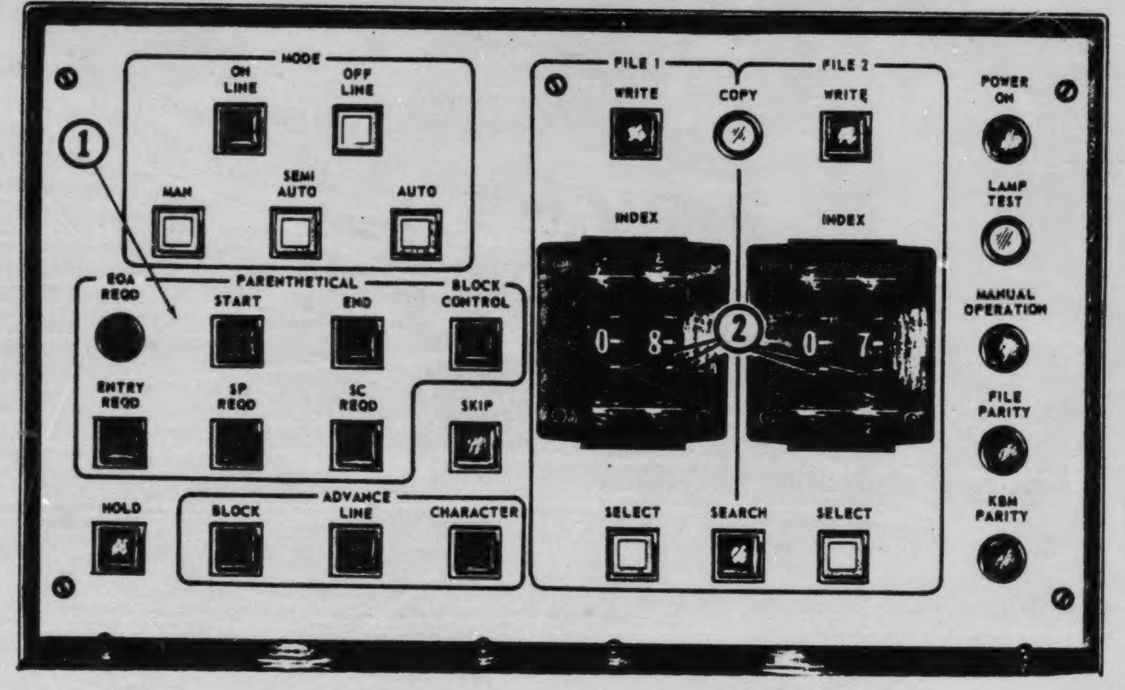

MECHANICAL ANALOG DATA INPUT
DIGITAL DATA OUTPUT
0V
S1
-12V
0V (0) D0
-12V (1) D1
0V (0) D2
0V (0) D3
-12V (1) D4
(0) D5
-12V (1) D6
S8 0V (0) D7
MECHANICAL ANALOG-TO-DIGITAL CONVERTER

Figure 6. Letter selection code.


MODE
ON LINE
OFF LINE
①
MAN
SEMI AUTO
AUTO
EOA REQD
PARENTHETICAL
START
END
BLOCK CONTROL
ENTRY REQD
SP REQD
SC REQD
SKIP
HOLD
ADVANCE
BLOCK
LINE
CHARACTER
FILE 1
FILE 2
WRITE
COPY
WRITE
INDEX
INDEX
0- 8-
②
0- 7-
SELECT
SEARCH
SELECT
POWER ON
LAMP TEST
MANUAL OPERATION
FILE PARITY
KBM PARITY

2 FILE SELECTION KNOBS

1 EOA = END OF ADDRESS
SP REQD = SEND PARTIAL REQUIRED
SC REQD = SEND COMPLETE REQUIRED

Figure 7. Control unit.

1-20. The keyboard is also used as an output device when checking the validity of program data on magnetic tape and the control of signals called for from the control panel. By selection of a file on the control panel with the selection knobs in callout ② (shown in fig. 7) and the command signal *search*, the keyboard will select the proper key through its electronic package and cause it to print. At such time in the printing of a program that a control signal from the operator is called for, the program stops and a control panel light lights (in callout ① area) identifying which operator action is called for. The operator completes the operation and the program continues. The final action on a message or program will be an operator action called *send complete* (SC REQD). This action provides the command signal to transmit.

1-21. **Tape Transport Units.** Let's briefly identify tape drive units and discover what we

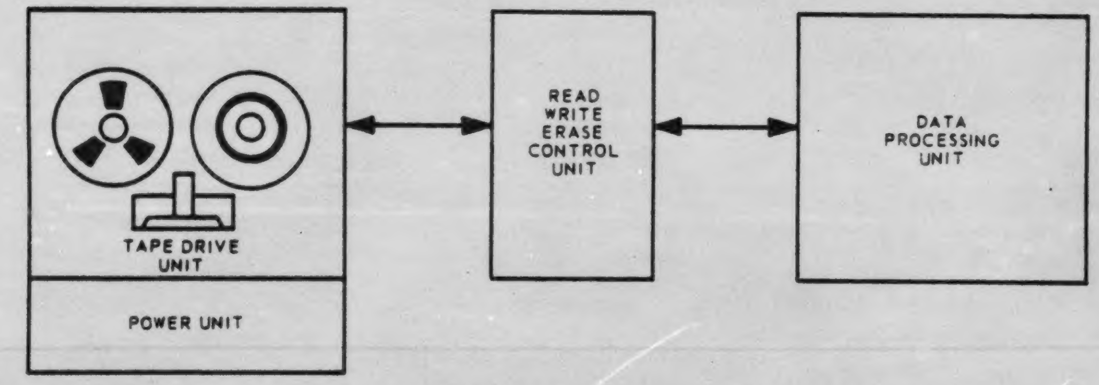

TAPE DRIVE UNIT
POWER UNIT
READ WRITE ERASE CONTROL UNIT
DATA PROCESSING UNIT

Figure 8. Block diagram, tape drive.

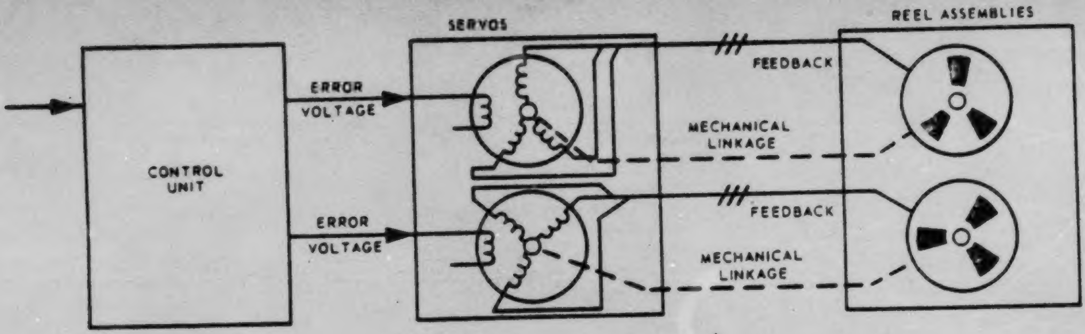

SERVOS
REEL ASSEMBLIES
CONTROL UNIT
ERROR VOLTAGE
ERROR VOLTAGE
FEEDBACK
MECHANICAL LINKAGE
FEEDBACK
MECHANICAL LINKAGE

Figure 9. Servo unit, tape drive.

should look for during operational checks. Refer to figure 8, the block diagram of a tape unit, and observe that the tape unit is usually an external part of a data processing system. This unit provides flexibility in the uses of the EDP because many fixed programs may be stored on individual tapes and may, at the discretion of the user, be inserted. The data and control functions are fed through and controlled by the interface unit between the data processor and tape drive unit. Some error checking may also be performed by the control unit.

1-22. Mechanically, the tape drive unit consists of two units to house the tape reel and takeup reel, servo units to control each reel assembly, a vacuum pump (on many models), photocells for tape orientation and control (on some models), and a motor drive unit and power supply unit. When the servos are supplied an electrical error voltage, they will cause the reel assemblies to rotate until the error voltage (induced voltage) is nulled. The rotation and velocity of the reel assembly are dependent upon the phase angle and magnitude of the applied error voltage. (For a detailed explanation of servo units, refer to the servo unit in the chapter on alignment.) Look at figure 9 and see that the servos do, in fact, control the reel assemblies and that external voltages in the form of error voltages provide the drive force necessary for tape movement. Now that we have briefly discussed some of the general characteristics of tape transport units and have seen how the unit is connected to the data processor, let's identify, in the next two paragraphs, some elements of the unit which are considered during the performance of operational checks.

1-23. *Mechanical and electrical elements:*

a. Servos.

b. Motors.

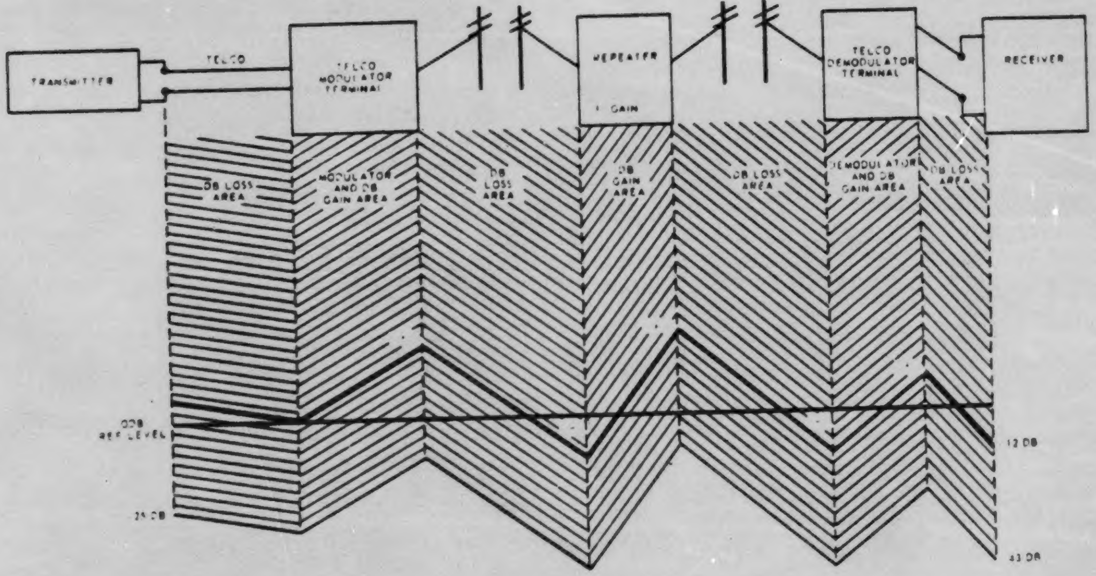

TRANSMITTER
TELCO
TELCO MODULATOR TERMINAL
REPEATER
GAIN
TELCO DEMODULATOR TERMINAL
RECEIVER
DB LOSS AREA
MODULATOR AND DB GAIN AREA
DB LOSS AREA
DB GAIN AREA
DB LOSS AREA
DEMODULATOR AND DB GAIN AREA
DB LOSS AREA
0DB REF LEVEL
25 DB
12 DB
43 DB

Figure 10. Repeater stations.

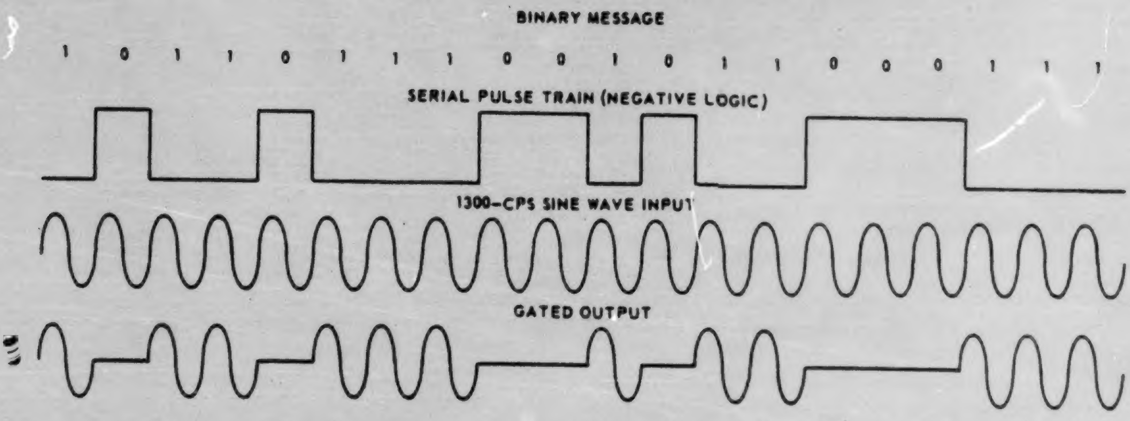


Figure 11. Dipole data.

c. Vacuum pump.
d. Reel assemblies.
e. Tape head positioning.
f. Photocell.
g. Voltages, currents.
h. Tape tension.

1-24. *Data flow elements:*
a. Read, write, and erase.
b. Control signals.
c. Diagnostics:
  (1) All ones check.
  (2) All zeros check.
  (3) Crosstalk check.

d. Reliability check between tape transport and data processor.

e. Error check circuits check.

1-25. The above listings point out each area in which an operational breakdown may occur. These areas are significant enough to have performance routines prepared and performed. Some may be daily, such as the diagnostic check, servo unit check, photocell check, or vacuum pump check; others may be scheduled as infrequently as every 180 days.

1-26. Transmission Line. This system input and output requires the use of indicators, meters, and switches. To aid in understanding why and how performance checks are performed in this area, let's first explore what is necessary in order for data to be transmitted and received. Then let's identify how the input/output equipment can sense the correctness of data and errors in data.

1-27. Whenever data is accumulated at a station, it may be of value to higher headquarters. That is why almost all command and control systems have data links. For the most part, these data links are conventional telephone (TELCO) lines or microwave units of a telephone company. In overseas areas and under tactical situations in the United States, Air Force personnel and equipment replace a commercial company.

1-28. Since data must be transmitted and received over these media, a problem arises in that any signal entered into a long wire loses power. The reason for this is that wire has resistance which impedes the flow of a signal. To compensate for this, refer to figure 10 and see that TELCO places repeater stations every 6 or 7 miles with capabilities of taking in a very small signal and boosting it to a high enough power rating to reach the next repeater station. The amplifiers in the repeater station are linear-type amplifiers with automatic frequency and gain controls built in. They can raise the power level of the output signal with no loss of signal data.

1-29. To get the data to a TELCO line properly, you may have a modulator or transmitter in your equipment. This unit prepares the digital data for the line. In one system, it may change the digital data to dipole data. Referring to figure 11, dipole data shows that a change of binary one of zero to 1 (1 0 1) in a message results in a change from a cycle pulse to a level to a cycle. Further examination of figure 11 shows that each binary one results in one cycle pulse. Another system currently in use uses *frequency shift keying* (FSK). This method (refer to fig. 12) uses two audio frequencies. A change in frequency represents a binary one. No change in frequency for successive time periods represents binary zeros.

1-30. *Line quality.* Selection of the bit rate of a message is determined by the quality of the local TELCO lines. If the noise levels, crosstalk, or other factors related to audio transmission cause the line quality to be low,

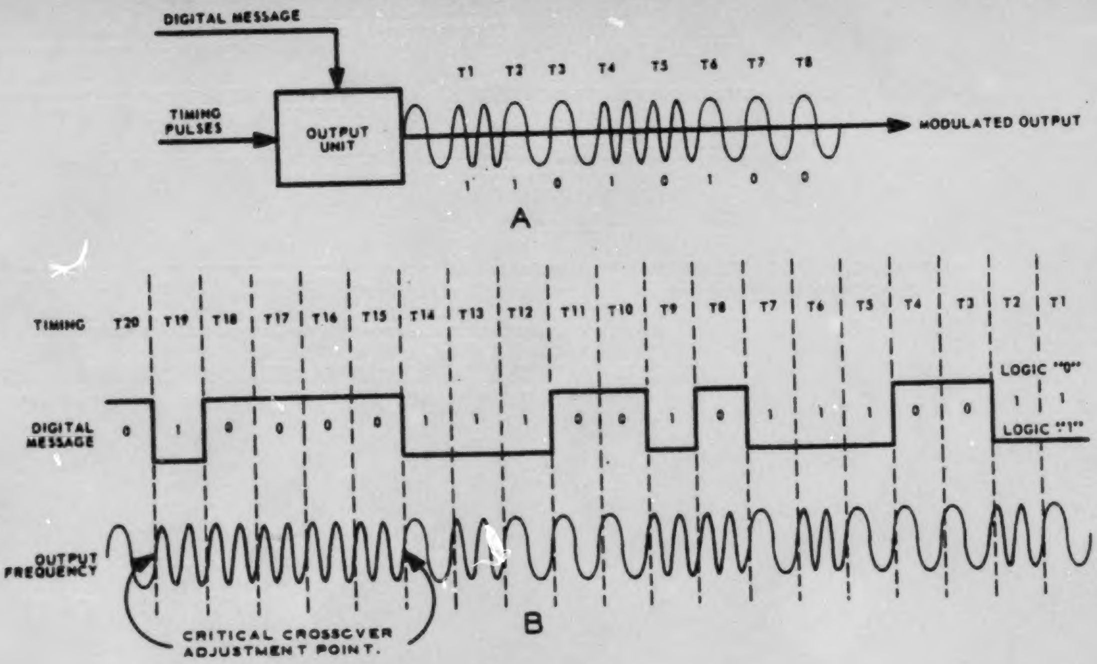

DIGITAL MESSAGE
TIMING PULSES
OUTPUT UNIT
T1 T2 T3 T4 T5 T6 T7 T8
MODULATED OUTPUT
1 1 0 1 0 1 0 0
A
TIMING
T20 T19 T18 T17 T16 T15 T14 T13 T12 T11 T10 T9 T8 T7 T6 T5 T4 T3 T2 T1
DIGITAL MESSAGE
0 1 0 0 0 0 1 1 1 0 0 1 0 1 1 1 0 0 1 1
LOGIC "0"
LOGIC "1"
OUTPUT FREQUENCY
CRITICAL CROSSOVER ADJUSTMENT POINT.
B

Figure 12. FSK data.

then data must be transmitted at the slowest rate possible. On the other hand, a noise-free, interference-free line can handle data at a fast bit rate and is called a high-quality line.

1-31. *Decibel.* Now we need one final bit of information; then we can tie this discussion up. This information concerns the decibel (db) and dbm. The db is a unit of power ratio, and the dbm is a measure of absolute power as compared with a reference level of 1 milliwatt. One milliwatt of power is equal to 0 dbm. Look at figure 13. As you can see, the line loss from the transmitter (west line) is 10 db—transmitter output equals 0 dbm, repeater input equals - 10 dbm; This loss of 10 db represents a power loss of 90 percent, so if the signal injected into the line were 1000 Hz at 1 milliwatt of power, then the repeater would receive a .1-milliwatt signal at 1000 Hz. The repeater amplifiers are adjusted to provide a +30-db gain. This provides a power-ratio factor of 1000 and the output is 1000 × .1 = 100, or a +20-dbm signal since a power-ratio factor of 100 = 20 db. The east line loss is - 10 and the receiver input is +10 dbm.

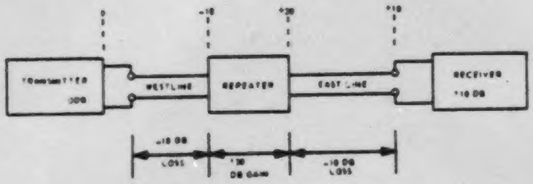

0
-10
+20
+10
TRANSMITTER
0DB
WEST LINE
REPEATER
EAST LINE
RECEIVER
+10 DB
-10 DB
LOSS
+30
DB GAIN
-10 DB
LOSS

Figure 13. Db loss and gain.

1-32. *Transmission path.* Refer again to figure 10 for this discussion. The transmitted signal enters the phone line from the modulator or transmitter at a fixed db level, usually between +6 to - 25 db. It may pass through one or more repeaters until it reaches the high-frequency terminal equipment. Here the data is modulated onto a high-frequency carrier and sped on its way to the receiver. Periodically along the line, repeater stations amplify the signal so that it has sufficient power to reach the next station. At the receiving end, the high-frequency carrier is removed and the audio-frequency data is fed to the receiver at the proper db level. The receiver demodulates the signal by a reversal of the process used to modulate it—dipole-to-digital, or FSK-to-digital as examples. Processing within the equipment then begins.

1-33. **Printers.** Operational checks on printers generally are performed by making the printer produce a printed copy. This makes for a reliable check since a good printout indicates that the printer is operationally satisfactory. Since the check is reliable for various types of printers, we shall discuss the identification of subelements within the printers which could cause an improperly printed

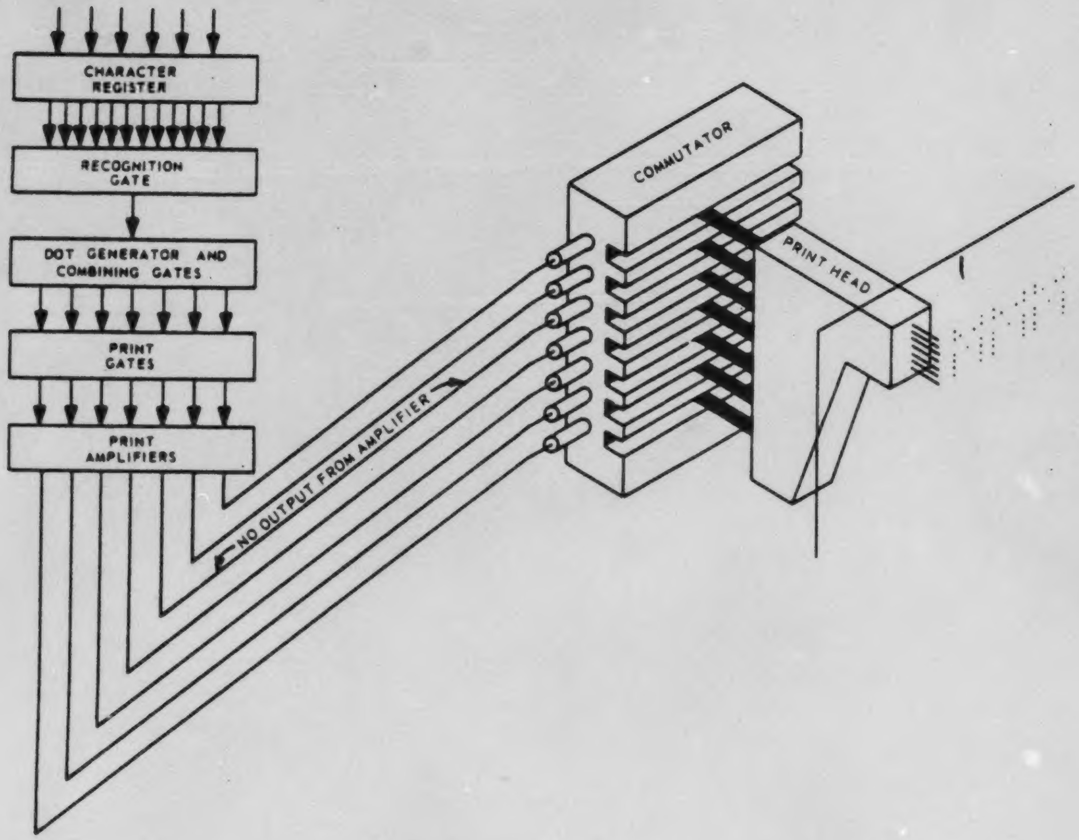


Figure 14. Printer character check.

message and visual tasks associated with them.

1-34. *Subelements.* Each of the elements listed and explained below can contribute to a defective printer output; therefore, each may be part of an operational check.

a. Switches. Various types of switches provide for control of the printer. These may be start, cycle, paper feed, advance, and electronic switches (solenoid) for selection of relays; during a print cycle any or all may be used. Failure of one often results in improper operation which can be visually determined.

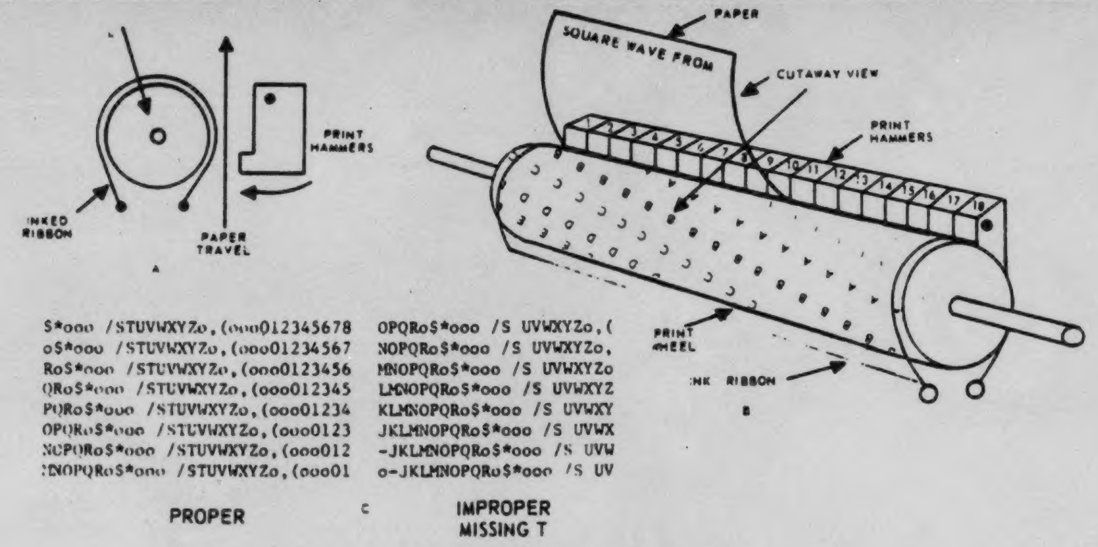
b. Power. Improper power supply voltage output affects operation. Indication of improper voltages may result in an insufficient number of printed lines per minute, improper spacing between lines, and missing or overlapped printed characters.

c. Character formation. Missing or incomplete character formation is generally the problem that is encountered. Understanding of the principles of printers aids in quick evaluation of malfunctions. For instance, if an amplifier fails (fig. 14) a row of dots will be missing on each letter of the printed message on the electrographic printer. Or if a character failed to print when using the impact printer, a hammer driver (refer to fig. 15) could be defective. Each of these examples shows the usefulness of the printout in locating the defect.

d. Mechanical. A defective printout could also be caused by a mechanical malfunction. Audio noises emitting from motors, drive units, etc., may be identified when a review of the printout shows defects in operation.

1-35. *Printout.* To summarize, printer operational checks can be performed reliably by using the maintenance diagnostic printout. Depending upon the type of printer, electrographic or impact, the test should include checks of as many subelements of the machine as possible. Characters, paper advance, switch operation (external and internal), mechanical units, and power supplies are some of the most important areas to be exercised during maintenance testing of operational reliability.

1-36. CRT Display. The method that is most adaptable to performance checks of the


PAPER
SQUARE WAVE FROM
CUTAWAY VIEW
PRINT HAMMERS
PRINT HAMMERS
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
INKED RIBBON
PAPER TRAVEL
A
PRINT WHEEL
INK RIBBON
B
C

```
$*ooo /STUVWXYZo,(ooo012345678   OPQRo$*ooo /S UVWXYZo,(
o$*ooo /STUVWXYZo,(ooo01234567   NOPQRo$*ooo /S UVWXYZo,
Ro$*ooo /STUVWXYZo,(ooo0123456   MNOPQRo$*ooo /S UVWXYZo
QRo$*ooo /STUVWXYZo,(ooo012345   LMNOPQRo$*ooo /S UVWXYZ
PQRo$*ooo /STUVWXYZo,(ooo01234   KLMNOPQRo$*ooo /S UVWXY
OPQRo$*ooo /STUVWXYZo,(ooo0123   JKLMNOPQRo$*ooo /S UVWX
NOPQRo$*ooo /STUVWXYZo,(ooo012   -JKLMNOPQRo$*ooo /S UVW
MNOPQRo$*ooo /STUVWXYZo,(ooo01   o-JKLMNOPQRo$*ooo /S UV
```

PROPER

IMPROPER
MISSING T

Figure 15. Impact printer defective print.

CRT display is the visual method using switches and controls. The visual display available most often can be selected by switch action from the console in which the CRT is located.

1-37. *Parts of a display unit.* Refer to figure 16. Almost all display systems require four basic units for operation. They are the vertical drive unit; the horizontal drive unit, which controls the sweep display; the intensity unblanking unit, sometimes called Z-axis, where intensification, blanking, video, or symbol analog data and high voltage are applied to the CRT; and a basic timing unit for controlled generation of all timing signals necessary for CRT display.

1-38. *Analysis.* By simple analysis of the video and control selection of data during callup, performance checks can pinpoint the defects in any one of these four areas. As an example, suppose that the focus is fuzzy. High voltage to the focus anode could be the problem if the variable control did not correct the focus. Linearity problems can be traced to horizontal or vertical sweep circuits. A blackened screen could lack timing or unblanking or even high voltage. Thus you can see that performance checks do check quality of the display and readily point to trouble spots.

1-39. Now let's see if you can associate performance checks with likely defects in circuits. Match the defects listed below with

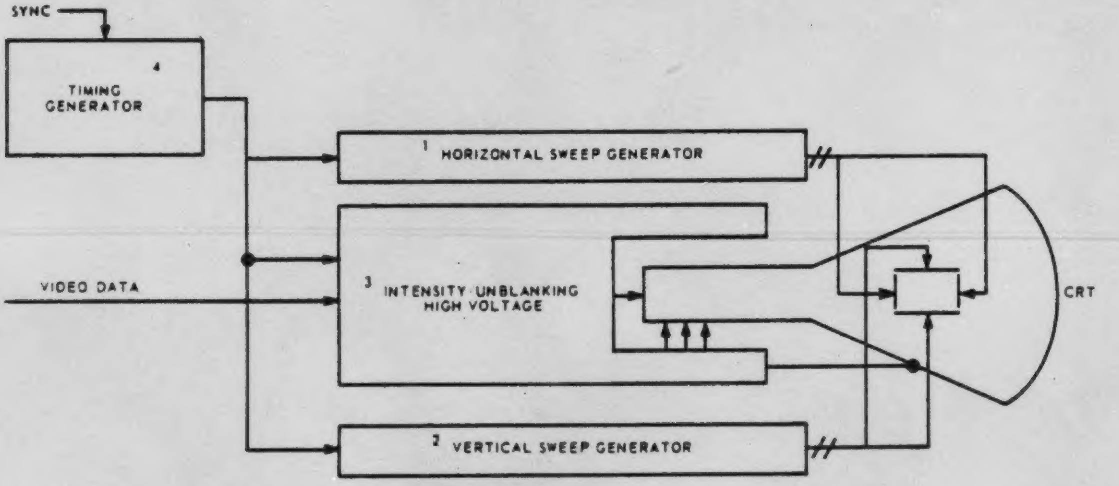

SYNC
TIMING GENERATOR
4
1 HORIZONTAL SWEEP GENERATOR
VIDEO DATA
3 INTENSITY UNBLANKING HIGH VOLTAGE
CRT
2 VERTICAL SWEEP GENERATOR

Figure 16. Display unit.

the units of the display unit that are listed:

Defects	*Display units*
____ *a.* A bright picture.	1. Intensity unit defect.
____ *b.* Out of focus.	2. Low high voltage.
____ *c.* Poor vertical linearity.	3. No high voltage.
____ *d.* No horizontal sweep.	4. Defective focus anode or low high voltage.
____ *e.* No data or video.	5. Intensity control advanced too far.
____ *f.* All black screen.	6. Sweep unit defective, vertical.
____ *g.* Sweeps do not reach outer limits of screen.	7. Timing control to horizontal unit missing.

Responses:

a. 5
b. 4
c. 6
d. 7
e. 1
f. 3
g. 2

1-40. **Central Processor.** A fault and facility panel, a confidence indicator, or error lights associated with on-line and off-line testing are the primary devices that are used to check performance in central processor units. The checks are primarily designed to validate the quality of data transfer, formation, storage, and erasure at specific times with specific known data inputs.

1-41. In every test, the successful end result validates the quality of the central processing (CP). These tests quite often must encompass I/O devices and peripheral equipment because the data needed comes from these units or must go to these units and return. To give you an example, consider the following sequence of events for processing data through an RCC (remote communication center):

a. Input fed from I/O keyboard through
b. concentrator (central processor) through
c. modems (modulator) and
d. back into the modem (demodulator) station-to-station operation, or
e. to a headquarters center, and
f. back into the modem (demodulator)
g. through the CP, and
h. to the printer (0) unit.

1-42. Another example might be checking the validity of data through the CP of the 412L AWCS system by using the central storage (tracker) unit by selecting a message for crosstell and having the message processor wired for back-to-back operation. The message would:

a. Process through the tracker storage unit to

b. the data link central when the data is formatted for transmission to

c. the message processor (MP). The message processor converts the data to FSK and transmits.

d. Back-to-back operation causes decoding of FSK data in the MP (demodulator) into digital data for

e. processing by the data link central for

f. storage in the tracker.

1-43. You can see by these simple examples that exercising the CP of equipment does provide reliable checks.

1-44. Interruption in data flow usually can be detected by observation of lamp indications on equipment and on confidence panels. If, you know and understand the full data content of a message and data flow within the CP, you will have very little difficulty interpreting data transmission and processing quality.

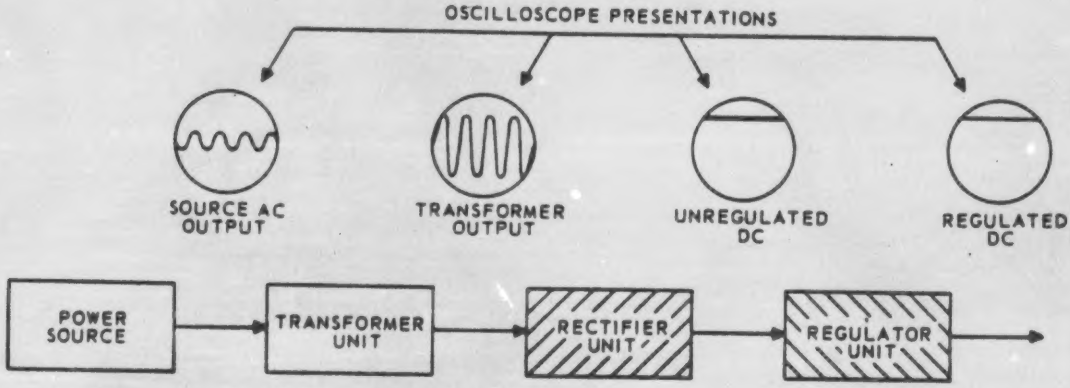


Figure 17. Power supply unit.

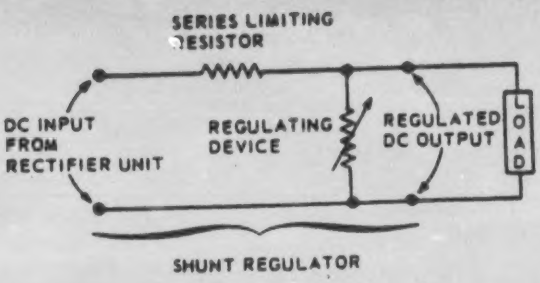


Figure 18. Shunt regulation circuit.

1-45. **Power Supplies.** Electronic power supplies are the units that supply the necessary voltage, power, and current for the operation of EDP equipment. Whether you are working on solid-state or electronic tube equipment, you will find that a well-regulated source of power is of primary importance. Performance checks are performed on these units to verify their proper operation. A review of general power supply construction identifies that most units have four elements. These are shown in figure 17 and are explained next:

a. AC source. Depending on the particular computer, the AC source may be the output of the motor-generator set or 60-hertz commercial power.

b. Transformer element. A DC power supply does not always have an input transformer; the input could be taken directly from the AC source. An obvious advantage of an input transformer is that the AC source can be isolated from the load and either stepped up or down within the transformer secondary.

c. Rectifier element. The rectifier unit converts AC to pulsating DC. Therefore, within the rectifier unit there must be some type of rectifying device such as half- or full-wave rectifiers or bridge rectifiers made from various electronic components such as diodes, saturable reactors, or transistors.

d. Regulator element. Although the unregulated output of a power supply may be satisfactory for some applications, a regulated output is necessary for most circuits. Regulating DC means keeping the output of the DC power supply constant. This is of critical importance for most circuit applications. Some regulator circuits may be quite simply designed, through the use of a single thermistor or zener diode. On the other hand, complicated units use an array of solid-state devices to attain proper regulation. Although solid-state regulators are functionally similar to electron-tube regulators, they can be used in more different ways. The fact that either NPN or PNP transistors can be used permits considerable diversity in design. Regulation of a power supply involves the control of either *voltage* or *current* or both. The types of regulation most commonly used are:

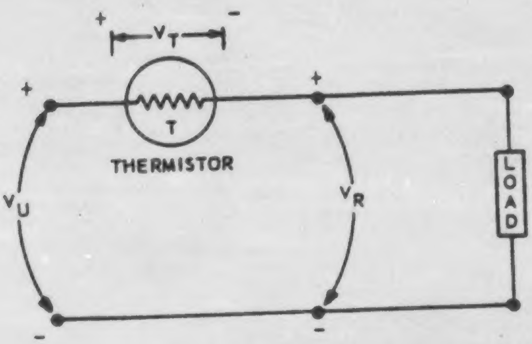


Figure 19. Series regulation circuit.

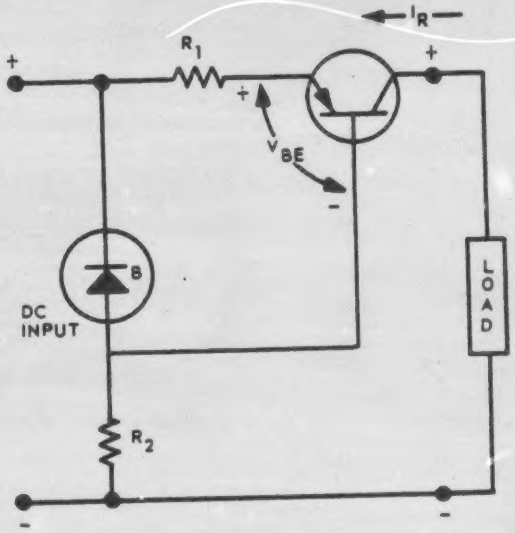


Figure 20. Current regulation circuit.

(1) Shunt voltage regulation has, as shown in figure 18, a limiting resistor in series with the load and a variable resistance in parallel (shunt) with the load.

(2) Series voltage regulation has, as shown in figure 19, a variable resistance in series with the load. The thermistor used as the variable component because of its negative temperature coefficient regulates the voltage at the load as the load changes, thereby regulating the output voltage.

(3) Constant current regulation has, as shown in figure 20, the capability to regulate the current rather than the voltage output. This is done by variation of the bias on the transistor. The transistor resists the current change.

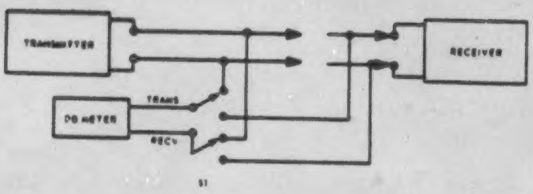

TRANSMITTER
RECEIVER
DB METER
TRANS
RECV
S1

Figure 21. Metering data lines.

1-46. Each power supply generally provides a visual display to identify its status. The display may be voltage or current meters, or indicator lamps in various colors. Some lamps represent proper operation (green), while others represent overload (amber or red) or failure (red) conditions.

2. Devices Used to Accomplish Performance Checks

2-1. In this section, we shall attempt to identify which methods and devices are used in performing operational checks in specific sections of computer and data processing units. After studying each discussion, you should complete parts of chart 1 (printed in the workbook), by placing an X under each part of the system which uses that method or device.

2-2. **Meters.** The performance checks accomplished in various areas using AC voltmeters (RMS), DC voltmeters, and differential voltmeters and VOMs are examined in the following paragraphs:

a. Line data (I/O). A method for determining line or data quality is by using an AC voltmeter (db meter). This unit is usually connected to the lines or at the common point in the modulators and demodulators. By reading the meter (dbm scale) and comparing the value to prescribed values for transmit and receive, it is easy to determine line quality. Refer to figure 21. You can see that it is relatively easy to connect the unit. One important factor to remember here is that the sensitivity of the meter must be very good or attenuation of the input and output signal will occur, and as much as 3-db loss can occur. A loss of 3 db results in 50-percent power loss and can easily interrupt data.

b. Power supplies (I/O/C). The performance checks used on power supplies require the use of DC meters for measurement of output amplitudes of DC power supplies and AC meters for AC power supply output measurements. The power supply may use a current (micro or ma) meter to measure current load output. The power supply may be equipped with a differential (null) DC meter where the output voltage is measured against an internal reference voltage. A deviation voltage reading from the null indicates improper output voltage.

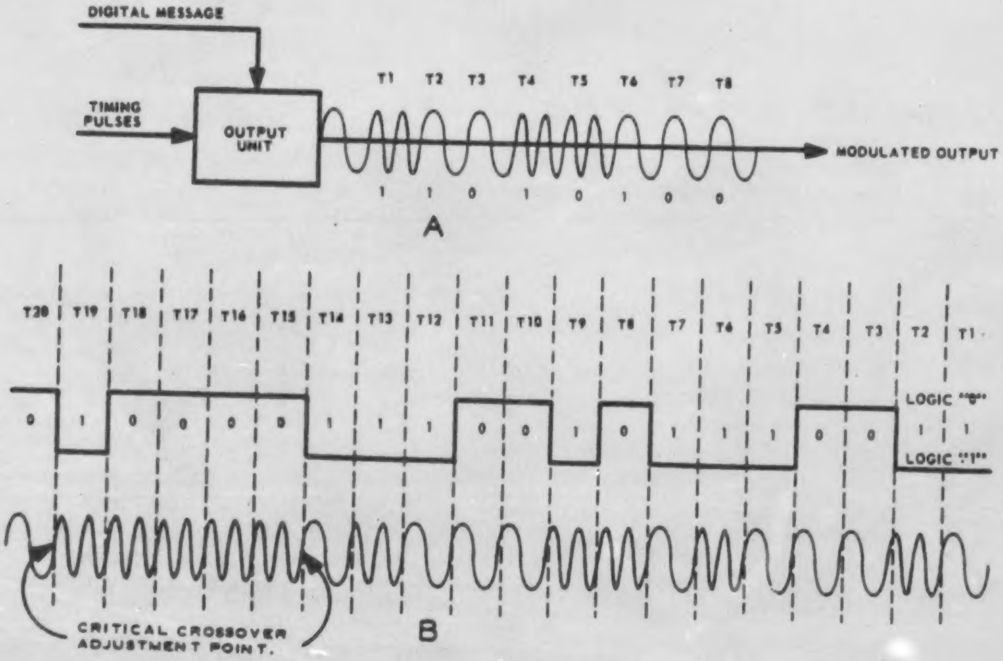

DIGITAL MESSAGE
TIMING PULSES
OUTPUT UNIT
T1 T2 T3 T4 T5 T6 T7 T8
MODULATED OUTPUT
1 1 0 1 0 1 0 0
A
TIMING
T20 T19 T18 T17 T16 T15 T14 T13 T12 T11 T10 T9 T8 T7 T6 T5 T4 T3 T2 T1
DIGITAL MESSAGE
0 1 0 0 0 0 1 1 1 0 0 1 0 1 1 1 0 0 1 1
LOGIC "0"
LOGIC "1"
OUTPUT FREQUENCY
CRITICAL CROSSOVER ADJUSTMENT POINT.
B

Figure 22. FSK crossover point.

c. Reference voltages (C). Within many data processors and computers, selected circuits generate DC reference voltages in order to insure proper linear circuit operation. These are generators other than power supplies. Performance checks on these voltage sources require the use of DC volt and differential meters.

2-3. Oscilloscope. We shall discuss next the performing of operational checks by use of the oscilloscope.

a. Line data (I/O). Oscilloscopes may be required to perform operational checks on modulators and demodulators, especially where a system is using an FSK system or frequency modulation system, or where data, sync, and timing pulses are transmitted separately. A critical point of inspection for FSK is at the coincident point (refer to fig. 22) where one frequency of FSK meets with the other frequency. The crossover point must be at the zero-volt level and the first frequency must be ending a cycle while the second frequency must be starting a cycle.

b. CRT displays (C). Oscilloscopes are frequently used on performance checks of CRT displays to measure waveforms such as ramps, generator outputs, timing circuits, deflection and intensity circuits, and input signal data to the CRT. Check to see that each signal measured contains all the elements of the waveform, and compare the waveform to a standard if possible. Some of the elements may be:

- Pulse width.
- Amplitude.
- Linearity of ramp signals, sine waves.
- Operating voltage levels.
- Pulse recurrence times (PRT).
- Proper waveform, i.e., no overshoot or undershoot of square wave.
- Ringing (noise).
- Data Content.

c. Servo units (I/O). The oscilloscope is used to validate waveform data from servos for nulling operations and reference voltage checks. Polarity, phase, and amplitude measurements must be determined and compared with standards. Amplifier chain waveforms may be compared to standards. Feedback loop signals may be measured for phase and amplitude.

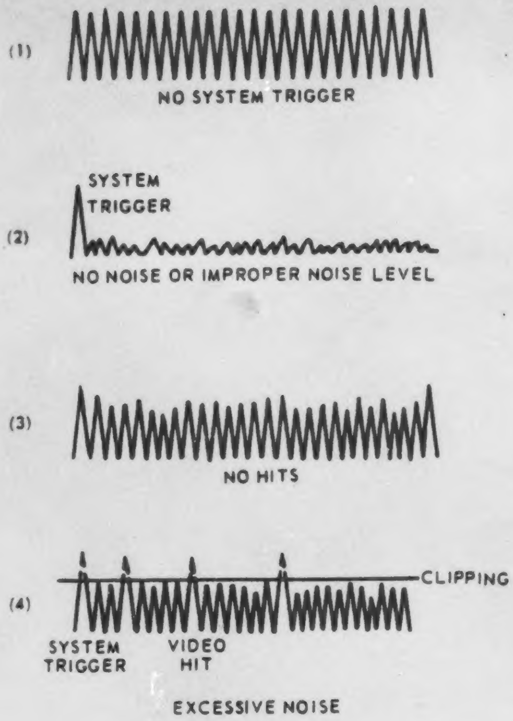


Figure 23. Defective radar returns.

d. Radar data (I). Oscilloscopes are the primary measurement tool for determination of the accuracy and content of radar data. Common defects or missing components of a waveform as shown in figure 23 can only be detected with a scope. These defects may be (1) no system trigger, (2) no noise or improper level of noise, (3) no video (hit) returns, and (4) excessive noise (clutter or jamming). The circuits which first receive radar inputs are usually the point of inspection. In these circuits, you must establish that video is present and that it is of the proper amplitude and polarity. Therefore, the operational check usually contains instructions to:

- Identify the points to measure and the controls to adjust.
- Measure the input level of the radar returns at various ranges.
- Measure and adjust the circuit output for a desired level and phase or polarity.

2-4. The instructions in the TO may also provide a video return drawing which resembles figure 2. If the regulating circuit is designed to adjust the amplitude of the video return by resistive means, weak signals and noise signals will be amplified or attenuated just as strong signals are. If the circuit is designed to adjust the amplitude of the video return by capacitive means, then amplification or attenuation of weak signals and noise can be controlled more than strong signals. This condition exists because a weak return may be only slightly stronger than the noise being received. Both of these components of

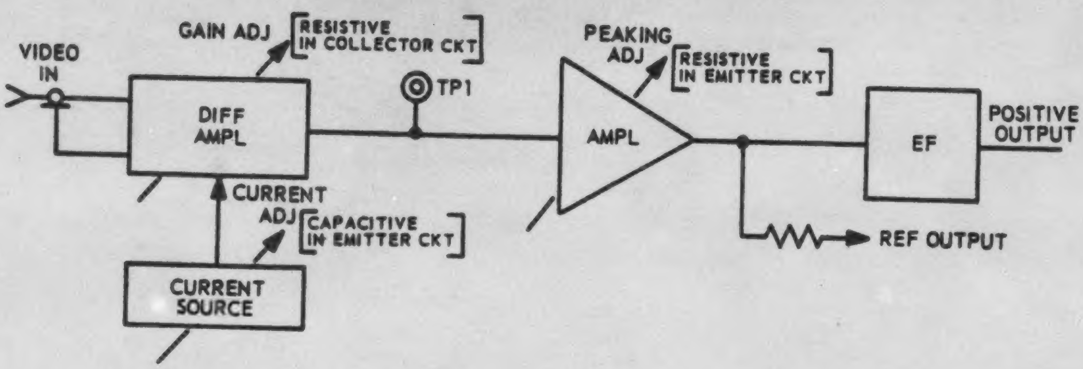

VIDEO IN
GAIN ADJ
RESISTIVE IN COLLECTOR CKT
DIFF AMPL
TP1
CURRENT ADJ
CAPACITIVE IN EMITTER CKT
CURRENT SOURCE
PEAKING ADJ
RESISTIVE IN EMITTER CKT
AMPL
EF
POSITIVE OUTPUT
REF OUTPUT

Figure 24. Video amplifier circuit.

the video return consist of sharp spikes of very narrow pulse width, and a pulse with a narrow pulse width may be expressed as a high-frequency pulse, especially when it is taken in relationship to the time for one radar trigger period. So, we must be conscious of which type of control we are using when examining and adjusting these inputs.

a. Video Amplifier Circuit. An oscilloscope is used to measure video amplification, and performance checks show where the likely measurable points are. Look at figure 24. You will see that video is fed to a differential amplifier through a coaxial cable. The shield of the cable is connected to the other input to the differential amplifier. These signals are forced by the amplifier to present the difference signal at the output. A variable current source is used to supply sufficient current for amplification and drive. This current source control is resistive. The video output is then fed to an amplifier circuit where a capacitive control is installed in the emitter portion of the circuit and is called a "peaking adj." Since capacitors control high-frequency pulses more than low-frequency pulses, as was previously stated, this control can, if misaligned, eliminate weak returns. The output of the amplifier is then fed to an emitter follower (EF) which supplies a current gain, no voltage gain, and no signal inversion. The EF output is routed to a gated amplifier which provides a control over the intensity of the video through a video intensity control. Therefore, a video return can be attenuated by three means—two are resistive and one is capacitive. The object, of course, is to establish a desired video output with sufficient amplitude and current to present a reasonably strong signal to a display CRT or to a detection circuit which is designed to store these pulses. Let us now consider another type of input unit which processes raw or normal radar video.

b. Quantizer Video Unit. A quantizer (refer to fig. 25) transforms video information from radar returns into distinguishable pulses for target determination. An oscilloscope is used to verify signal amplitudes. Performance checks require adjustment of various controls

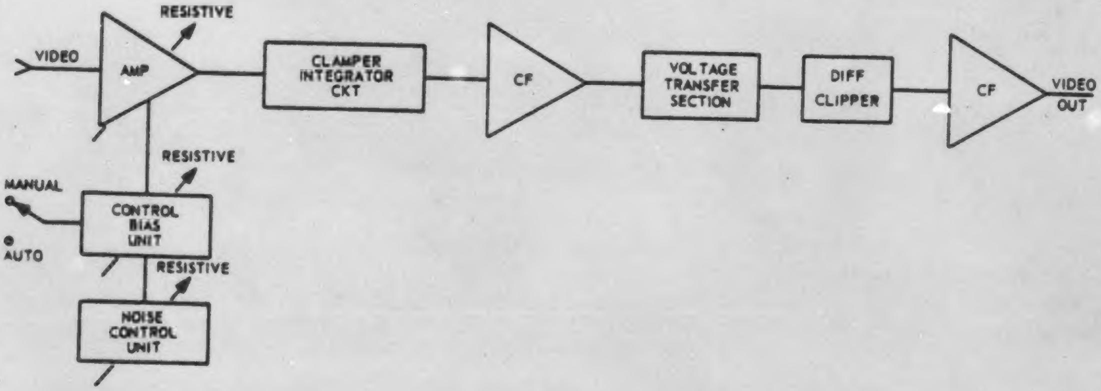

VIDEO
AMP
RESISTIVE
CLAMPER INTEGRATOR CKT
CF
VOLTAGE TRANSFER SECTION
DIFF CLIPPER
CF
VIDEO OUT
RESISTIVE
MANUAL
AUTO
CONTROL BIAS UNIT
RESISTIVE
NOISE CONTROL UNIT

Figure 25. Quantizer.

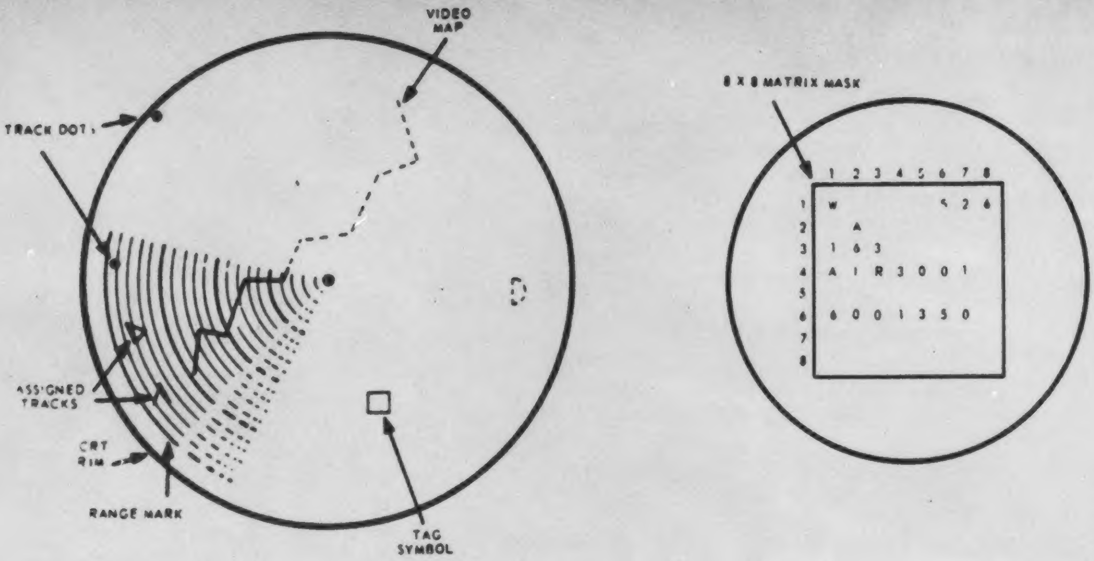

VIDEO MAP
TRACK DOTS
ASSIGNED TRACKS
CRT RIM
RANGE MARK
TAG SYMBOL
8 X 8 MATRIX MASK
1 2 3 4 5 6 7 8
1 W 5 2 6
2 A
3 1 6 3
4 A I R 3 0 0 1
5
6 6 0 0 1 3 5 0
7
8

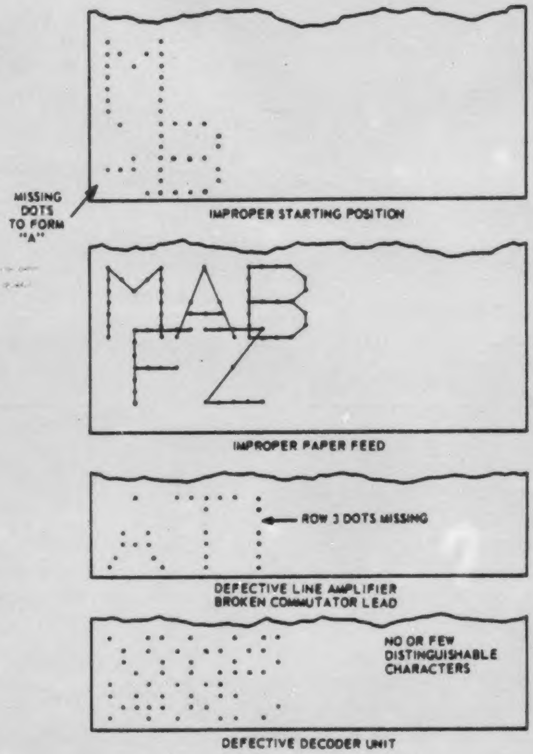
Figure 26. CRT displays.

in selected portions of the quantizer. The unit contains elements which aid in the detection of video and in the elimination of noise, clutter, and jamming. It provides a digitized video pulse output. There are various quantizers designed using vacuum tubes, solid-state devices, and integrated circuits; however, their functions are similar. Each uses a noise meter to establish an acceptable level of noise which must be present to insure that weak video returns are not eliminated from processing. The first control in the circuit is a video amplifier (resistive) control. Since the quantizers may be operated in a manual or automatic mode, bias level controls are included in these circuits and they are resistive. These bias adjustments cause amplifiers to pass only selected peak amplitudes of returns, but they must be adjusted to include a percentage of noise.

2-5. One final point about the use of a noise meter is that once its threshold has been exceeded, it blocks all video returns for the remainder of the radar period and part of the next radar period. The obvious conclusion is that the noise meter circuit can:

- Affect valid video returns by elimination.
- Be very effective during a jamming situation.
- Control the noise level of all video being processed.

2-6. Radar orientation validation (I). Oscilloscopes are used as coincidence detectors for insuring that the north mark and the prescribed number of ACPs occur. The scope is also used to check phase and amplitude signals from radar servos which are compared to a standard established for the system.


MISSING DOTS TO FORM "A"
MAB
FZ
ROW 3 DOTS MISSING
NO OR FEW DISTINGUISHABLE CHARACTERS

IMPROPER STARTING POSITION

IMPROPER PAPER FEED

DEFECTIVE LINE AMPLIFIER
BROKEN COMMUTATOR LEAD

DEFECTIVE DECODER UNIT

Figure 27. Defective printout.

420

2-7. CRT Displays (C). Video or symbol or digital displays have examinations performed during operation and the checks quickly pinpoint defects. Refer to figure 26 for some of the operations that must be included in the checks:

- Use of CRT voltage controls for intensity, focus, positioning, and astigmatism.
- Symmetry and linearity of range marks.
- Callup operations of console.
- Printing capability of the digital display by use of test pattern. If complete, this test also exercises all character generators.

2-8. Printouts (O). The following discussion covers the use of printouts as a check for operational quality:

a. Electrographic printers (O). The printout determines the operational capability of this printer. An accurate printout satisfies performance requirements for quality and accuracy. A defective printout such as that shown in figure 27 indicates (1) improper starting position of commutator brushes, (2) defective paper feed, (3) defective line amplifier or a broken commutator lead, or (4) defective decoder unit.

b. Impact printer (O). Printouts which display all characters and numbers validate operational quality. Print selection circuits, mechanical assemblies, and character decoding circuits are the most frequent sources of trouble.

c. Central processor data (C). Printouts which are generated as a result of data taken from peripheral equipment or I/O equipment and which process through the DPC may be used to validate DPC operational quality.

2-9. Lamps and Audio Alarms (I/O/C). The use of lamps and audio alarms is discussed next:

a. Line data lights (I/O). Interpretation of lamps or alarms usually verifies that sync group (audio signal data preceding the data message) signals are present or absent. They may be called busy bit, sync group, or no message characters. A synchronization circuit samples sync bits and provides visual lamp failure indications and audio tone failure indications.

b. Parity lights (I/O/C). Lamps provided for these circuits show that a circuit designed to count each bit of an incoming or outgoing message detects overall correct parity. Failure may be indicated on fault facility panels or confidence indicator units or other convenient panels where lamp and audio indicators alert failure.

c. Power supplies (I/C). Lamps indicate operational quality; green or white for power on, amber for overload, and red for voltage failure.

d. CP units (C). Lamps indicate counter operations, sequences, data flow (yellow or white), and failure (red). Sampling circuits may use live data or test data, depending upon design.

e. Tape transport units (I/O). Sequence lamps, failure lamps, and command and control lamps indicate the status of the unit. Interpretation of lamps may relate to specific areas where operation ceases.

2-10. Visual Examination of Mechanical Assemblies (I/O/C). Some examples of visual examination to find defects are given below:

a. Servo units (I/O). Noisy or binding gear trains are the only visual examinations possible on these units.

b. Electrographic printer (O). Noisy drive unit or clutch assemblies and improper paper feed are all signs of visual defects.

c. Impact printer (O). Visual indications of improper or proper operations of cams, motors, paper feed, impact hammers, and other related units provide reliable visual examination of this printer. Interpretation of the printout also provides reliable performance data.

d. Tape units (I/O). Proper orientation of tapes, operation of servos, takeup reel tension, and photolamp illumination or vacuum pump operation are all visual indications of proper or improper operational performance.

2-11. Conclusions. The examinations of operational checks performed on some of the various input/output and DPC units bring certain factors into focus. These are:

a. The checks require the use of visual indicators such as:

- Lamps.
- Readout prints.
- Meter readouts.
- Mechanical movements.
- Meters and test equipment.

b. The checks can often be made by exercising the machine operationally and analyzing the output product. The input, output, and DPC units require that specific tasks and specific equipments be used to perform the operational performance check. When you completed chart 1 (printed in the workbook), you identified which part of the data processing system used specific pieces of test equipment and indicators. Listed below in column 1 are the units. In column 2 we list the most appropriate methods used to perform operational checks. A comparison of this listing with the chart you completed should reinforce the concepts you learned while studying

430

this chapter. Figure 28 (printed in the workbook) shows how chart 1 (in the workbook) should be completed. Should you find significantly different indications in your chart, restudy the text.

Unit Data	*Subtask Check*
(1) Radar, Beacon	*a.* Hands-on method. *b.* Use oscilloscope. *c.* Measure input amplitude, phase, and polarity.
(2) Radar Antenna Orientation	*a.* Hands-on method. *b.* Use display equipment. *c.* Use oscilloscope. *d.* Measure and adjust ACP counter output, north pulse. *e.* Correct for error of ECC.
(3) Keyboard	*a.* Operational check. *b.* Check for proper orientation of key board characters, Fieldata codes. *c.* Use with tape unit. *d.* Perform electrical check. *e.* Interpret error indication.
(4) Tape and Tape Drive	*a.* Operational check. *b.* Mechanical check. *c.* Cause advance, reverse, read, and write. *d.* Evaluate printout of tape. *e.* Check all ones, all zeros, crosstalk.
(5) Line Data	*a.* Use meter readings for line quality. *b.* Transmit and receive. *c.* Interpret visual indication. *d.* Examine data for quality on a bit-rate ratio basis.
(6) Printers	*a.* Operational check with printout. *b.* Visual check of mechanical movement. *c.* Interpret noise, impedance, poor quality printout. *d.* Interpret lamp indicator.
(7) CRT Display	*a.* Visual inspection, using video, symbol modes. *b.* Examine for definition of details. *c.* Operate display with controls and switches. *d.* Interpret indications. *e.* Locate defects in digital information displays.
(8) Servos	*a.* Use oscilloscope, display consoles, RMS and DC meters. *b.* Check null. *c.* Check servo vs. antenna rotation. *d.* Check servo position.
(9) Power Supplies	*a.* Use meters—current and voltage. *b.* Use differential meter. *c.* Interpret lamps.
(10) Central Processor	*a.* Use fault indicator panel. *b.* Use confidence indicators. *c.* Interpret reference indicator lamps (counters, data transfer).
(11) Reference Voltage	*a.* Use same procedures as for power supplies. *b.* Use meters. *c.* Interpret lamp indicators.

CHAPTER 2

Adjustments

EACH OF YOU HAS, during your training at the resident center, performed a task called "adjustments." In all probability, you were shown the control to adjust and given a standard to meet. You turned the control in one direction or the other until a specified standard was indicated on a measuring device. Some of you were very cautious in turning the controls and others were not. Since you arrived at your work center and started upgrade training, you should realize that indiscriminate control manipulation often produces disastrous results. Circuit misalignment can result in loss of equipment operation, cause unnecessary work problems, and upset supervisors.

2. Each adjustment must be made with care for the circuit operation. Often, these adjustable components are set very near the proper point. It helps if you know the proper direction in which to turn a control. However, if you must guess the direction, you have a 50-50 chance of disturbing the circuit operation and causing it to operate worse than it did before. Then you will have an extreme adjustment to make. In many circuits, reactive components are the adjustable units and, when these are arbitrarily turned, extreme results are produced. Selected frequencies may be attenuated or lost, waveforms may be distorted causing improper data flow and loss of digital data quality, and operating levels may be affected causing a shift in amplifier operation.

3. This chapter identifies reactive controls, gives their characteristics, and shows how they are used in various circuits. The definitions below should help you to distinguish the difference between adjustments and alignments.

4. *Adjustment* is the act whereby a device is used to alter a condition to make it fit or correspond. This means, for purposes of this discussion, the physical change of a variable component to make the circuit provide a discrete output. The word *alignment* means to bring into line or straight line. For the following chapter on alignments, this means that the adjustments are combined within a functional unit to provide a discrete output.

3. Characteristics of Variable Controls

3-1. Characteristics are explained by purpose, type, and principle of operation.

3-2. **Purpose.** Each time that a variable control is included in a circuit, it serves a distinct function in the operation of that circuit. It is a compensation device used because the inputs to the circuit are variable signals which must be regulated to provide a specific output. Within the circuit, this may cause increase or decrease in bias voltage or current, a change in frequency, or a shift in frequency. Any one of these changes causes the circuit to operate outside its designed operating level. The signal may be affected by distortion, limiting, attenuation, or amplification. Variable controls are used to alter the output waveform to meet specifications. However, if the input signal strength causes the circuit to operate beyond the control of the variable device, no amount of adjustment can correct the output waveform. This is a significant factor to consider when studying the purpose of a variable control.

3-3. **Types.** Study the illustrations in figure 29 (printed in the workbook). Each of these components is a variable control, even though physical appearances vary. Two common types of *variable capacitors* are the tubular type (A) with an adjustable core, and the button type (B) with a variable rotor. In either case, different values of capacitance are obtained by varying overcoupling of the plates. For most frequencies up to 30 MHz, these are adequate. For frequencies above 30 MHz, the variable capacitor must be constructed so that no RF voltage is developed. This is often done by having the external circuit connected to two sets of stator plates and using the rotor to increase or decrease the

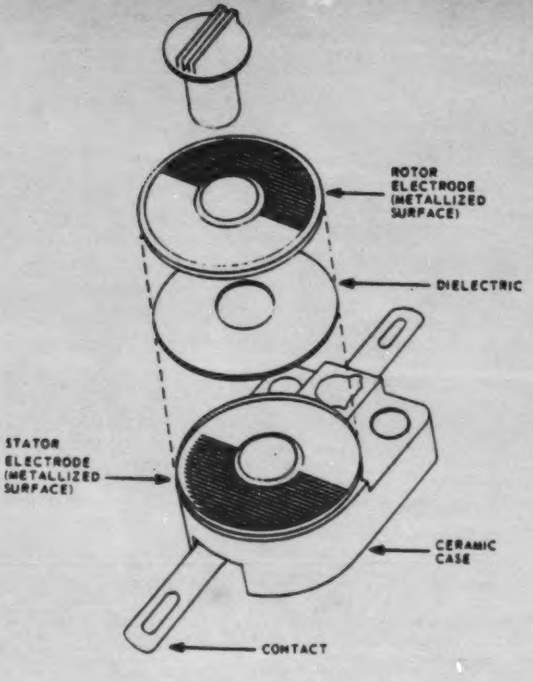

ROTOR ELECTRODE (METALLIZED SURFACE)
DIELECTRIC
STATOR ELECTRODE (METALLIZED SURFACE)
CERAMIC CASE
CONTACT

Figure 30. Variable capacitor.

total capacitance between the plates. In this arrangement, no RF current flows since the rotor is not a link between the stator plates. Figure 29, C (printed in the workbook), shows a typical *potentiometer*. This control uses a rotor; however, the rotor is in contact with the resistive element. The output voltage or current is tapped off at the point of contact. Figure 29,D, is an example of a potentiometer commonly found on printed circuit cards. Its control is a screw-type shaft which, when turned, causes a contact point on the screw to mate with the resistive element. This provides an output voltage or current proportional to its wiper arm position. The control shown usually has from 8 to 26 full turns.

3-4. Inductors and coils may also be variable and are used extensively in electronic equipment. However, variable coils are seldom used in data processing and computer circuitry so no further coverage is included.

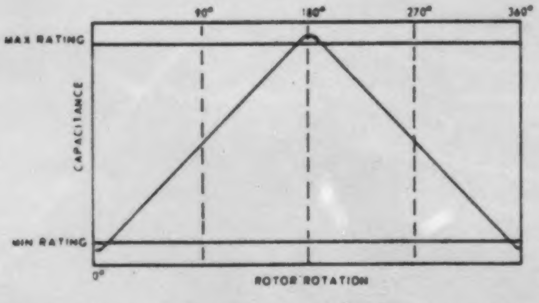


Figure 31. Linearity through 360° of rotor rotation.

3-5. **Principles of Operation.** *Variable capacitors* are manufactured, using different material as dielectrics. Some are ceramic, mica, glass (piston), polystyrene, teflon, and air. Each of these materials has a different dielectric constant. The basic principle of a variable capacitor involves positioning the rotor with respect to the stator. The area of electrode (plate) is fixed. Turning the rotor from 0° to 180° varies the amount of plate surface exposed, thereby varying the amount of capacitance. Refer to figure 30 and note that the metallized rotor surface may overlap any part of the metallized stator surface. With this arrangement, the capacitance varies, depending upon the amount of metallized plate overlapping and the dielectric constant. To vary capacitance requires either varying the dielectric of varying the overcoupling of the electrode plates.

3-6. In most trimmer capacitors used in computer and data processing circuits, the variable change in capacitance is linear throughout its rotation (see fig. 31). The figure shows linear increase and decrease in capacitance through 360° of rotor rotation. Variable capacitors or trimmers are frequently used as filters in oscillators, and as attenuators in displays and counters.

3-7. Let's review some characteristics of the newer types of capacitors which can create problems for us:

a. Most ceramic capacitors have a maximum life of 250 turns. Some tubular types have 1000 or more turns of life expectancy.

b. Adjustments must be made with tuning wands since most trimmers connect the stator or rotor to the end frame or turning screw. Placing a metal screwdriver on the turning screw changes the effective area of the metallized plated surface of either the rotor (usually) or the stator, thereby altering the characteristics of the capacitor.

c. The size of these units is being reduced to meet demands of industry for microelectronics. As a result, the voltage breakdown values have been drastically reduced.

d. Tubular type variable capacitors (fig. 32) are now satisfying industry's requirements for microelectronics. These capacitors possess a characteristic not unlike potentiometers in that small, critical adjustments can be made on them. The sliding action of the rotor, controlled by the screw, changes the plate area opposite the stator, thereby varying the capacitance.

3-8. Later in this chapter, applications of these capacitors will be explained. Let us now review the principles of potentiometer operation.

3-9. Potentiometers are variable resistance components. They may be either carbon pile or wire wound. The wire-wound potentiometers are usually used as rheostats rather than as potentiometers. To see the difference between the two, look at figure 33. Figure 33,A, is a schematic symbol for a rheostat. Notice that the resistor element is connected to the circuit at each end, and the slider arm, which is used as the pickoff point, is connected to one of the ends. However, in figure 33,B, the potentiometer is connected with the entire resistance in a series configuration and one end of the slider performs the pickoff function while the other end is connected to an external circuit. It may be used like a rheostat and still be called a potentiometer.

3-10. Potentiometers, or "pots," are used extensively in computer and data processing equipment. Usually, they are carbon and resemble those shown in figure 34,A and B (printed in the workbook). Notice that figure 34,C indicates that a brass slider is positioned by the turning screw to some point along its path of travel. Its position is manually selected and the resultant output voltage is fed to the using circuit. In the manufacture of these units, the adjusting screw is isolated from the carbon resistor and the metal turning shaft by a nonconductive substance, such as epoxy. Figure 34,D shows the internal structure of the pot shown in figure 34,B. Notice that the resistive element is circular in shape and that each end is connected to an external terminal. The variable slider or wiper is pressed against the resistor by spring action and is isolated from the turning screw. The slider has continuity to the third terminal through the circular ring. Two factors must be identified and explained here. First, when the turning device of the rectangular pot is turned to its end, it may make an audible clicking sound signifying that no further turning in that direction is possible. Second, the pot shown in figure 34,D, usually has a mechanical stop at each end of the resistor and further turning of the screw results in shearing the stop pin or destroying the pot screw or both.

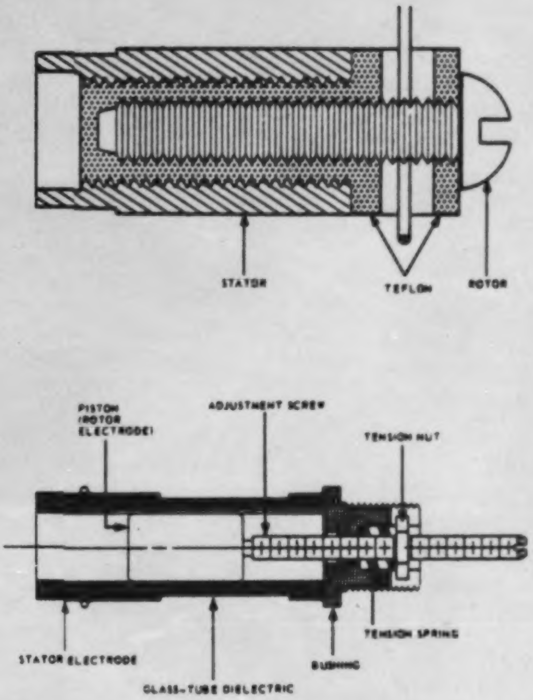


Figure 32. Tubular capacitor.

3-11. Since we are discussing the adjustment of circuit components and the variable resistor, we must recognize another manufacturing characteristic of these components. Variable resistors and pots are made linear and tapered. The linear pot is made so that its resistance is distributed evenly over its entire length. When an ohmmeter is used to measure its resistance, the wiper arm output resistance causes an even deflection of the meter needle for the entire length of the resistor. The tapered pot is made so that one-tenth of the total resistance is available between one extreme and the midpoint of the adjustment cycle, and the other 90 percent of resistance is available between the midpoint and the

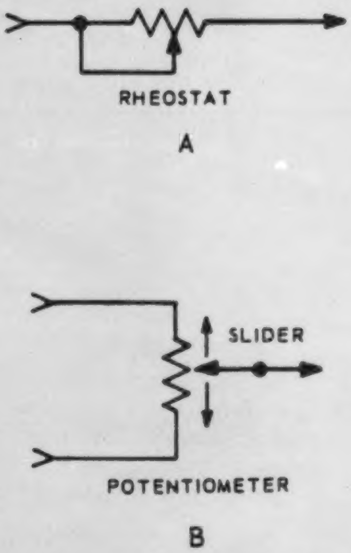


Figure 33. Potentiometer and rheostat.

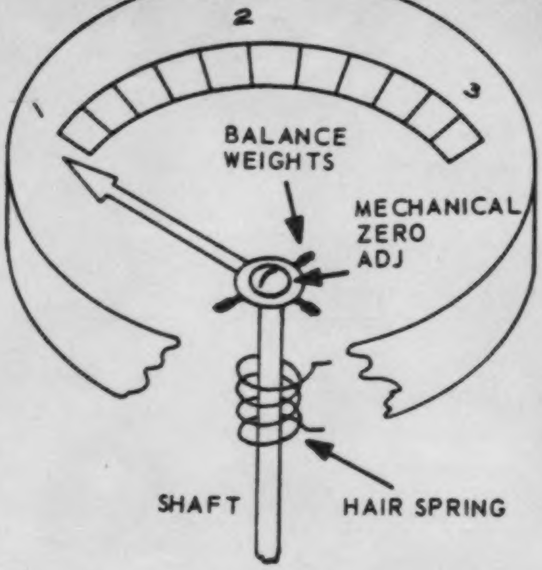


Figure 35. Mechanical needle adjustments.

other extreme of the adjustment cycle. If you use an ohmmeter to measure the resistance of a tapered pot, placing one lead on the input terminal and the other lead on the wiper (rotor) terminal, you can see that, as you turn the wiper, the resistance increases (from zero) very slowly and gradually until you reach a point midway on the pot. From the midpoint on, as you continue to turn the wiper shaft, the resistance increases much more rapidly in comparison with the first half pot rotor rotation.

3-12. Technical Orders. Typically, adjustment instructions are found in preventive maintenance routines and in the chapter of the service manual titled "Maintenance." These instructions seldom provide any explanation of why an adjustment is performed. Compliance with the instruction is not very difficult when you can accomplish it; however, when you cannot comply, where do you go? The answer, of course, is that you must study the theory of operation of the circuit or function so you can apply a logical and accurate solution in minimum time and, by having a thorough understanding of variable components, their design and application, insure greater success. Speaking of applications, let's explore some of the most typical areas of equipment where we might use adjustments.

4. Adjust Meters and Dials

4-1. Adjustments that you can make on meters and dials are usually restricted to centering the needle and calibrating it with the calibrating voltage and adjustment control. The only exceptions to these adjustments are those where you are required to perform category 1 or 2 test procedures for test equipment (Chapter 4, Volume 1).

4-2. **Balancing.** Positioning the needle on a meter or dial requires you to use a small screwdriver and to carefully adjust the screw until the pointer aligns with the proper mark on the meter face. Refer to figure 35 and you will see that this adjustment is mechanical and that no voltage or current is involved. You merely twist the control and position the pointer, which is pressed onto the shaft, to the correct position. Balancing the meter needle requires disassembling the meter and

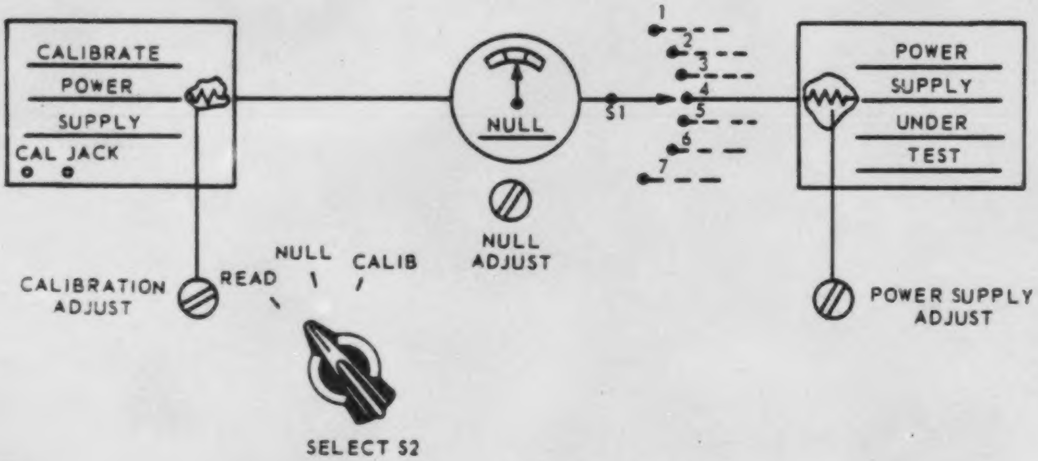


Figure 36. Simplified differential meter circuit.

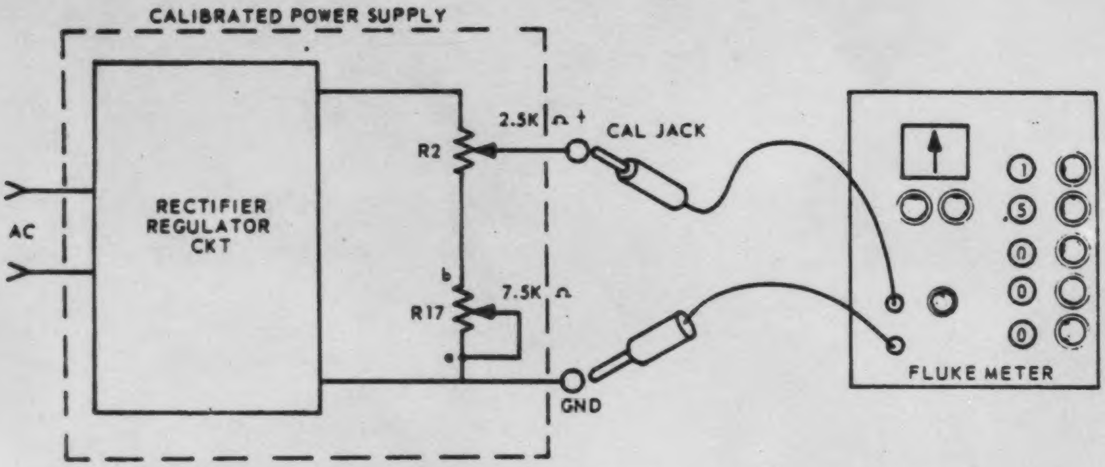

CALIBRATED POWER SUPPLY
AC
RECTIFIER REGULATOR CKT
R2
2.5K Ω +
CAL JACK
b
R17
7.5K Ω
a
GND
1
.5
0
0
0
FLUKE METER

Figure 37. Calibrate adjust.

repositioning the weights on the needle shaft; these adjustments are performed by PME Laboratory personnel.

4-3. Centering. Adjusting a meter before it is used requires a check of internal electrical components. This is called *zeroing in the meter.* For ohm-adjusting, short the two probes together. This should cause 100-percent deflection of the needle. A potentiometer in the meter circuit will adjust current from the battery to cause 100-percent needle deflection. When you change ohm scales on your meter, you change the sensitivity of the meter. Therefore, you must adjust the needle deflection again by use of the adjustment of zero pot. To adjust a meter such as a differential voltmeter, apply a source voltage to the balancing circuit. Most differential voltmeters work on the same principle. Refer to figure 36 for a simplified circuit of a differential voltmeter application. Notice how simple the unit is. As you can see, the calibrated power supply is very similar to an 801B differential voltmeter except that this power supply is permanently installed as part of the equipment. It feeds its output to one side of the meter. The power supply under test has its output sampled under load condi-

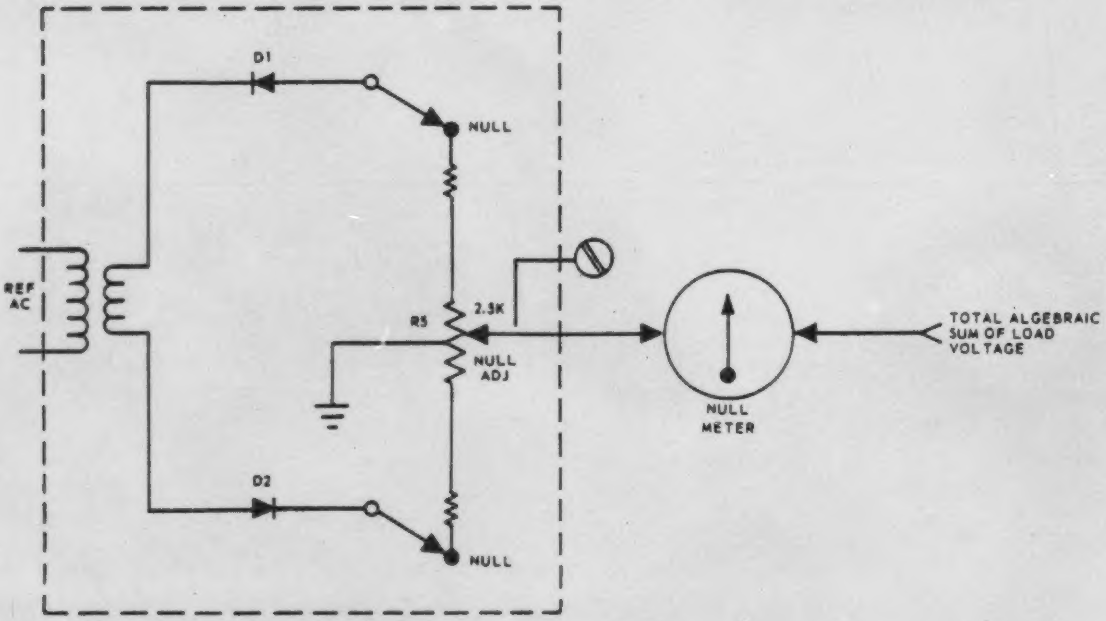

D1
NULL
REF AC
R5
2.5K
NULL ADJ
NULL METER
TOTAL ALGEBRAIC SUM OF LOAD VOLTAGE
D2
NULL

Figure 38. Null adjust.

tions, and if both voltages are exactly the same, there is no deflection of the null meter needle.

4-4. Two factors become important to the analysis. First, before the power supply can be used as a standard, it must be calibrated. Remember, from your study of test equipment calibration in Chapter 4 of Volume 1, that some equipment is calibrated by PME for use as a shop standard. An 801B, for instance, can be used to calibrate the power supply. Then you can use the power supply as an equipment standard. Second, having a calibrated source voltage available in the equipment allows an accurate check of all power supplies that use that same voltage. By use of a selection switch (S1 in fig. 36), any or all units can be tested rapidly.

4-5. Applying. Figure 37 shows an application of potentiometers. R17 is a 7.5K potentiometer connected as a rheostat. It can, by variation, change the output voltage for the full range of the 7.5K potentiometer because when the wiper arm is at point *a*, the full resistance is in the circuit. If the wiper is moved to point *b*, then all of the reisstance is removed from the circuit. R2 in figure 37 is a 2.5K potentiometer used to pick off a portion of the voltage, depending upon its position. R2 and R17 combine to make a voltage divider.

4-6. By plugging in a differential voltmeter and setting it for the exact output voltage, adjustment of R2 and R17 can provide an output which can act as the standard.

4-7. *Null adjust pot.* In figure 38, the null adjustment pot incorporates a centertap pot and, in this application, the centertap is grounded. The variable control then has the ability because of the conduction of diodes D1 and D2. The *pickoff* voltage is matched against the algebraic sum of the load voltages of the power supply under test.

4-8. Finally, the power supply under test is adjusted to the calibrated voltage power supply. This is done by switching to the read position as shown in figure 36, and the power supply voltage under test is fed to the meter. If deflection occurs out of the limits prescribed in the TO, adjustment of the pot for that supply increases or decreases the voltage to the null meter and effectively calibrates the power supply to the preset calibrated value.

4-9. *Ohmmeter adjust pot.* Refer to figure 39 (printed in the workbook), the meter zero circuit of a typical VOM. This meter incorporates two voltage sources for measuring resistance: the 1.5V battery for the RX1 and RX100 scales, and the 6V + 1.5V batteries for a total of 7.5V for the RX10K scale. In each case the meter, which has an internal resistance of 1.8K and requires a current of 50 μa for full-scale deflection, uses only .09V of the battery source. The remaining voltage and current are dropped within the circuits when zeroing the meter.

4-10. By examining the three modes of operation, RX1, RX100, and RX10K, you can see that Rt for each mode is different. RX1 has an Rt of 29,788 ± 5K. RX100 has an Rt of 28,760 ± 5K. They are almost alike, except that in RX100, R2 is substituted for R1. Finally, Rt for RX10K mode has a total resistance of 124.5K ± 5K. This mode has an additional voltage source of 6V, making a total of 7.5V. The three modes are calculated below to show Rt and Et:

RX1 Path = M + R25 + R3 and R1
= 1800 + 10K + 21,850 + 1,138
Rt = 29,788 ± 5K
Et = 1.5V

RX100 Path = M + R25 + R3 and R2
= 1800 + 10K + 21,850 + 110
Rt = 28,760 ± 5K
Et = 1.5V

RX10K = M + R25 + R4
= 1.8K + 10K + 117,700
Rt = 124.5K ± 5K
Et = 7.5V

4-11. In addition to these factors, consider R25, the 10K pot. Its quality is established at an accuracy of only ±30 percent. Finally, the voltage source must be taken into account. If it is weak, it will not provide the current required for proper circuit operation. With all these conditions, you can see the importance of the role the pot plays in providing a control in the variables for accurate use of the meter.

4-12. The examples of centering and null adjusting begin to identify the versatility of the potentiometer. Each example shows how the pot acts as a resistance factor and that the wiper arm selects a voltage proportional to its position. You can see that meters and dials require the use of potentiometer adjustments and screws to prepare them for use as measuring devices, just as amplifiers and pulse generators need them for amplification and bias control.

5. Amplifiers and Pulse Generators

5-1. In many cases, amplifiers and pulse generators incorporate variable components. The primary objectives of variable components in these circuits are to (1) alter the gain ratio of the circuit, (2) control the pulse

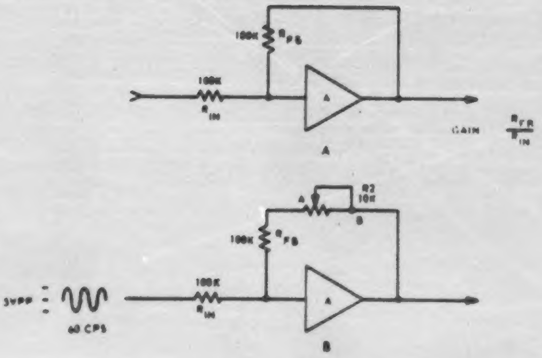


Figure 40. Operational amplifier.

duration, or (3) act as phase-shifting device. To understand these uses of the pot or variable capacitor, examine the basic amplifier and relate its principles to some of the more complex circuits.

5-2. Adjust an Operational Amplifier. An operational amplifier is a circuit consisting of three basic parts: (1) an input resistance, (2) a high-gain amplifier, and (3) a feedback resistance. Refer to figure 40,A, and note that R_{in} is the input resistance and has an assigned value of 100K; therefore, the circuit has a gain of unity $\left(\frac{R_{fb}}{R_{in}} = \text{gain}\right)$. For example, a 5-volt signal into R_{in} results in a 5-volt signal output from the amplifier. Now look at figure 40,B. By the insertion of 10K pot, the circuit is made to provide a variable amplitude output. Apply a 5-volt 60-Hz signal into the amplifier and see what effect the pot will have.

5-3. First, establish the parameters of the circuit. R_{in} = 100K; R_{fb} = 100K ± R2, 10K. Therefore, the gain of the circuit is from unity in the case where the wiper of R2 is at point A, or 10 percent where the full pot is in series with R_{fb}. With 5V PP input and the pot at minimum, or point A, the output equals 5V PP—unity. Consider the full pot in the circuit. The feedback loop equals 110K; R_{in} = 100K. Therefore:

$$\frac{R_{fb}}{R_{in}} = \frac{110}{100} = 1.1 \text{ gain}$$

Therefore, 5V PP × gain of 1.1 = output of 5.5V PP, or a gain of 0.5V PP.

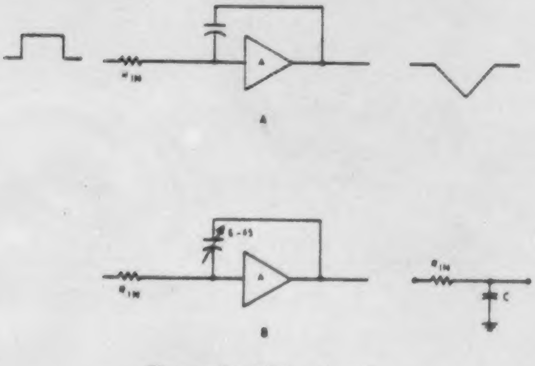


Figure 41. Miller circuit.

5-4. Based on these conditions, the maximum variation that the circuit can have is .5V PP. Change the size of any component and apply the formula and you can obtain the maximum and minimum gain.

5-5. Adjust a Miller Circuit. Now, alter the basic circuit again and this time replace R_{fb} with a fixed capacitor. This simple change results in development of a Miller integrator circuit. Refer to figure 41,A, and see that a rectangular wave input produces a sawtooth output. The Miller integrator is a special amplifier, using a feedback capacitor instead of a resistor. It provides a linear rising (or falling) output voltage when the input level is suddenly decreased or increased. This circuit is basically an RC circuit with the time constant increased by the amplifier gain. Since long time constants can be obtained by using high gain, the output is very linear.

5-6. Now refer to figure 41,B, and see that by replacing the fixed capacitor with a variable capacitor, the capacitor provides a capability for altering the overall time constants of the circuit. Selecting any position of the variable capacitor affects the amplitude of the output waveform since the input pulse is constant. All RC networks contain specific time constant values to charge to full potential. Therefore, if the time is restricted as in our example, any change in capacitance results in a charge being accumulated on the capacitor for the same time duration each cycle. Study the following example:

$$T = RC$$

Where:

$R = 1000$
$C = 6 - 45\ \mu\text{fd}$

Therefore:

$$(1)\quad T = 1 \times 10^{3} \times 6 \times 10^{-6}$$
$$= 6 \times 10^{-3}$$
$$= .006 \text{ seconds or 6 milliseconds}$$

or:

$$(2)\quad T = 1 \times 10^{3} \times 45 \times 10^{-6}$$
$$= 45 \times 10^{-3}$$
$$= .045 \text{ seconds or 45 milliseconds}$$

The output waveform can be altered to have one time period for charge from 6 milliseconds to a maximum of 45 milliseconds. Now, by applying a fixed input waveform to control the output as is shown in figure 42 (printed in the workbook), you can see that the output waveform becomes a sawtooth. Also, by studying the graph you can see that for a pulse duration of 1 millisecond:

a. The circuit with a capacitance of 6 μfd allows a charge of 20 percent before discharge begins.

b. The circuit with a capacitance of 45 μfd allows a charge of 2.5 percent before discharge begins. From these conclusions, then, the output waveform varies in amplitude depending upon the position of the variable capacitor.

5-7. To go one step further, you can calculate the maximum and minimum points or the maximum variable gain. Assume that the output can have a maximum voltage of 35 volts with a control input gate of 1 millisecond. This would mean that the variable capacitor would have a capacitance of 6 μfd. Turning the control to the other end or 45 μfd decreases the amplitude 17.5 percent to 2.5 percent of charge.

Therefore:

17.5% of 35V = 6.125V change

or:

Min to max range = 28.875V to 35V

5-8. **Adjust a Pulse Generator.** A pulse generator, such as a one-shot MV, single-shot MV, or monostable MV, can be designed to provide a variable pulse-width output signal. Most frequently, the device used is a POT.

5-9. *Use of RC time constant.* The pot may be installed in the input circuit or in the output circuit. In either case, it is usually installed in the emitter or collector circuit of a transistor MV. Its primary function is to alter the RC time constant of the circuit, thereby causing a shorter or longer decay time. This allows the circuit to provide a varied or adjustable output pulse width. Most of these circuits require a trigger input to cause a change in states. From a quiescent state a trigger may be applied to either the base or collector to cut off the conducting transistor or bring into conduction the cutoff transistor. This action causes the MV to switch states. The decay time of the RC circuit controls the conduction period of the entire circuit by maintaining bias values until the voltages decay through circuit RC components to the point where the circuit reverts to its original state.

5-10. Refer to figure 43 (printed in the workbook), for an example of miniature potentiometers being used with an integrated circuit. The operation of pots R3 or R4 is very similar to the uses already described. Their primary function is, once again, variable control; when each is used with a 3.3K resistor and an 8-picofarad capacitor, an RC network is formed. Study figure 43 closely during the discussion of pots used in pulse generators.

5-11. *Integrated circuit with RC pulse-width control.* The circuit consists of integrated units Z1 and Z2, and external to the ICs are pots R3 and R4, both 20K. Resistors R5 and R6 are 3.3K each, and capacitors C1 and C2 are 8 pfd. On each half of the IC, Z2 is a Schmitt trigger circuit. The primary function of a Schmitt trigger is to provide a rectangular waveform output whenever the input is caused to change states. If the input is a low-frequency AC signal (i.e., 60 Hz), the input circuit delays its reactions to the input until the controlling slope of the signal reaches an amplitude sufficient for the change to occur. No change in output results until reaction occurs.

5-12. For instance, if the input waveform takes 50 μsec to rise high enough to bring the input circuit out of cutoff, the output has no reaction until the change takes place. On the other hand, if the input is rectangular and the rise time is 20 nanoseconds or faster, the output reacts almost instantaneously. Considering these factors, examination of the circuit in figure 43 (printed in the workbook) shows that the input AND gate Z2A requires three high inputs on pins 1, 13, and 14, plus a high from pot R3. Since this AND gate has pins 13 and 14 tied to +5VDC, pin 1 causes the Schmitt trigger to start operation. R3, R5, and C1 form an RC network for pulse-width control. The maximum and minimum times derived from the formula T = RC reveal two conditions: (1) a time of 20 nanoseconds with the pot effectively removed, and (2) a time of 187 nanoseconds with the full pot in the circuit. This variable component controls the conduction times of the input circuit of the Schmitt trigger and consequently delays the completion of the rectangular output waveform.

5-13. The Z1A NAND gate provides a pulse when the inputs to pins 12 and 13 are high. A negative pulse is fed to pin 1 of IC Z2 AND gate Z2A. On the rise of the output signal from NAND gate Z1A, the trigger is turned on, and an output is generated from the

Schmitt trigger. The length or pulse width of the output pulse is dependent upon the value of the RC circuit consisting of R3, R5, and C1. Their sizes provide a time constant value, which causes the Schmitt trigger to stay in its ON state. The delay resulting effectively stretches the pulse. R4, R6, and C2 and the second Schmitt trigger unit do the same thing.

5-14. With this understanding of circuit operation, performance of the adjustment routine shown below has meaning:

- Set up scope for 5V at 0.1 nanosecond—each channel.
- Adjust trailing edge control R3 fully clockwise.
- Adjust leading edge control R4 for maximum value (as near to 600 nanoseconds as possible) while looking at TP20 on channel 1 of the oscilloscope.

5-15. This is a primary example of the simplicity of instruction taken from a -9 (alignment) TO, and it focuses on the point of this discussion that a knowledge of circuit operation is needed if for any reason the pulse width does not measure 600 nanoseconds.

6. Adjust Power Suppliers

6-1. The following four quotes from PMIs show the simplicity of power supply adjustment instructions:

Adjust power supply control R25 for a 15V ± .01V output.
Adjust R8 for a meter reading of -15VDC.
Adjust the 390VDC power supply for 390V ± .5V.
Adjust R16 for a voltmeter reading of 15VDC.

The first and third examples reflect an exact percentage of deviation and, because they do, the use of a differential voltmeter is required. On the other hand, instructions two and four specify voltage taken from a meter installed on the power unit. The adjustment of any of these pots consists of varying the resistance to the load at the output of the supply. By varying this component, conduction in the circuit is varied and output voltage indications show the new value.

6-2. If adjustments are made using a differential meter, the output of the power supply is measured against the output of the calibrated meter and the adjustment potentiometer on the supply provides the control.

6-3. Most regulated power supplies are complex units and require extensive study. For this discussion on adjustments, a brief review of their makeup provides the basis for understanding. The output of a regulated supply is distributed to many circuits. The output voltage is usually adjustable within limits. The output current may or may not be adjustable and visually measured; however, its value is considerable. It may be as much as 100 amps.

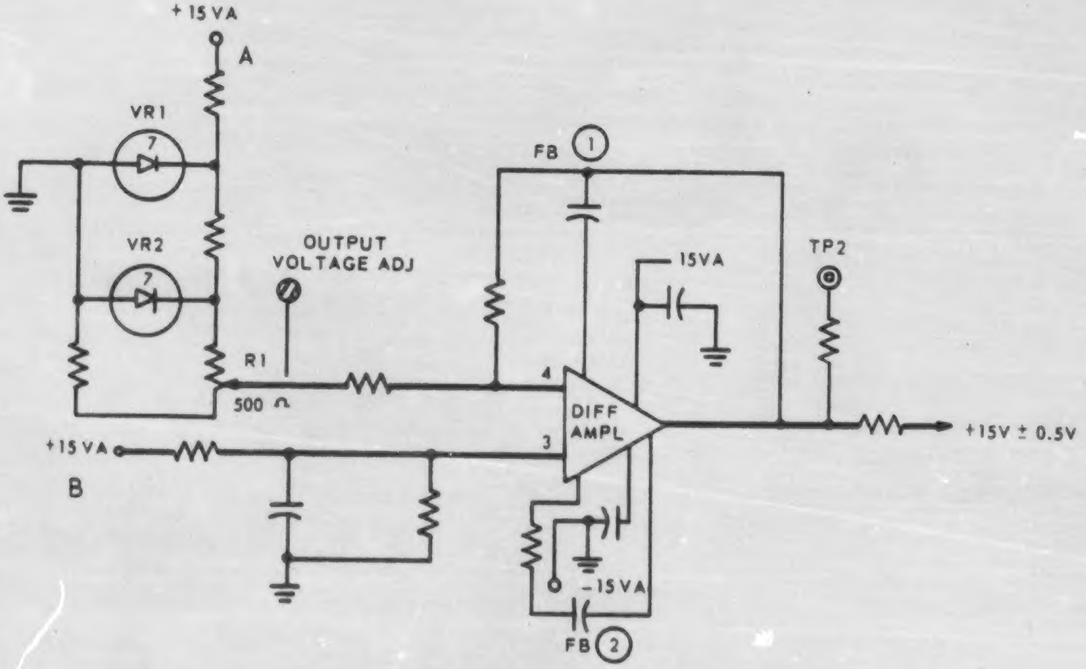


Figure 44. Differential amplifier voltage regulation.

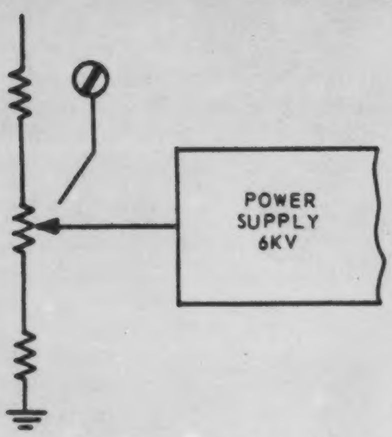


Figure 45. High-voltage adjust.

6-4. Low Voltage. To have this much current at the low voltage required for transistor and integrated circuit operation necessitates the use of extensive front-end circuitry. Common electronic components such as *silicon-controlled rectifiers*, *zener diodes*, *thermistors*, and *thyratron semiconductor devices* are all used to provide current and voltage regulation. Filtering is accomplished by extensive use of coils, capacitors, and resistors. Finally, the source input is frequently 400 Hz instead of 60 Hz because it is easier to filter.

6-5. In figure 44, VR1 and VR2 are zener diodes used in conjunction with R1, a 500-ohm pot. They provide a variable +15V signal to one input of a differential amplifier. The other input (pin 4), also a +15V signal, is inverted in the first stage of the circuit. The output is regulated by developing a difference between the two inputs which, when added to the gain of the amplifier, regulates the output voltage to +15V ±0.5V. The RC network provides filtering for high frequency induced by amplification of noise. In this example, the control is included in the input circuitry. This illustration points out again the usefulness of potentiometers and the variations of their arrangement in circuits.

6-6. High Voltage. Most high-voltage power supply test points and adjustment controls are isolated. Frequently, the potentiometer is connected to a voltage divider network from infinity on one end to ground on the other. This arrangement is shown in figure 45. The wiper arm, however, has a very high potential since it has a voltage equivalent to the power supply. Caution must be used because of the high voltage present, even though the controls and test points are isolated.

7. Adjust Timing Devices

7-1. Almost without exception, timing units incorporate crystals. The extremely-high stability of these solid-state structures has accounted for remarkable advancements in newer computer equipment. Many crystals are encased in ovens in order to insure proper operating frequencies. Many crystals are cut for negative or positive coefficients which require engineering solutions. Advanced technology and manufacturing skills have provided solutions to most of industry's demand, and the result is that little maintenance of the timing units of the newer computers in the Air Force inventory is required.

7-2. Time and Frequency. One of the oldest data processors in use in the Air Force is the AN/FST-2B. It is used to collect and process data for use in the SAGE system, and it transmits the data to the AN/FSQ-7 computer at a direction center. The T2 uses a 323.44-kHz crystal in a pulse Hartley oscil-

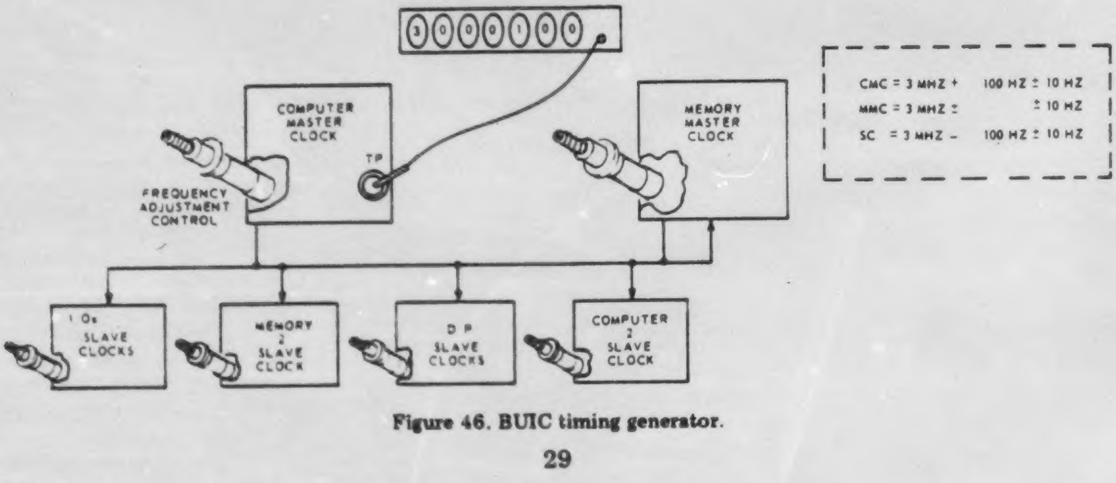


Figure 46. BUIC timing generator.

lator to provide frequency stability. When properly adjusted, pulses from the oscillator are generated each 3.09 microseconds. In adjusting the frequency of the oscillator, the output of the circuit encompassing the crystal is measured. When its amplitude is at peak, the circuit is operating at the frequency of 323.44 kilohertz.

7-3. The AN/GPA-73 air weapons control system uses a basic 1-megahertz crystal-controlled clock. The output feeds local clocks which, in turn, divide this timing generator output into 64 reference pulses of various pulse widths and pulse repetition times. Timing adjustments in this system are extensive and are made with potentiometers. The master clock circuitry provides for adjustments of the output frequency by trimmer capacitors. The calibrated output must be measured with a frequency counter and must be 1 megahertz plus or minus 1 hertz.

7-4. The AN/FSQ-7 uses a 2-megahertz, crystal-controlled, reference generator. Its output frequency variation also is exacting.

7-5. The AN/GSA-51 BUIC system uses a 3-megahertz timing reference generator. Its crystal-controlled timing generator is set by tubular capacitor adjustment to 3 MHz + 100 Hz ± 10 Hz. By referring to figure 46, the block diagram of the clock generation circuit of the BUIC, you can see that:

a. The computer master clock (CMC) is set by the adjustable capacitor to a frequency of 3,000,100 hertz ± 10 Hz.

b. Each slave clock (SC) is set for a frequency of 2,999,900 hertz ± 10 Hz.

c. The memory master clock (MMC) is set for exactly 3 MHz ± 10 Hz.

7-6. With these frequency variations, it becomes easy to see that the CMC does all controlling when operative and causes the slave clocks to speed up to 3 megahertz. If the CMC clock fails, the MMC clock which is still running faster than the slaves causes the slaves to speed up and the system still runs at 3 megahertz. If both MMC and CMC fail, the system fails; however, the SCs are used for local testing.

7-7. The MD 452 modems used with the SACCS employ a crystal-controlled reference generator. This unit uses ovens for frequency stability. Its requirements are for 100 kilohertz, plus or minus 1 hertz. Adjustable trimmer capacitors (button type) are included for frequency adjustment.

7-8. The MD 807 modems used in 407L tactical control equipment use a crystal which is also encased in an oven. However, this crystal and associated circuit has no frequency compensation controls. Its crystals are cut to oscillate at 10.36 MHz and 1.0752 MHz. The crystals feed frequency dividers which are manufactured with variable pulse width and amplitude resistive controls.

7-9. While the T2, GPA-73, and BUIC have reference clocks for central timing, 407L uses many different clocks. The computer uses a 4-megahertz clock, and displays use 20-MHz, 10.36-MHz, 1.0752-MHz, and 1.67-MHz clocks. All are crystal controlled.

7-10. In addition to central or master timing, many other timing circuits are used. Some of these are:

- Free-running oscillators.
- One-shot multivibrators.
- Blocking oscillators.
- Time-sharing circuits for displays.
- Automatic gate length (AGL) generator for use with radar returns.

7-11. In each case, a variable control is usually incorporated and frequently it is resistive used for control of voltage amplitude.

7-12. Let's look at the facts we have covered so far. First, variable capacitors of both the button and tubular type are used for controlling frequency. They are normally found in circuits used for master timing and are often found in display timing units. Second, resistive variable controls in master timing units are usually in the output for amplitude control. They are also used in other timing circuits to control *pulse width*, *pulse repetition rates*, and *amplitude*.

7-13. **Timing Routines.** Timing routines fall in two broad categories:

- The frequency adjustment of a crystal-controlled oscillator.
- The adjustment of a duty cycle.

7-14. The frequency adjustment is made with a frequency counter externally connected to the oscillator output. The frequency control is adjusted until the counter reads the precise value of the performance standard.

7-15. The duty cycle adjustment is usually measured on an oscilloscope. A basic reference pulse is usually displayed on either A or B trace and the waveform of the circuit to be adjusted is displayed on the other trace. Calibration of the waveform is performed and adjustment of the duty cycle is performed by altering the variable component in the circuit under measurement. If an amplitude variable is included, the instructions usually specify

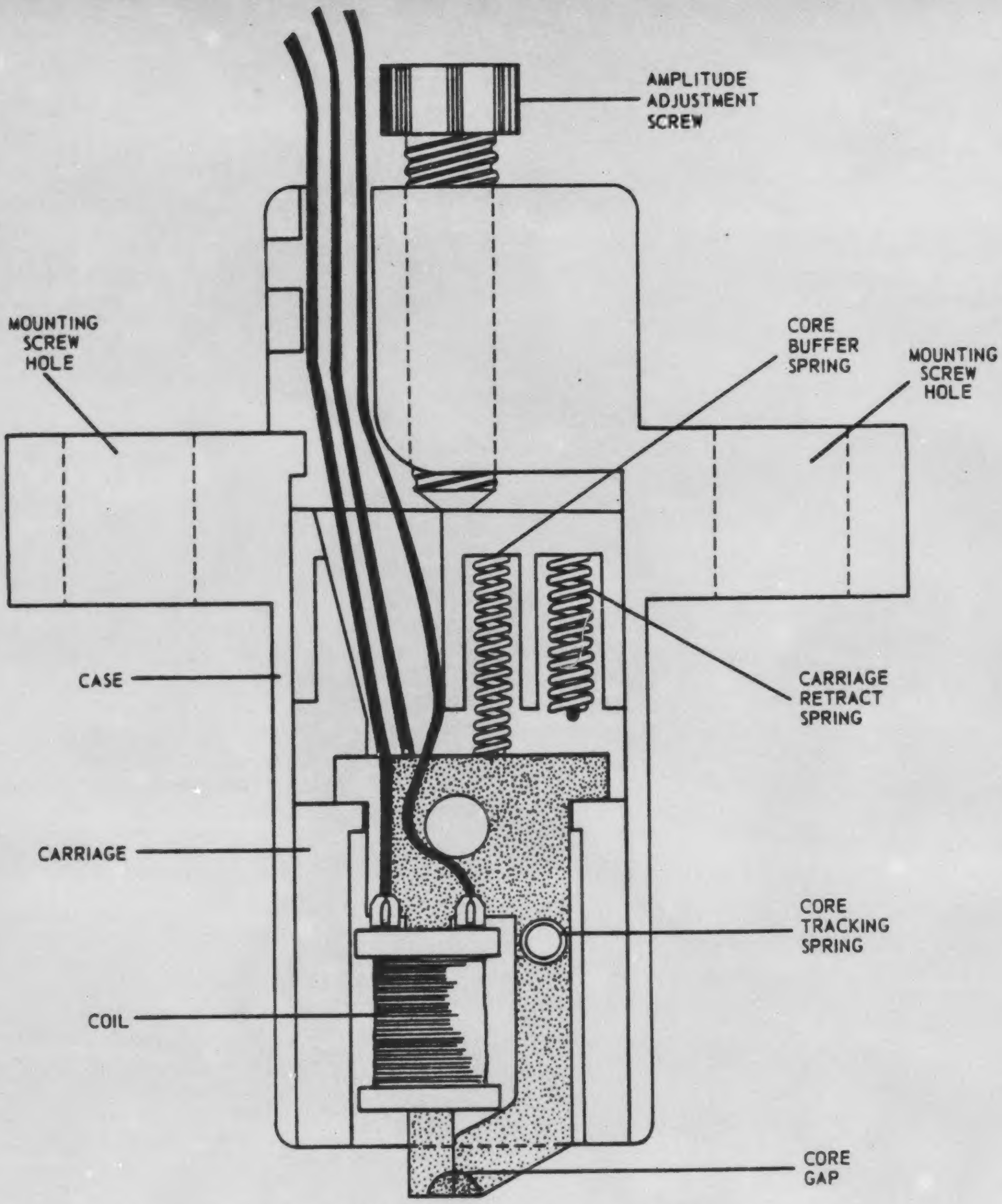

AMPLITUDE ADJUSTMENT SCREW
MOUNTING SCREW HOLE
CORE BUFFER SPRING
MOUNTING SCREW HOLE
CASE
CARRIAGE RETRACT SPRING
CARRIAGE
CORE TRACKING SPRING
COIL
CORE GAP

Figure 47. Read/write head, Q7, T2.

the amplitude plus or minus a specified deviation.

7-16. **Technical Orders.** Once again extensive use of the adjustment/alignment manual, the -9 TO, is made. In addition, checks for circuit operation are made with the preventive maintenance manual, the -WC6. If repairs are made and circuits realigned, both the maintenance chapter of the service manual, the -2, and the alignment manual, the -9 are used.

8. Adjust Storage Devices

8-1. During a study of storage devices and their adjustments, a significant factor developed. The adjustments performed were divided into two separate, significantly different, subtasks. One was mechanical adjustment and the other was electrical adjustment using an electronic component. One might say that any adjustment, even a pot, is mechanical, and in the truest sense this is correct. In this study, mechanical adjustment indicates the physical altering of components to specific distance, even though the distance is measured in voltage amplitudes. Electrical adjustment is construed to mean a variation of a pot or capacitor to provide a standard waveform or level.

8-2. Based on these premises, mechanical adjustment can be readily associated with drum systems, tape systems, and disk systems, since each has the same principle of depositing data and extracting data through a magnetic head. The electrical adjustments can be associated with the systems listed above and also with core systems, thin film, electrostatic storage tube systems, delay line storage systems, and some integrated circuit storage systems. In these systems, electrical adjustments are performed on components external to the storage device in almost every case. During this study you will see that this is true.

8-3. **Mechanical Adjustment Principles.** The *drum storage device* consists of many channels, and each channel has read/write heads and usually an erase bar. Each head is secured to a frame which is designed to place the head very close to the drum surface. This is nothing new to you since you have already studied drums. The read/write head assembly on the AN/FST-2 or AN/FSQ-7 is similar in construction, and is shown in figure 47.

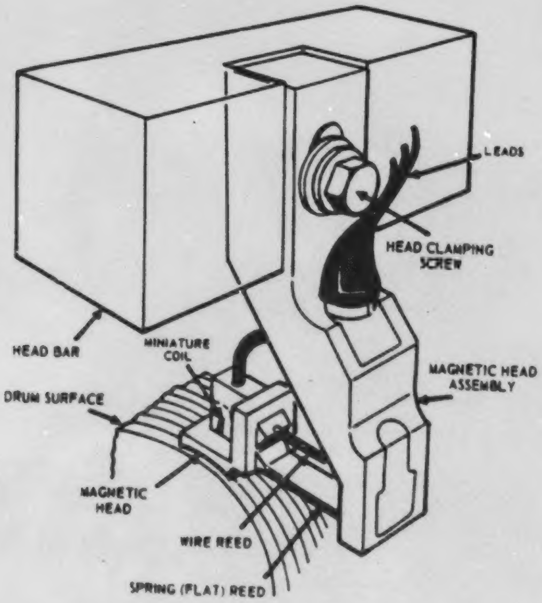


Figure 48. Read/write head installed.

8-4. *Drum head adjust.* The assembly is approximately 1¼ inches wide by 3/8 inch thick. It contains two mounting screw holes on the flanges and internal coil, the heart of the unit. The amplitude adjustment screw allows the carriage to move up or down, closer to or farther away from the drum surface. The adjustment routines require that data in the form of a binary one be written onto the drum channel being adjusted. The pulse is measured on a dual-trace oscilloscope with one trace measuring the input waveform and the other trace measuring the output waveform. Adjustment of the head for the Q7 requires that an output voltage be measured at 125 to 150 millivolts peak to peak. The steps to arrive at this voltage output are such that the head is lowered to the stopped drum surface and then raised until 75 percent of the voltage waveform is displayed on the scope.

8-5. Ten years of progress and advanced technology have brought simplification to the drum head units, as shown in figure 48. This BUIC read/write head is smaller, simpler, and uses spring steel (spring flat reed) to hold the recording head near the drum. It incorporates a miniature coil that is approximately 1/8 inch square. The techniques for adjustment are similar to those for adjusting the older models in that a binary one is written into the channel and the readout voltage is measured while adjustment is being made. Special tools are required to adjust this system. The pivot screw shown on the left in figure 49 (printed in the workbook) secures the adjustment tool to the head mounting bar, and the adjustment screw controls the positioning of the head. The head clamping screw is tightened and the task is complete.

8-6. *Tape drive adjust.* On tape drive systems, mechanical adjustments are usually associated with the drive mechanism rather than the heads. Most heads are installed in a metal container and are recessed from the outer surface of the container 3/1000th to 7/1000th of an inch, thereby providing the required gap for magnetizing the tape. One tape system uses shims to raise the tape .003 to .005 inch from the tape head.

8-7. Mechanical adjustments vary in accordance with the design features; however, they are common in that the proper drive speed, stop, start, and tension must be maintained. For instance, in the format message composer of SACCS, there is a sprocket adjustment which provides the required tension for the tape as it passes over the read/write head.

8-8. On the tape drive units, a pinch roller is adjusted by use of shims, and so is the brake. The vacuum pump adjustment is made

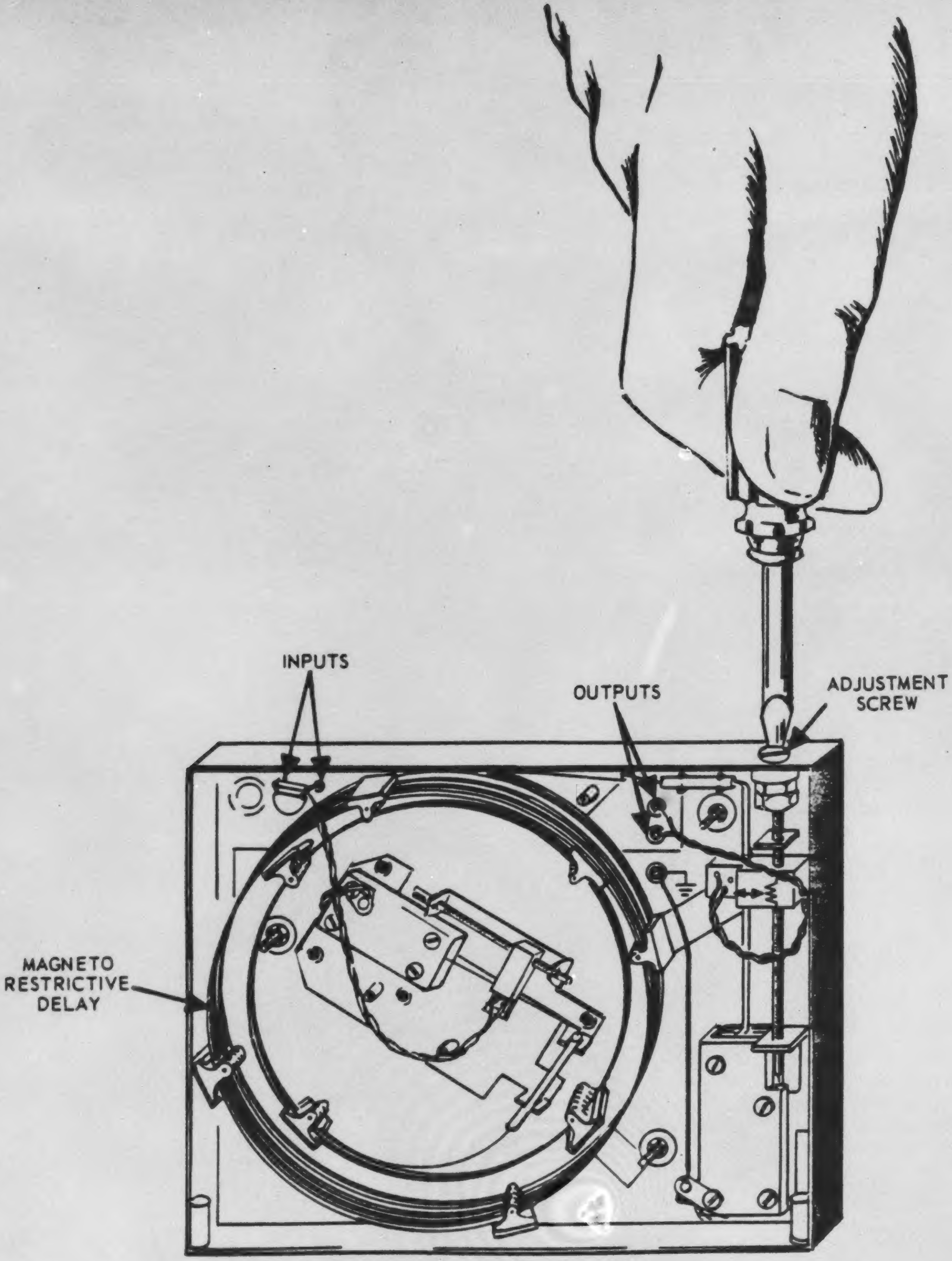

INPUTS
OUTPUTS
ADJUSTMENT SCREW
MAGNETO RESTRICTIVE DELAY

Figure 50. Magnetorestrictive delay line.

so that the water gauge shows a reading of 40 inches, plus or minus 5 inches. Also, adjustments are made on belt-driven assemblies at the time that corrective maintenance is performed. They involve the driven capstan, vacuum pump motors, and rewind motors.

8-9. *Delay line adjust.* The magnetorestrictive delay line storage system incorporates a mechanical adjustment device, tunable to a precise position. The principle of storage with this device is shown in figure 50. A silver wire is used as the storage element with approximately the last 16 microseconds variable. Current in the form of a short duration pulse is entered into the wire at one end. It travels down the wire at the rate of approximately 1100 feet per second. Since its rate of travel is linear, the selection of a precise length then identifies two facts: (1) the time delay of the pulse is known by the length of the wire times the rate of travel, and (2) if the pulse (data bit) occupies a precise measurement of length along the wire, a specific number of data bits or words may be stored. Access to data at the output is sequential and any selected data can be sampled if its entry time and the total length of the storage line are known. The adjustment of the last few microseconds becomes a critical factor and precise timing is necessary. Two methods are used for making the adjustments. First, an oscilloscope using two traces may be used. On one trace the input pulse is shown; on the other trace the output pulse is shown. Since these are the same pulse, the measurement of time between input and output reveals the delay or storage time. Adjustment can be made to display a precise known delay storage time. The second method is performed by using a test setup designed and built for adjusting these storage devices. The principle used is that switches program the tester's internal circuits, thereby providing pulses and measuring pulses at specific times. The pulses are then displayed by use of neon lights. The first light to come on is interpreted to indicate that a close setting has been achieved and the second light indicates an exact setting.

8-10. *Disk memory adjust.* The disk memory system is related to the juke box in that the disk rotates and the heads are placed above and below the recording disk. Figure 51 (printed in the workbook) shows a cutaway view of a disk memory unit. As is true with other storage devices using magnetic recording, there are mechanical and electrical adjustments. The mechanical head assemblies are adjusted by screws installed in pivot arms. These are shown in the breakout of figure 51. The heads are adjusted with shims and the use of a micrometer. From figure 51 you can see that the heads are placed in various positions around the disk. Examine callout 1 of figure 51 and you can see that the head bar has an adjustment called a *pivot screw.* The head bar is shown more clearly in callout 2 of figure 51. Once again, extensive use of mechanical adjustment is made on storage devices.

8-11. **Electrical Adjustment Principles.** Current is required to write a one onto a storage device, and all systems use drivers to accomplish this. The current is almost always the result of a decoding action of data. A binary one will usually cause a circuit action which converts the digital one into a current pulse of the proper polarity for use in a magnetic storage medium. The device most generally used is the write amplifier.

8-12. *Read/write amplifier adjust.* Almost all systems use write amplifiers and read amplifiers. These amplifiers usually have potentiometers installed for fine adjustment. They may be current-limiting or voltage-limiting, or both. They are usually adjusted to specifications as performance routines. A study recently completed of some of the weapons systems reveals that all tape storage units have either a read amplifier or a write amplifier adjustment pot, but some drum storage systems have neither. One drum sys-

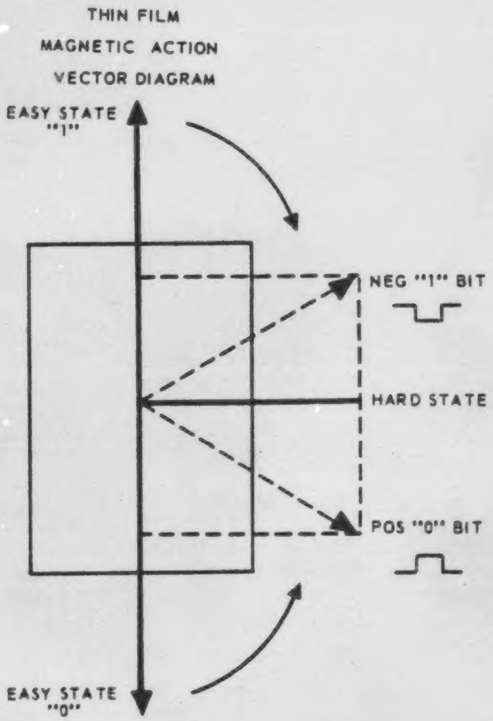


Figure 52. Vector diagram thin film memory.

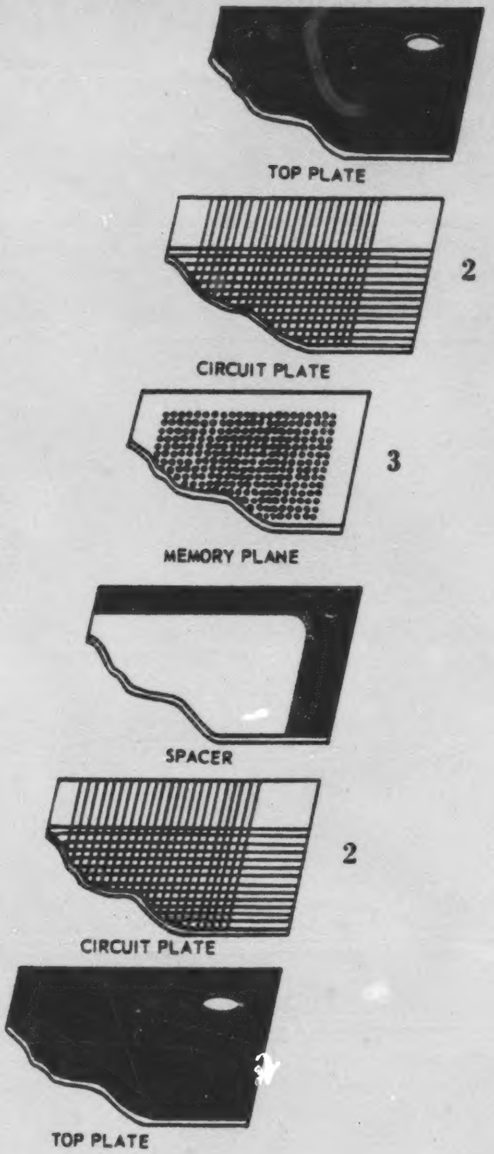


Figure 53. Thin film memory.

tem uses a current-limiting memory protection circuit with adjustment pots to regulate the current requirements for the entire drum unit.

8-13. *Thin film circuit adjust.* Thin film memory systems provide a nondestructive readout after storage of data. This is done by reading a current amplitude of slightly less than switching current or hard state, as is shown in figure 52. The adjustments associated with this memory system are made on the read/write amplifier units. Coincidence of two pulses is required to provide the switching current necessary for storage of data.

8-14. The principle for write needs a coincident address current plus a write current sufficient to cause switching. To read requires a coincident current, but one that is not high enough in amplitude to cause switching. The diagonal dashed line in figure 52 is the read value for either a one or a zero.

8-15. The makeup of a thin film storage unit is shown in figure 53. The storage area consists of dots of magnetic deposits (3) within a grid of coincident connectors (2). Each dot is capable of acting as a core and is addressed in a similar manner. The primary differences are the physical makeup and the nondestruct readout or data loss from loss of power.

8-16. *Storage tube adjust.* The electrostatic storage tube is a device using a modified CRT to allow operators to view its stored data. You may use variations of this tube. One is called the memoscope. The principle of operation is shown in figure 54. Data is written by the high-velocity write gun through the collector screen onto the storage screen. The flood guns scan the screen and every point on the storage screen where data is present (+ voltage). The flood voltage penetrates and illuminates the CRT phospher. As is true in drums and core storage, the applied voltage and current are controlled by pots. They control scanning, unblanking, video data levels, flood gun intensity, and storage and collector screen erase.

8-17. *Integrated circuit display (CRT) adjust.* One system previously using the storage tube had the circuit redesigned to use a simpler more modern design. Figure 55 (printed as a foldout in the workbook) shows a view of the control panel including all the potentiometers, a view of the CRT and integrated circuit packages, and logic and circuit diagrams. The simplified circuit eliminated the storage scope with its six mechanical centering controls for pitch and yaw, its eight stepping voltage adjustments (four for horizontal and four for vertical), and its two intensity controls. The new system operates on a principle of storing the data to be displayed in a recycling storage buffer (not shown in fig. 55). The data from the buffer programs the memory IC storage, figure 55,B, which provides an output to digital to analog converters, 1 and 2 in figure 55,D. The character voltage from the D/A converter is added to a vertical and horizontal stepping voltage, and these voltages are applied to the deflection plates. During intensity time, the character is painted. The controls, all pots, adjust for:

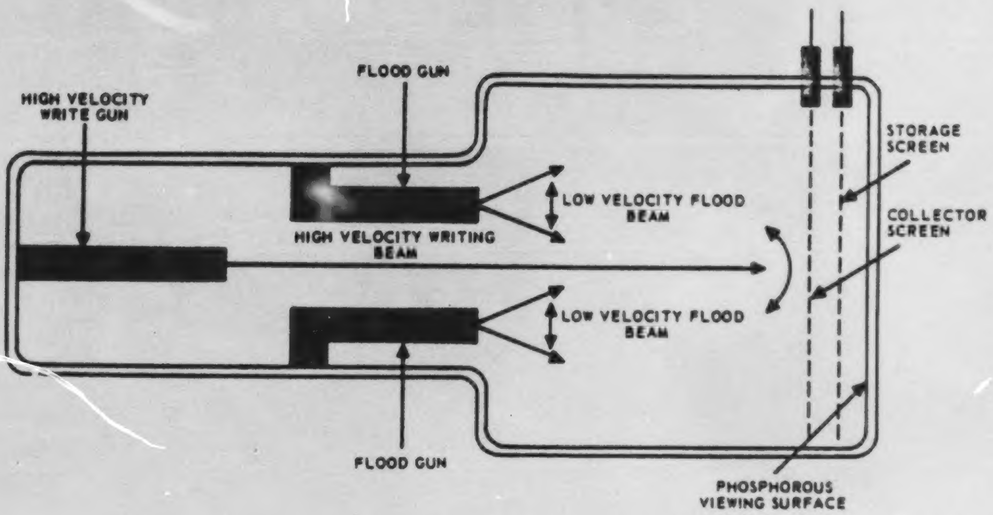


Figure 54. Electrostatic storage tube.

(refer to fig. 55,A)

- Character width and height.
- Position vertical and horizontal.
- Character spacing vertical and horizontal.
- Intensity.

8-18. Let's study figure 55,A, the alignment panel of the digital informational displays (DID) unit. The upper third contains three potentiometers, all contained in a serial voltage divider network with one end tied to soucre voltage +13 volts and the other end to ground. Tracing back to its use, each wiper arm feeds to the D/A converter board. R11, vertical gain, feeds to an amplifier (shown in 2 of the D/A converter (D)) to the high-order bits decoder. The symbols shown are really transistors acting as switches. The output voltage of the high-order bits is determined by the binary count input. It may be 0 through 15. Each count biases one or more of the transistors and the algebraic sum of the four, plus or minus the variable gain of R11, through the amplifier provides a deflection voltage for the vertical deflection plates. The unit is capable of providing 16 stepping voltages; however, by looking at figure 55,C (printed in the workbook), you will see that only 10 vertical positions are used.

8-19. The next in the series of pots is the *character height pot*. It allows the increase and decrease of the vertical size of the individual characters. The voltage from the pot is fed to the lower order bits decoder. The variation in size, therefore, is restricted by the allowable parameter of the decoder.

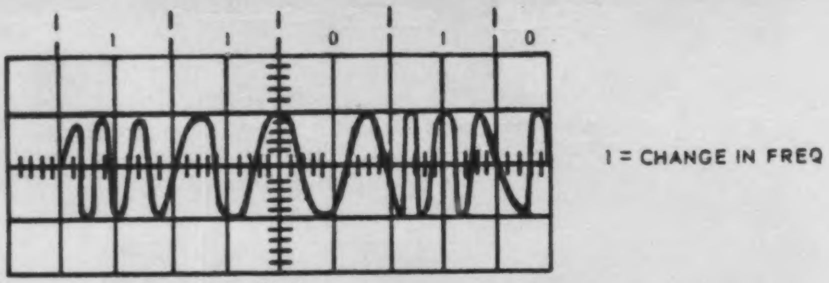
8-20. The third control (vertical position) voltage is fed to the differential amplifier. This control determines when the difference output occurs. It does not alter the character size. It provides a control for positioning the characters in a particular position on the CRT.

8-21. To show you the effects of the pot as displayed on the CRT, look at callouts 1, 2, and 3 of figure 55,C. Callout 1, the vertical gain, alters the stepping voltage to the plates. Therefore, it provides more or less stepping voltage and causes the display to vary as shown. Callout 2, the character height pot, controls the size of the character within the space allotted for the character. The difference in size is shown in callout 2 of figure 55,C. Callout 3, the vertical position control, moves the display up and down, as shown in figure 55,C, but does not affect the size.

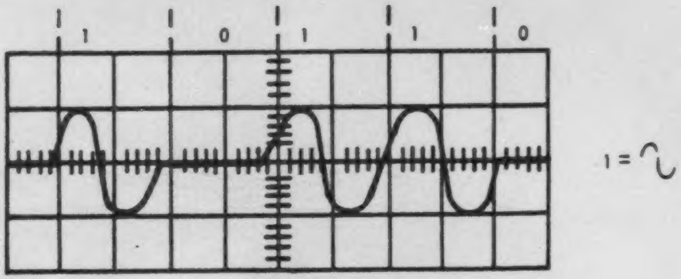
8-22. Returning again to the schematic of the alignment panel (fig. 55,A) the upper shaded area of the panel shows a similar arrangement for the horizontal control of characters. Notice, though, that R5 is 2.5K ohm where R11 in the vertical unit was 1K ohm. The additional variable resistance is provided because the display is wider across than down, and more stepping voltages (16) are generated. The controls provide the same functions as the vertical controls.

8-23. The right side of the alignment panel (fig. 55,A) shows a bezel (rim) light control knob and, more important, an intensity amplitude control for overall brightness of the CRT display.

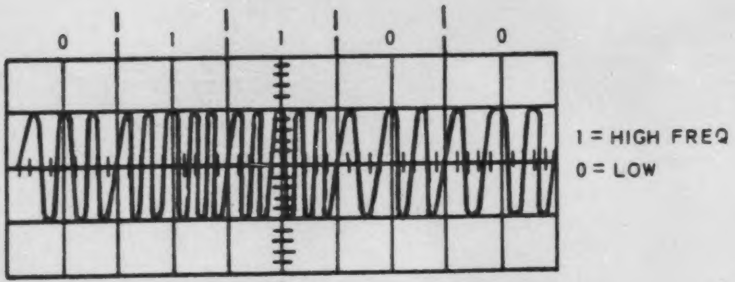
8-24. From this study of adjustments, you can see that adjustments are many and varied. The final area of application in this study is



FSK



DIPOLE



FSM

Figure 56. Transmitted data (FSK, FSM, dipole).

the adjustment of data input and output circuits.

9. Adjust Data Input and Output Circuits

9-1. Both potentiometers and variable capacitors are used in establishing the correct data levels within the input and output circuits of the computer, data processing, and communications systems. Since some systems use more than one type of data entry or exit, this discussion shows where typical adjustments are performed according to type of data. The data inputs and outputs can be separated into many classes, but for this study these three were chosen:

- Digital data.
- Video data.
- Electronic data convertible to or from digital.

9-2. **Digital Data.** Digital data is that data which is transmitted from one unit to another via landlines (TELCO), troposcatter, or microwave. The system of transmission involves primarily frequency shift keying (FSK), dipole, and frequency shift modulation (FSM). Although we covered FSK and dipole in Chapter 1 of this volume, review their forms in figure 56. Each time, in FSK, that a binary one is transmitted or received, the circuits sense and process a change in frequency. Contrast the dipole data where each binary one is represented by an AC pulse and a binary zero is represented by a level. The FSM not previously discussed, but shown in figure 56, combines some of both systems in that frequencies are modulated—one representing a binary one and one representing a binary zero. In all three cases, timing is related since the speed of sampling of the pulses corresponds to the data content.

9-3. Adjustments performed upon circuits using these systems of data transfer use both pots and variable capacitors. The pots primarily control amplitude and pulse width. The capacitors affect frequency amplitude and phase control. Adjustment routines require the use of measuring devices, frequency counters, and oscilloscopes. Some of the common names applied to these input/output units are:

- Message processors.
- Modems.
- Modulators-demodulators.
- I/O units.
- Transmitters or receivers.
- Decoders or encoders.

9-4. Video Data. As we discussed in Chapter 1 of this volume, radar and SIF may be provided in many forms, from raw to digitized. Radar sets, of course, receive a *very* small pulse return, and the amplifiers within the set boost them considerably. If the return is digitized within the radar set, all target returns are presented to the data processing unit at a standard pulse width and amplitude. The data processor input unit might then have amplitude pots as controls, but not much more. However, if the data is selectable by personnel using the data processor where digitized, raw, or processed radar enters the input circuitry, extensive use is made of variable components. Capacitors are incorporated to provide gain control for high-frequency pulses, and potentiometers are used for low-frequency (DC) pulse control, pulse-width control, duty cycle control, and bias control. Some of the common names applied to these units are:

- Quantizers.
- Video amplifier units.
- SIF processors or beacon input processors.

9-5. Electronic Data Convertible To or From Digital. The units providing data to input/output units in this category are:

- Punch card readers.
- Teletype.
- Printers.
- Video printers.
- Paper tape machines.
- Keyboards.

9-6. Many of these units have adjustment controls installed in their circuitry which eliminate the need for the data processor or computer to have adjustable components in their input/output circuits. For instance, a certain card reader has two controls—one for pulse-width adjustment and the other for timing of a strobe pulse generated by a saturable reactor. Then there is a selection control within another unit with a variable amplitude control for each level. Some printers and keyboards have variable mechanical and electrical controls, so input/output units do not use them. These are examples of adjustments being provided on I/O equipment feeding to or being fed from data processors or computers, or communication equipment. The data codes used by these devices differ from both the digital input data and video in that frequently the data is converted to current pulses, is fed in parallel, travels at a higher rate of speed, may be completely digital at prescribed logic levels, or is converted to digital from relays and switches.

Alignments

THE BRINGING together of individual elements to provide an overall function is the primary concept for the performance of alignments.

2. In Chapter 1 of this volume, operational performance checks were identified and analyzed. These checks were made almost entirely upon functional circuits which provided a specific output that was necessary for the entire equipment to perform. Some of the checks took into consideration only small segments of the equipment, such as video amplitude validation. Others checked the entire unit as in the case of a printer.

3. From this study, we developed Chapter 2 and analyzed the variable component which was used to make the individual adjustment. The analysis brought out that adjustments involve individual circuit elements, as well as interconnecting and interrelating circuits, and often other functions.

10. Alignment Concept

10-1. Combining the objectives of these two chapters aids in acceptance of the concept that for alignment to be meaningful and effective, a complete understanding of the overall function of the circuits within the alignment is essential. The principal objectives and selected applications are identified, explained, and analyzed in the paragraphs that follow.

10-2. **Principal Objectives.** Look at the man in figure 57. Does he resemble someone you have seen a few times during the short period that you have been in the work environment? He is well equipped. He has his alignment technical order, test equipment, plenty of leads, and a job order. He is going to align a complex piece of computer equipment. Do you think that he will do a good job? In all probability, he will, because the instructions written in the alignment TO are clear and specific, and the standards are specified.

10-3. This man was praised for doing an efficient job on the alignment, but 2 hours later the equipment he aligned went down. Back to the equipment he went, only to discover that he did not know what caused the failure.

10-4. We all know that a failure can occur at any time, but consider the close time interval between the completion of an alignment and the failure. Is one act the cause of the other? Is there more to performing an alignment than completing the steps of a given routine? What may some of these answers be, and how could they relate to improving an idividual's work? How can answers to these questions be used to improve the mission of preparing the man? Let's see if we can break down the performance of alignments into some significant elements.

10-5. *Identify the basic objectives of the alignment.* Our man in the figure learned to perform the steps in the alignment. Did he understand the objective? He probably knew what it was from the title of the alignment routine, but did he realize that the title only identified a particular area, function, or subfunction of the equipment?

10-6. To identify the basic objective of an alignment routine requires more study than reading the title. It involves an in-depth study of all the related circuits, components, electronic principles, and work techniques combined. Figure 58 (printed in the workbook) illustrates that there are five major subdivisions of an alignment. The first subdivision is the alignment title and the objective of the alignment. The second element is the subunits, circuits, and components of the objective. The third element identifies the need to study interrelated functional units which have a bearing on the objective. The fourth element is the sequence of alignment of the interrelated functions and objective. The fifth element is the alignment of the objective. The first of these subdivisions is "determining the objec-

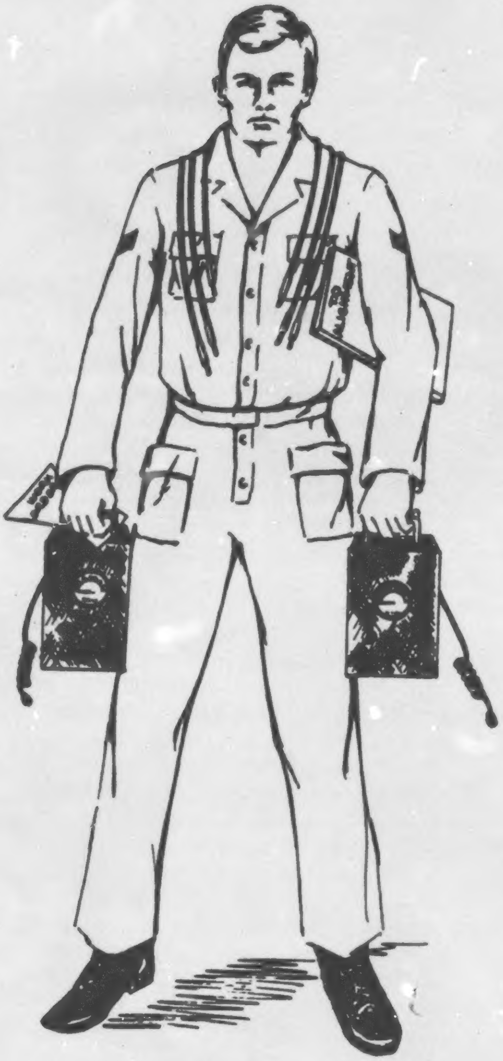


Figure 57. Alignment technician.

tive." Expanding part of figure 58 into figure 59, we identify that there are two requirements which are necessary in obtaining a clear definition of the objective. The study must *first include an examination of the specific alignment and the related technical orders.* This will determine:

- Various segments of the technical orders which would aid in understanding the objective.
- The data or signal flow paths which may be altered by the alignment.
- Specifications and limitations of the various steps involved in the alignment instructions.
- The theory of operation of the unit to be aligned.

10-7. The second element shown in figure 59 as being necessary to obtaining a clear definition of the objective is *electronic principles.* As an example, if integrated circuits are included in the system, their capability must be thoroughly understood. Their physical makeup must be identified. The maximum and minimum variations possible with variable controls must be studied. As we pointed out in Chapter 2, if a pot can only alter a circuit output by 10 percent and the measurements of the actual output vary by 20 percent, no apparent alignment can be made. Is the circuit containing the variable control isolated, or is it interrelated? If it is isolated, then a local problem exists and correction is required. If, on the other hand, the circuit is interrelated with another control circuit, the possibility exists that the other control circuit is causing the wide variation from the specification.

10-8. Combining the two elements of the study to determine the objective of an alignment establishes the primary purpose for the alignment. This purpose must be established in clear specific terms and must convey a specific meaning to you. It must identify either a major or minor function which the machine must perform. It must relate to theory of operation of the equipment. Finally, it must lead you to development of an in-depth study. The next logical step in the study of an alignment, as indicated in figure

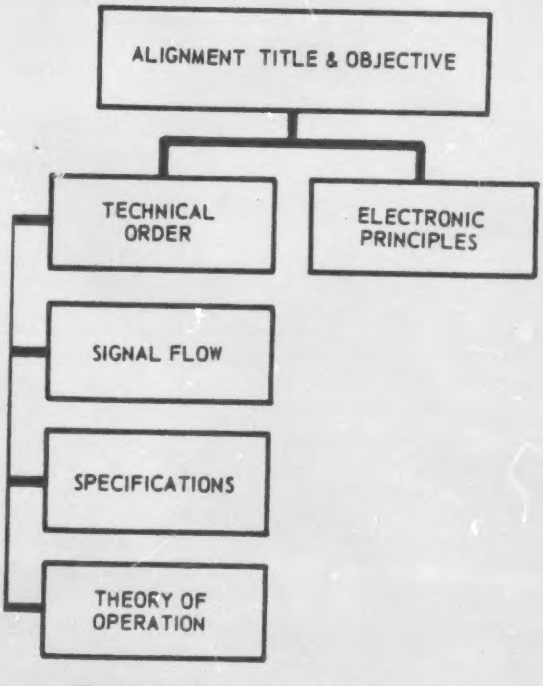


Figure 59. Alignment title and objective.

58 (printed in the workbook), is the identification of subunits or circuits which affect the main objective.

10-9. *Identify subunits or circuits which affect the main objective.* Almost without exception, a function of a computer system is made of multiple circuits. Some functions have no adjustment controls; others have one or many. If the circuits within the function contain only one control, understanding its operation is easy; so is the verification of its functional operation. The complete understanding of the function, however, is no less important. This is so because any circuit, either preceding or following the circuit containing the variable component, may have one or more of its parameters changed due to a physical breakdown of elements within the structures. For instance, heat affects all components and causes resistances to change, capacitances to change, or thermal runaway of semiconductor devices. Changes in current, caused by the structural changes in components, alter conduction parameters of these components and their related circuits. The variable control is primarily designed to overcome these factors, and it will compensate for some of them.

10-10. Figure 60 illustrates that when functions are broken into subunits (individual circuits), data about the function must include the items listed. In computers and processing machines, manufacturers have built circuits on printed circuit cards and then interconnected the circuits with wire or cable. To identify these circuits, you merely extract the circuits included in the function by:

- Identifying the alphanumeric in the alignments.
- Identifying circuit titles, parameters, and purposes.
- Locating them in the circuit and diagram manual.
- Placing the circuits, if not on the same pages, into a straight line (sequence) on a work pad to show initialization, processing, and utilization.

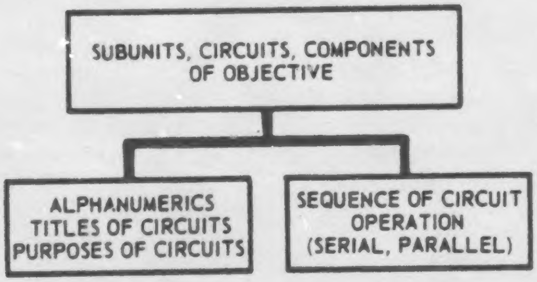

SUBUNITS, CIRCUITS, COMPONENTS OF OBJECTIVE
ALPHANUMERICS
TITLES OF CIRCUITS
PURPOSES OF CIRCUITS
SEQUENCE OF CIRCUIT OPERATION (SERIAL, PARALLEL)

Figure 60. Subunit, circuit information.

10-11. If, for instance, circuitry within a function contains an oscillator circuit and a flip-flop frequency divider, identify the oscillator as one block and the frequency divider as another block. If the function contains switching networks, amplifiers, and buffers, make a block for each circuit—one for the switching network, one for the amplifiers, and one for the buffers. Label each block. The separation aids in understanding relationships of circuits within the function. It also allows for listing selected necessary parameters of the individual circuits.

10-12. Because of the wide variety of circuit design and application, we cannot cover parameters in this CDC. However, in-depth understanding of them is essential to the understanding of the operation and alignment. Do not be misled by attitudes or comments that changing a printed circuit board (PCB) is always the solution to problems. This is a fallacy. This concept allows for restoration of equipment for operational purposes, but it does not identify causes of equipment failure. It does not answer questions about why the variable component in a function could not bring the function into line.

10-13. To cite an example containing this thought, consider that transistors are classed according to frequency passing capability; i.e., audio RF, VHF, etc., as well as current handling capability. We know that two space regions exist in each transistor—one between the emitter and base and one between the collector and base. Under normal operating conditions of a given circuit using transistors, these regions are the controlling elements. The amount of forward and reverse bias determines operation. We also know that transistor amplifiers have interelectrode capacitances, and the capacitance existing between these regions affects operation. Therefore, interelectrode capacitances may change under varying conditions and, when they do, they offer more or less reactance to the input frequency. This can cause a change in output frequency or amplitude.

10-14. Let's relate one more factor to this example. Most of the processing circuits develop rectangular waveforms, and we know that these are made from a basic frequency and infinite odd harmonics of the basic. If a partial breakdown occurs within the regions identified above and reactance changes, then some of these harmonics will be attenuated by the amplifier, and the output waveform becomes distorted. It may become integrated, differentiated, or begin to have ringing. It may increase or decrease in amplitude. It may

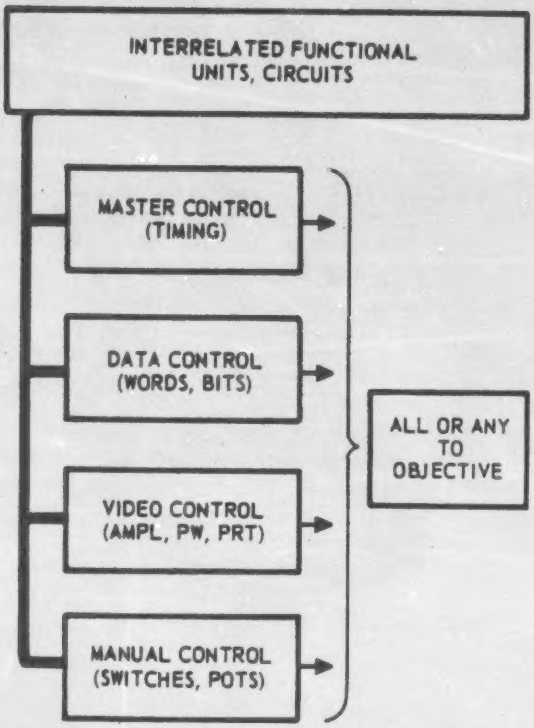

INTERRELATED FUNCTIONAL UNITS, CIRCUITS
MASTER CONTROL (TIMING)
DATA CONTROL (WORDS, BITS)
VIDEO CONTROL (AMPL, PW, PRT)
MANUAL CONTROL (SWITCHES, POTS)
ALL OR ANY TO OBJECTIVE

Figure 61. Interrelated functional information.

frequency shift, causing a delay in time.

10-15. This example typifies the need for analysis of an alignment to identify its elements. It furthers the need for basic electronic understanding of circuit design and interconnection, and it brings another significant element of alignments into view.

10-16. *Identify interrelationships of the function with other circuits or functions.* This element, illustrated in figure 58 (printed in the workbook) and amplified in figure 61, brings into focus the concept that very often functions other than the one being aligned must provide a discrete, specific input. An example, as shown, might be the timing unit supplying time share pulses at particular pulse widths and pulse recurrence times (PRTs) to a display unit.

10-17. Some system must be used in an alignment routine to identify external requirements. The system may be substeps in the first stages of the alignment and may require a verification of the externally controllable pulses. It may be a general statement stipulating the prerequisite that certain pulses be present in accordance with specifications. Or it may be sequencing of alignments within scheduling that provides the method for determining that all necessary controlled pulses are present in accordance with specifications.

10-18. Whichever system is used, the significant idea is that some people knew that preliminary steps must be performed. These people also knew and understood the entire unit operation. Therefore, they were able to sequence the necessary steps. They knew from research exactly which functional units or circuits provided inputs to the function being aligned. As shown in figure 61, any or all of the areas may play a significant part in allowing the circuits to perform. If these people knew the system, you need to know the system. Therefore, each interrelated function must be identified. Its title, purpose, and significant data input to the function under alignment must be listed. Using a separate block for each interrelated function allows for quick, sure identification of its influence. You should also include notations within the block about any and all controllable variables such as pots, capacitors, and data.

10-19. For an example of the concept stated above, refer to figure 62 (printed in the workbook). The figure shown in 806B symbology represents a functional alignment with other functions having bearing upon its function. Function A is the function to be aligned. Notice that function B must provide an output and, to do so, both signal 1 and signal 2 must be present at its input. Further, B is a functional unit which is in itself aligned. Notice that function C allows for the processing of either generator D or E, and both D and E are aligned.

10-20. We now have a situation where A's function is dependent upon its own internal circuits, parameters, and components, and also needs either (1) D processed by C, and B, or (2) E processed by C, and B. Consequently, the output of A could not be brought into proper specifications unless alignment of D, E, and B preceded A's alignment.

10-21. To point up this discussion, you need to analyze each alignment, using the technical orders to determine the complete picture. You must find if any interrelationships of function exist, what they are, and how they affect the function being aligned. This brings us to the next element of the objective as indicated in figure 58 (printed in the workbook).

10-22. *Determine the sequence of interrelated functional units and the objective alignment.* For overall success to be guaranteed, the broadest knowledge of processing must be thoroughly understood. This means that the theoretical knowledge of unit and subunit functions must be focused upon the question, "What part must be aligned first, second, and third?"

10-23. This element is concerned with identification of sequencing alignments between interrelated functions and units, but not within the functional unit being aligned. Let's use figure 62 again. In order for A to be aligned, we see that it must have two inputs. Therefore, B in figure 62 must be aligned before A. Also, D and E must be aligned before A because either D or E provides the other requirement to A.

10-24. Therefore, B, D, and E must precede alignment of A, but since D and E can provide a separate input to A, either can be aligned without regard to sequence. On the other hand, B may have an input on either of the two input lines which may be from an aligned circuit.

10-25. Should this be the case, B's input must be proper. Therefore, the alignment of the circuit supplying the input must precede B's alignment. To recap the sequence:

- D or E can be aligned first.
- B can be aligned if its inputs are not coming from an aligned circuit. If either input does come from an aligned circuit, that circuit alignment must precede B's alignment.
- Finally, A circuits can be aligned.

10-26. This discussion has illustrated in a simplified manner our previous question, "What part must be aligned first, second, and third?" A detailed study of your equipment can show that interrelationships are dependent upon determining the data listed in figure 63.

10-27. *Independent/dependent.* You must, after identifying the interrelated functions and their associated circuitry, determine if the function is independent or dependent. if the function is independent, then it is a generator of some sort which is designed and manufactured to provide discrete outputs. Except for power requirements, it functions by itself. A unit of this type usually contains an oscillator. It may include frequency dividers, phase shifters, discriminators, quadrature networks, multipliers, and other assorted circuitry. These internal circuits only prepare the discrete output which is necessary for the objective alignment. Detailed information for your study of the objective alignment need not include all aspects of the independent related function, but must include enough to show what and when the generator outputs are, what generates them, and what circuits alter them.

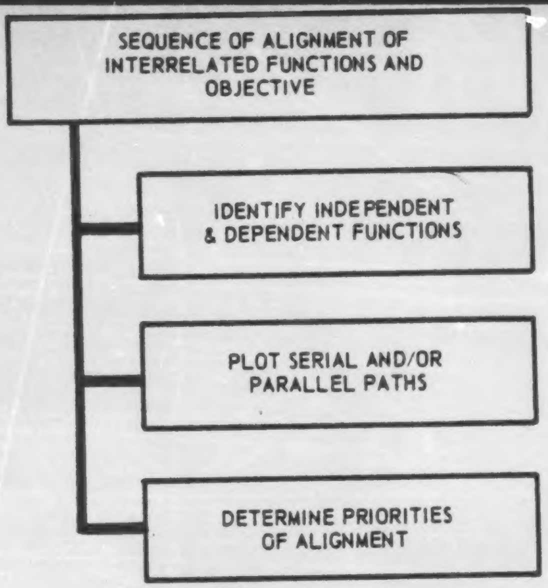

SEQUENCE OF ALIGNMENT OF INTERRELATED FUNCTIONS AND OBJECTIVE
IDENTIFY INDEPENDENT & DEPENDENT FUNCTIONS
PLOT SERIAL AND/OR PARALLEL PATHS
DETERMINE PRIORITIES OF ALIGNMENT

Figure 63. Sequence of alignment requirements.

10-28. If the interrelated function is dependent, you must identify its dependency. You must identify the major elements which cause it to be dependent. While doing this, determine whether or not the inputs to these elements are from other independent or dependent functions or circuits. If independent, your study (as in the case of the generator) can be concluded. If dependent, you must look further and identify all the relationships. This may require search for the origin of the signals. After all functions have been identified and listed, data relating to generation, distribution, and processing can be listed. It can then be related to the objective alignment as minor to the objective or major to the objective. This may sound like considerable effort, but experience has shown that dependency seldom exceeds three or four functions.

10-29. Serial/parallel. The next step in this phase of the analysis is determining whether the interrelationship is serial, parallel, or both. This means that you must find how the functional unit's output is relevant to the objective alignment, how it interacts, and when it occurs. You must identify simultaneous occurrences, time sequences, delayed sequences, automatic and manual control sequences, and off-line test/on-line test sequences.

10-30. Refer again to figure 62 (printed in the workbook). This simple diagram clearly shows that the sequence of actions is combined serial and parallel. Most frequently, the common elements to complexing the definition of sequencing are the timing and control units. The wide distribution of these signals necessitates careful study. These controlled signals play an extremely significant role. In the past, the circuits containing timing and control have been the ones first aligned. This trend must of necessity remain high on the list for starters. Other circuits using any inputs from the timing and control unit could not be aligned without proper receipt of timing pulses.

10-31. Priorities. Since interdependency is so significant even though the study may reveal that the relationship is minor, some consideration must be placed upon the last element in figure 63, *priorities*. Each complex waveform may play an interrelating role with others and, because it may, it causes priorities to be established. Most often, though, the priorities you encounter are prerequisites of the alignment to be performed. They may be such items as determining that specific DC voltage levels are or are not present. Priorities also have to do with identification and verification of major signal inputs, minor signal inputs, and voltage requirements. A final thought on priorities is that of the function being aligned. The function may provide multiple outputs at various times. It may be able to be used in different modes. It may have test parameters other than the normal operating parameters. If any of these conditions exist, the priority to function validation through alignment may cause the alignment routine to specify particular sequences, comparison of results with alternate sequences, or serial validation while sequencing.

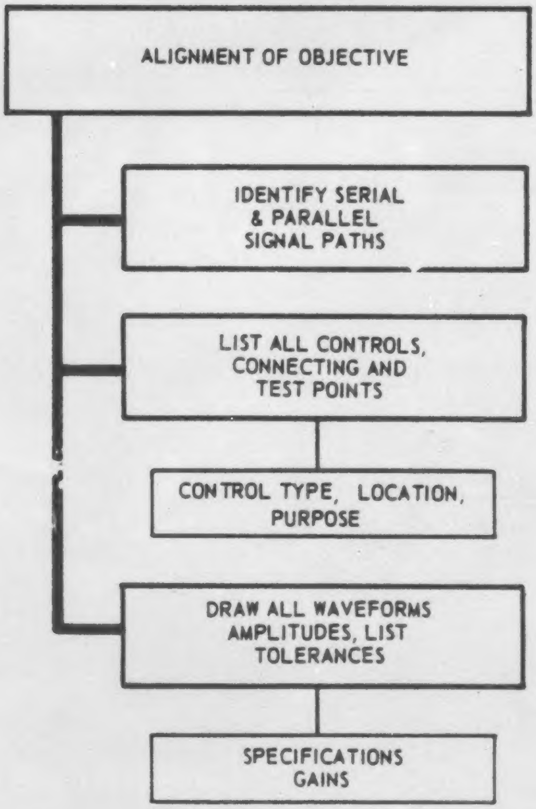

ALIGNMENT OF OBJECTIVE
IDENTIFY SERIAL & PARALLEL SIGNAL PATHS
LIST ALL CONTROLS, CONNECTING AND TEST POINTS
CONTROL TYPE, LOCATION, PURPOSE
DRAW ALL WAVEFORMS AMPLITUDES, LIST TOLERANCES
SPECIFICATIONS GAINS

Figure 64. Alignment of objective requirements.

10-32. Determining the sequence of units to be aligned is the fourth in a list of elements discussing the principles of alignment. To this point we have identified the objective, listed the subunits affected, identified any interrelationship which the function to be aligned has with other functions, and, finally, determined the sequence in which the units or functions must be aligned. Now we must determine within a function where to start the alignment, the points to measure, and the intermediate and final adjustment.

10-33. *Align the objective.* The fifth element within the study of alignments, indicated in figure 58 (printed in the workbook), develops the information necessary for the understanding of the function to be aligned. Figure 64 shows that there are three main subelements which must be included in order to develop a complete picture. These are (1) identify serial and parallel signal paths, (2) list controls, connections, and test points, and (3) draw waveforms, amplitudes, and list tolerances. The second element in this entire study identified the requirement to list all *subunits, circuits, and components of the objective.* This fifth element requires the use of the data accumulated in the second element plus additional data collected about the three subelements and their subordinates which are shown in figure 64.

10-34. Before studying each subelement, let's examine a point. The functional unit being aligned may have as few as one to three circuits or as many as 20 to 30. It becomes reasonable to assume that in a function containing one or two adjustments, a study reveals that if: (1) the controls are independent and parallel, either may be done first, or (2) the controls are interdependent and serial, then the one preceding the other must be adjusted first, or (3) the one control is dependent upon the other, then the independent control must be properly set before the dependent control can be set.

10-35. If the function contains numerous controls, an analysis of each of their purposes and functions is necessary. The study must reveal the same information as a function having one or two controls. It must also reveal sequences and priorities.

10-36. Serial/parallel paths. The block diagram being developed for the study of the function must be arranged in serial and parallel order as shown in figure 62 (printed in the workbook). Connecting lines should be used but should be held to a minimum to avoid confusion. Include only significant lines which provide major or minor control data to the circuit.

10-37. *Controls, connecting points, and test points.* List all controls by name, type, and symbol in the block on the drawing where they occur. This information is obtained from the alignment itself. Include alphanumerics of the controls and locations of the test points. Draw the symbol for the control. Standard symbols are shown in figure 65. Figure 65,A represents a control including a knob. Figure 65,B represents a screwdriver adjustment. Figure 65,C represents a potentiometer or rheostat control. Figure 65,D represents a variable capacitor, and figure 65,E represents a tunable coil. For filling in your block diagram, you may choose any of these symbols or combine them. Finally, figure 65,F shows a typical test point symbol.

10-38. Waveform specifications. Up to this point in your analysis, you should have an almost complete picture and understanding of the alignment. You have the:

(1) Objective.
(2) Subunits within the function identified.
(3) Interrelationships of other functional units noted.
(4) The sequence of adjustments to be made.
(5) Test points used for checking the accuracy of the individual adjustment and the intermediate functional steps.
(6) Final output test point.

10-39. From the technical orders you can obtain the final data needed for your study. This data is the exact waveforms, voltage levels, and current amplitudes. Place these waveforms as close to their point of occurrence as possible—i.e., input and output waveforms located at their respective test points. Record exact voltage amplitude and allowable deviation specifications. Identify, along with the alphanumeric code of each control, its purpose and limitations. For instance, if it is a pot, list its maximum and minimum gain in volts, current, etc. If it is a capacitor, list it as trimmer for over/undershoot, frequency compensation, or gain, and specify its maximum and minimum effect. Know or list in notes on the sheet where the adjustable component is located in a given circuit—i.e., input, output, base, emitter, collector, grid, cathode, plate, coupling, or filtering.

10-40. We have given you all the requirements for an understanding of what it takes to make an alignment meaningful. Of course, you realize that the actual performance of the alignment takes considerably less explanation than we have presented here. You might even be thinking, "I don't need to know all this information just to turn a pot and get a unit back into tolerance during an alignment." You don't if every pot you turn accomplishes (within the specified limits) its intended function. However, what are you going to do if that pot does not accomplish this function? You're the repairman. You're the man who will have to find out why that pot didn't perform its intended function. You're the man who will have to do the troubleshooting and correct the problem. Don't you think that your job of correcting the problem will be much easier if you are equipped with the knowledge of the functions and interactions of the circuits within that particular alignment?

10-41. Block Diagram Overview. To be sure that you have a complete picture, let's put the whole program together in block diagram form with proper sequence. Let's also identify each element of the study as a step. Figure 66 (printed in the workbook) illustrates the whole concept. Steps 1 through 5 illustrate each phase of the study and list for us the pertinent data needed for that phase of the study. As you can see, no phase can be omitted. In the final drawn study, certain phases may not be present because they do not have a bearing on the alignment. However, the phase must be checked to determine its nonexistence. Finally, step 5 must complete the picture which step 2 started, and steps 3 and 4 must include all information necessary for understanding.

10-42. In the next four sections, we discuss four general areas where alignments are most frequently performed. They are displays, electromechanical assemblies, memory units, and message processors. In each of these studies, except memory, there is an example study of an alignment as detailed in this section. Preceding the study is an explanation of the type of unit (display, etc.) on which the alignment is to be performed, and an identifi-

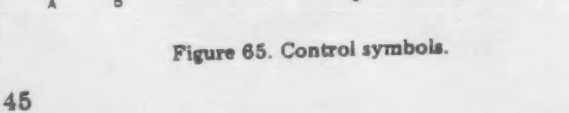


Figure 65. Control symbols.

cation of the limitation of the scope of the alignment. Your objective is to read and study each section carefully in order to:

- Gain understanding in areas related to your job requirements.
- Broaden your knowledge of related areas.
- Gain knowledge of new areas.
- Make comparisons and correlation to the equipment you work on.
- Identify with the concept of alignment in order to improve your worth to your unit through expertise.

11. Displays

11-1. Let's review what we covered in the previous chapter about displays. There are four logical functions in almost all display units. They are:

- Timing.
- Intensity.
- Vertical deflection.
- Horizontal deflection.

11-2. Associated with these areas are alignments, and we will see in our study that the identification and comprehension of interrelationships are extremely important elements. Alignments are performed in all the units.

11-3. **Timing.** Alignment of timing affects all units in the display; consequently, timing is usually aligned first. Some of the most significant subfunctions in the display functional areas using timing are:

- Sweep time generation.
- Sweep and symbol modes time sharing.
- Intensity unblanking and blanking.
- Data or video control.
- Expansion factoring.
- Special pulses for special display features being impressed on vertical, horizontal, or intensity units.

11-4. **Intensity.** The alignment of the intensity unit affects the control of the CRT display. This unit provides control for the cathode and control grids which affects emission in the CTR. Alignments are performed for:

- Intensity of the different types of displays—for example, normal and expanded mode.
- Unblanking and blanking of the CRT. The unblanking provides a display period, and the blanking provides a retrace period.
- Video selection or symbology processing of data which requires amplification, clamping, limiting, inversion, and shifting.
- High-voltage power supplies which provide the voltages for coupling, focus, astigmatism, aquadag, and acceleration.

11-5. **Deflection.** Display presentations most often use composite waveforms for generation of the display. Vertical and horizontal deflection units generally use the same sweep generators, have time-sharing symbol generating capability, and develop sweep signal inputs. For instance, range marks and radar data are often combined and processed simultaneously. Concurrently, through deflection, symbols may be presented on the scope screen. Alignment, therefore, requires at a minimum a clear understanding of where the displayed signals are coming from. However, an in-depth understanding of the alignments provides, in addition to a clear picture, a knowledge of each element of the display, its origin, and its use.

11-6. **Principles of Statistical Display.** The purpose of the development of statistical informational displays (SIDs) and digital informational displays (DIDs) is to provide visual, graphic presentations of digital information for command personnel to monitor and evaluate. Most often the display can be classified as being used for tactical control of airspace within the environment or for the use of the air defense of the environment.

11-7. The presentations include vector diagrams, numerical notations of weapons, and symbology designating weapons classification. Alphabetical and numerical listings are presented to identify headings, speed, armament, altitude, time to target or base, weather conditions, and other data pertinent to evaluation of the air environment. They also include geographical outlines of terrain, boundaries, and grids. Each element of the display requires circuitry for its generation and insertion into the display.

11-8. *Requirements for circuits.* Foremost in circuits required for display is the symbol generator. Since lines, curves, and dots are used extensively to create patterns on the display, symbol generators are built for these uses. One technique of activating these generators is to have a digital input cause an output. For example, a symbol is assigned to a particular type of aircraft. A generator is provided to create the symbol when the operator elects to use it. He initiates console action which creates a digital word. If the word has the 4 bits, 1101, in it, for example, a detection circuit as shown in figure 67 activates the generator. Examination of the detector gate in figure 67 shows that the 4-bit word must be 1101. The generator output is

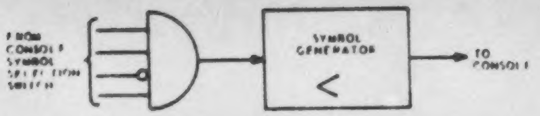


Figure 67. Generator with input decoder.

processed through the intensity channel (Z-axis) or deflective circuits for presentation on the CRT face.

11-9. Vector generators are another requirement for these types of displays. The generators usually require two locations for storage of the coordinates of the vector. Assume that a vector is to be drawn on the face of the CRT as shown in figure 68 (printed in the workbook). The vector is in the first quadrant; therefore, positive values of X and Y are used. The signs of the values are positive (0). The origin of all vectors is center scope. The LSD of each bit is 8 miles. Register contents must have binary values of 24 for start Y and 80 for stop Y, and 16 for start X and 24 for stop X. These values are added to the normal X and Y registers during sweep generation and deflection to cause intensification of the vector line. Vector lines can be drawn in any direction, but they have two limitations: (1) only a total number of lines can be drawn, based upon the number of storage locations allocated to memory, and (2) the length of each vector is restricted to the number of bits per register in storage and the bit value of the LSD.

11-10. Requirements for DIDs are similar to those of SIDs. Generators are activated by an operator through selection of switches. Characters and symbols are displayed on small CRTs. Various types of CRTs and circuits are used. One type is the charactron tube shown in figure 69 (printed in the workbook). The CRT incorporates two sets of deflection units: plates for character selection and coils for character positioning. Three-bit binary words are converted into deflection voltage for selection as shown in view A of figure 69. Compare the charactron tube with the typotron tube. The basic difference is the use of plates for character position instead of coils. This is shown in figure 70 (printed in the workbook). In each of these systems, the sweep positioning voltages allow for a horizontal and vertical positioning of characters and symbols to form words and statistical data and have a classification as DIDs. A newer device shown in figure 55 (printed as a foldout in the workbook), used as a DID, uses integrated circuits with programmed memories. Binary values are used to address the memory and select the characters. The unit uses a standard CRT, and the character is painted on the screen in a series of dots through the grid circuits. Deflection voltages are developed from binary counts converted to analog voltages. The vertical position counter is advanced each time that the horizontal counter resets. The generated voltages from the digital-to-analog (D/A) converters position the character on the screen of the CRT. A review of the requirements for circuits on these types of displays leads to:

a. Type of CRT.
b. Types of circuits used for generation of deflection voltages.
c. Circuits for conversion of digital to analog circuits.
d. Symbol generators.
e. Input selection and decoding circuits.
f. Vector generators.
g. Vector coordinate registers.
h. Panels containing controls (pots, coils, capacitors) for aligning the systems.

11-11. *Types of display programming.* We have mentioned some of the types of programming SIDs and DIDs in the preceding discussion. Now let us study them in greater detail.

11-12. Time sharing. Time sharing is one of the most extensively used methods for display programming. Figure 71 (printed in the workbook) shows clearly that only when the CRT is unblanked by timing control 1 does the intensification of the signal cause a character formation. In the formation of letter A, times 1 through 5 are painted; then the CRT is blanked for one time period while the symbol generators are idle. The CRT unblanks again for times 6 through 10 and completes the second line for letter A. Blanking is used again, and the vertical amplifier output reverses its polarity to prepare for the painting of the horizontal bar. At the same time, the horizontal amplifier output also reverses its polarity to allow for a sweep from right to left during time periods 12 through 14. At the end of time period 14, the CRT is blanked and stays blanked until the next character intensification period.

11-13. Matrices. In two of the DIDs mentioned above, each had a stencil plate (called matrix), and the flow of electrons through the character stamped in the plate created the shape of the character on the CRT screen. In the third DID examined, an integrated memory unit was used with each character as a permanent data entry. Addressing of a memory location allowed D/A conversion of the character storage to take place and a display on the CRT screen to occur through the grids of the CRT.

11-14. *Programmed.* Many displays contain forced display data. This is data which is usually hard wired and available all the time. The display may contain information by which analysis can show and verify the operation of the:

- Generators.
- Circuit processing symbols and characters.
- CRT circuits.

The programmed data may also be *hand* wired (by patch panel) to provide a display. For example, we have:

- Grid or polar coordinates.
- Site relationship.
- Maps of states, countries, etc.
- Maps of densely populated areas.
- Elevation maps, contour maps, etc.
- Maps of airfields.
- Satellite positional data.

The hand wiring allows for easy change when conditions warrant. It also allows for individual site configuration, thereby adding versatility to equipment and increasing its capability.

11-15. Callup methods. Numerous methods are used to perform programming of the display (often called calling-up data for display). The most usual methods employ:

- Switches.
- Tag symbol.
- Omniball or wheels attached to analog-to-digital converters.
- Light guns.
- Keyboard to memory program.

Each of the items listed above provides an input of correlation which the processor can compare and react to. The input may be directly sensed as binary or may be transmitted by gray code. It may be an analog input or photoelectric input through sensors.

11-16. **Principles of Radar Displays.** Radar displays are those that are usually associated with displaying radar returns. The two types of displays usually developed are the *search* display and the *height-finder* display. The purpose of the search radar display is to present all flying targets in positions on a CRT relative to the site location. We discussed this type of radar in Chapter 1 of this volume. We also discussed radar antenna rotation and beacon returns. Each of these elements is necessary for video display for air surveillance. Each flying object's position is assigned an azimuth heading relative to the site's position. It is also identified as to *type* of aircraft, by *beacon* code, by aircraft *flight plans*, or by scheduled airline *routing*. The purpose of height-finder displays is to determine the altitude of aircraft within the range of the radar. To accomplish this, the operator or computer controls the azimuth position and the height nod. Most height-finder radars also have a capability of locating an aircraft through a jamming situation. This operation is called *search lighting*.

11-17. *Requirements for circuits.* In addition to the basic complement of circuits that are normally used in displays, both types display certain characteristics of their radar. Search radar displays, as shown in figure 72, have sweep and intensity coincident with the azimuth position of the radar. Height displays, also shown in figure 72, have sweep coincident with the nod angle of the antenna. Since each display uses the position of the radar in its display, the voltage received from radar servos is processed by the display equipment and used for sweep or nod voltage in the display. In search displays, quite often the sweep generator is an integral part of the converter/processor unit. It is a free-running generator and provides continuously changing sweep voltages for all search display consoles in the site. The principal use is quite simple. As the generator operates, detection circuits cause two independent outputs—one for vertical and one for horizontal. A sawtooth of varying amplitude and inverse capability is generated for each deflection. When algebrai-

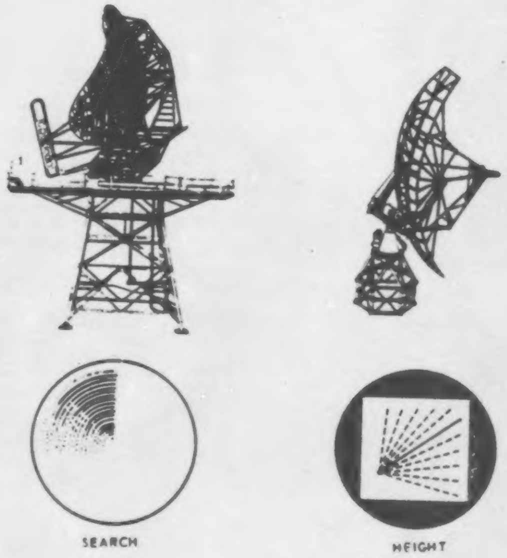


Figure 72. Radar CRT displays.

cally combined in deflection circuits, the intensity is shown as the instantaneous value of each. Figure 73 (printed in the workbook) shows how this operation can be performed. With two positive-going sweep ramps, the displayed sweep is shown between north and east. The magnitude of the horizontal sweep is minimum at 0° and maximum at 90°, and the magnitude of the vertical sweep is opposite (fig. 73, A). This shows that at any instant in time the combined values of sweep voltages provide a deflection between 0° and 90°. In figure 73,B, horizontal sweep voltage decreases, and vertical sweep voltage reverses polarity and increases in magnitude from minimum to maximum. In figure 73,C and D, the two other requirements for a full 360° sweep are established.

11-18. The antenna rotates, and the sweep on the display shows rotation. The two must be synchronized. A method frequently used for synchronization is called error sensing correction. A differential principle is incorporated whereby a feedback signal from the antenna servo is matched against the generator signal that is produced in the display equipment. If no difference is detected, the circuit is said to be null. If the antenna error voltage is greater or less than the generator output, a *difference* voltage is generated by the differential circuit. This difference, called *error* or *correction* voltage, is fed to the generator to bring the sweep generators into synchronization by speeding up or slowing down the operation.

11-19. In height-finder displays, two sets of generators (servos) are often used. One is for nod generation and the other for azimuth change. These generators function along with height-finder radars. Feedback voltages from antenna servos are used like search feedback voltages for control of internal generators. A significant difference in the operation of this display is that the sweep in azimuth is only done on command, while search is continuous. In addition, the nod origin is usually located in the lower left corner of the display. Nod voltages are shown in figure 74 (printed in the workbook). If the antenna is stopped at 0° elevation, the horizontal deflection voltage shown in figure 74,A, is maximum and the vertical deflection voltage is minimum. A nodding antenna contains all angles of nod between 0° and 30°, as shown in figure 74,B. The horizontal sweep voltage decreases with increases in elevation, and the vertical sweep voltages increase from null with increases in antenna nod. The relative magnitude of horizontal and vertical sweep voltages for 0° to -2° nod is shown in figure 74,C.

11-20. In addition to the requirements for sweep generators, servos, and differential circuits, another requirement is range mark circuits. The circuits must provide a signal for each 10 miles of range. Each radar mile is 12.36 microseconds. Therefore, each 123.6 microseconds the circuits must produce an output. The pulse width of the 50-, 100-, 150-, and 200-mile range marks must be stretched by blocking oscillator, delay line, or monostable flip-flop to allow a longer time for intensity. Finally, video processing circuits, such as quantizers and video amplifiers, are used to process radar returns and make these returns acceptable for display equipment.

11-21. *Types of display programming.* Programming in these types of displays includes programming of:

- Numerous kinds of search radar video.
- Beacon video.
- Height-finder video.
- Limited displays through control functions.
- Range marks.
- Angle marks.
- Video mapping.
- Antijamming control functions.
- Target identification.

11-22. Data selection. Each of the videos used by these display systems incorporates some specific limitation of the original video received by the radar set. For example, clouds are usually eliminated from the display by use of moving target indicator circuits. Jamming is reduced by anticlutter circuitry. Echoes are reduced by use of main lobe indicator circuits with suppression of side lobes. Digitizing video returns allows for uniform intensity of all tracks regardless of the original track intensity signal being received. Further limitation of display data is accomplished by circuits which limit the display to:

- Specific height groups; i.e., 40-60 K ft. or 20-40 K ft.
- Initial tracks.
- Old tracks.
- Tracks with ID.
- Tracks with beacon.
- Hostiles.
- Weapons.

Almost all of the circuits, either generating the displays or limiting the displays, are controlled by switch actions at the console. Each switch is wired to the program through circuits in the processor. It either arms or disarms the processing circuits which detect the data under its control. These switches seldom inhibit the accumulation of data.

11-23. Time sharing. Time sharing is an essential method used with these types of displays. It has the same weight as it did with statistical displays.

11-24. Programmed. Video mapping is usually performed through a program of a video mapper. The display is fed, along with other data and range marks, into the CRT and displayed. Video mapping usually provides a map of geographical boundaries; however, it is not limited to geographical maps. Coordinates, data content, and other data are programmed.

11-25. Callup methods. As we have mentioned, switches are the primary callup method. In addition to switches, light guns and omniballs are used as callup methods.

11-26. **Typical Alignment Requirements for Sweep Circuits.** Generally, the sweep alignments fall into two broad categories. One is the sweep generator and the other is the centering. The sweep generator alignment is performed to bring sweep voltage amplitudes to specification. It may also prescribe specifications for pulse duration, slope angle, and proper phasing. Alignments will usually require isolation of basic sweep generators during a phase of the alignment. Prerequisites usually require verification of timing waveforms because an improper pulse width affects the duty cycle of the sweep generator. After alignment of the sweep generator, alignment of the combining or controlling circuits usually follows. Frequently, capacitors (trimmers) are used in the controlling circuits to compensate for variables in the operation of these circuits. This allows for a proper overall display.

11-27. The centering alignments usually require the use of meters and isolation of the sweep driver circuits. Voltages, sometimes DC and sometimes AC, are read simultaneously while individual adjustments are performed. When both meters read the same voltages within tolerable allowances, centering is complete. It may be necessary to consider the front panel horizontal and vertical positions of these controls. If they are included while centering is performed, their positions must be at the 50-percent point within the control. This allows for operator positioning of the sweep in all possible directions equally. In addition to sweep and centering alignments, intensity and high-voltage alignments are performed.

11-28. **Typical Alignment of Intensity/Unblanking and High Voltage.** Intensity and unblanking circuits contain pots and trimmers. The pots usually control amplitudes of different gate outputs which cause more or less intensification on the CRT. Each gate amplitude ultimately results in bias control for succeeding circuits and the CRT. Video and data are usually imposed on top of the intensity gate. Therefore, the gate amplitude must be high enough for proper intensification, but low enough for the video data to cause a further intensification of this display.

11-29. Trimmer capacitors, used in aligning these circuits, provide two functions. First, they allow for squaring of gate waveforms, and second, they allow for amplitude control of high-frequency (short pulse width) data and video pulses. Generally, considerable variations in amplitude are possible when using these trimmers.

11-30. Specifications must be followed, especially when aligning gate amplitudes. Assume that the maximum signal into a high-voltage coupler is 15V and the CRT turn-on voltage is 7V. If an adjustment within the alignment were performed and the gate level were incorrectly set at 12V, the conduction of electron flow within the CRT would be almost maximum (extremely-high intensity). Add data or video to the top of the gate (amplitude 5V) and clipping within the high-voltage coupler (HVC) occurs.

11-31. The video or data displayed would be hard to see because of the clipping action. However, with proper alignment, a 5V gate and a 5V data or video pulse can pass through the HVC to the CRT without clipping and cause a display with a good contrast (signal-to-noise) ratio.

11-32. Focus and other high-voltage controls mainly consist of pots (refer to Chapter 2 of this volume). These may, however, be alignment controls on circuits using the high voltage which compensate for ripple. Some of these circuits are the high-voltage coupler and focus compensation circuits which correct the focus at the extreme edges of the CRT.

11-33. To recap, alignment of intensity/unblanking and high voltage includes the following:

- Pulse-width (duty cycle) control.
- Pulse shaping (squaring) control.
- Amplitude (gate, levels, and data) controls.
- Focus controls.
- High-voltage controls.

11-34. **Perform a Display Character Position Alignment Study.**

Title: *Character Position Adjustment.* Objective: *Align deflection units to provide characters of the proper size and placement.* The objective of this alignment is clear. Both

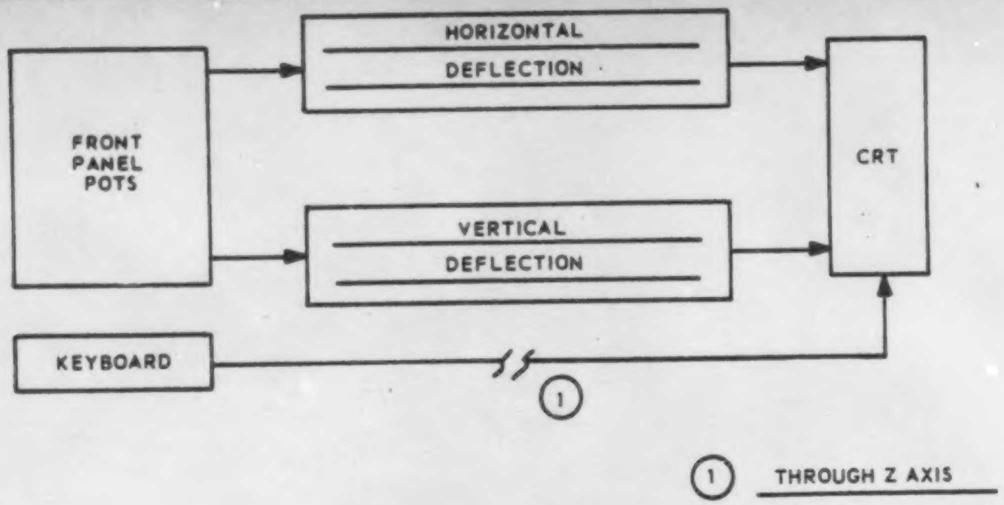


Figure 75. Alignment units with external elements.

horizontal and vertical deflection units are affected. Since these units are parallel as previously defined, an interaction (interrelationship) exists. The interrelationship is *not* between units but *within* the CRT. Each unit is self-contained and has no interconnection with the other unit. However, a simultaneous combining of the two outputs is required within the CRT in order to produce a complete display (all other functions being present). If either one is missing, a lack of height or width (a straight line) results.

11-35. *Elements.* Viewing figure 75, we see that a parallel exists. We also see that front panel controls are connected to the units. The CRT uses the output of each unit, and an input character generator (keyboard) provides data through the Z-axis (intensity) to the CRT grids. In this alignment, selected characters provide the visual element needed for adjustment of the deflection units. Also, note that the front panel control for height alters the circuit operation of the horizontal deflection unit. The same is true for vertical.

11-36. *Prerequisites and interrelationships.* From the study of operation and elements, we see that interrelationships exist and prerequisites are formed. In the order of their general priority, the prerequisites are:

(1) Power adjustments.
(2) Raster adjustments (front panel intensity).
(3) Front panel lights and vertical position adjustments.
(4) Character intensity.

11-37. Character intensity consists of:

- Z-axis adjustments.
- Beam current adjustments.
- Focus adjustments.
- Character input from the keyboard.

11-38. Verification of these prerequisites is required before the deflection alignment is performed.

11-39. Let's move along to figure 76 (printed in the workbook). In this figure, the interrelated units are identified. They are:

- Intensity circuitry.
- Beam current circuitry.
- High-voltage circuitry.
- Front panel control circuitry
- Keyboard circuitry.

11-40. Notice that in each unit except the keyboard (which is not an integral part of the display), variable controls are included. They are:

- An intensity control.
- A beam current control.
- A raster and focus control.
- Power setting controls.
- Front panel controls.

Carefully note that focus and beam current have interaction. Therefore, one control affects the other circuitry.

11-41. *Align the deflection units.* Moving into the final phase of our study, refer to figure 77 (printed in the workbook). Included are the three controls on the horizontal deflection unit and the three on the vertical unit. Looking closely at the *zero reference* (vertical) pot and *vert gain* pot, we see that these two controls interact. We also see that the *vert amplitude* pot interacts with the *vert pos* (front panel) control. The same interactions of controls exist in the horizontal deflection unit.

11-42. This arrangement of controls requires a delicate touch while adjustments are made. Proper sequence of positioning these controls results in an accurate alignment.

11-43. The technical order which listed the information for this study established the sequence, not in precise instruction but in its format. Finally, the *character position adjustment* routine was followed by a series of routines which refined other elements of the display unit.

12. Electromechanical Devices

12-1. For the discussion of alignment on electromechanical devices, only two examples are provided. These are aligning a servo unit and aligning part of a printer. The principles of understanding an alignment in this area are unique in that, in addition to normal electronics, some mechanical changes occur. Electronic pulses (voltages or currents) are converted into mechanical actions or work, or mechanical actions are converted into electronic data (voltage or current). One sample examines the alignment of a servo unit which converts two positional data messages into a vector voltage magnitude. The vector voltage causes actions further on in two forms: (1) the electronic displacement of sweep voltages to a display unit, and (2) the conversion to mechanical readout unit through a chopper unit. The other example presents a representative selection of an alignment of a mechanical element in a printer. This alignment is restricted to one small segment for presentation of the concepts which were outlined in the first section of this chapter. Research showed that electronic control is provided for the mechanical actions, so it becomes part of the analysis. Keyboards, card readers, punches, tape units, and printers fall into a classification with electromechanical devices. Therefore, the discussion on the printer alignment can also provide an example for analysis of alignments on these other devices. The interaction of mechanical and electrical assemblies is closely related in all units. When you do research on your equipment, apply the principles shown here on the printer to those electromechanical units in your equipment.

12-2. **Requirements.** Selected requirements for understanding alignments on electromechanical devices relate to:

- Understanding the processing of the immediate circuit or mechanical element.
- Identification of specifications and tolerance.
- Proper selection of circumstances to activate and control the element under alignment.
- Visual recognition of mechanical assemblies from illustrations.

12-3. **Perform Servo Unit Alignment Study.** Title: *Align the Range Servo Unit.* Objective: *The purpose of this alignment is to measure and adjust individual controls to specifications to allow for generation of voltages through coupling by mechanical means for positioning the displays on a console.* This information provides an answer to step 1 of the procedure which was detailed in the beginning of this chapter. The purpose clearly states that all adjustments must be aligned to specifications in order to provide an overall alignment of the servo unit. It also indicates that mechanical coupling is involved in the servo unit. This shows that feedback positioning, although measured in voltage form, is performed by mechanical means. The title indicates that range data (X and Y) are involved. Therefore, feedback voltages from resolvers are to be included in the analysis.

12-4. Before going into step 2, we shall review servo units—their purpose and operation. Figure 78 (printed in the workbook) shows a simplified block diagram of a servo unit. It shows an input unit, an amplifier chain, a servomotor unit, a feedback pickoff device (which can be electrically or mechanically linked), a nulling device or point, a rate feedback, and a power source. In the example in this text, the feedback is primarily electrical through mechanical coupling from the drive motor.

12-5. *Nulling.* Servoloops operate on the principle of positioning a feedback pickoff device so that the feedback voltage can be summed with the input signal to produce a null. The difference between the input and feedback signals is fed through a chain of amplifiers to the "signal windings" of a 2-phase 400-hertz motor. The motor also contains a "reference winding" which is connected to a constant power source. For motor operation, both sets of windings must receive power, and the direction of rotation is a function of the phase relationships between the two sets of windings. Typical feedback pickoff devices are potentiometers, synchros, and resolvers. When the motor is correctly positioned, the feedback will null the input signal leaving no further drive power to the motor signal windings. The drive motor will stop at the desired point.

12-6. *Rate feedback*. A refinement is present in the form of a negative rate feedback—one whose amplitude is a function of motor rate of rotation. Without this feedback, the motor would have a tendency to "coast" beyond the actual null point and would receive an acceleration in the reverse direction. This could, in turn, cause an overshoot in the reverse direction followed by another reversal, etc., which would set up a continuing oscillation. The rate feedback tends to reduce drive power as the motor picks up speed, but gives virtually no opposition at very low speeds, such as in the immediate vicinity of the null. Therefore, it helps to eliminate oscillation or hunting without destroying null accuracy.

12-7. *Direction of rotation*. In the 2-phase AC motor, the direction of rotation is a function of the phase relationship between the signal and reference windings. A reversal of current direction (phase) in either, but not both, will reverse motor direction.

12-8. When the input signal changes (which should drive the servo to a new position), the difference between input and feedback signals will result in a signal either in phase or 180° out of phase with the reference signal; this will determine the direction of rotation.

12-9. It should be noted that a reversal of connections on either, but not both, sets of motor windings will reverse the current direction and, consequently, the motor direction. If these phase relationships are incorrect, the servo will drive away from the null position instead of toward it.

12-10. Using this information and the figure, we see that a voltage input signal into the resolver provides a signal to the amplifier chain. The phase and amplitude of the signal cause the servomotor to rotate. The feedback is coupled to the null point. A difference value to the amplifier chain causes the motor to rotate in a direction which reduces the voltage into the amplifier chain. This action continues until the signal into the amplifier chain is reduced to null.

12-11. Step 2 requires the identification of the subelements, circuits, and components of the unit to be aligned. Figure 79 (printed in the workbook) illustrates these elements. In the sequence of their respective placing, they are, left to right, as follows:

(1) The *input transformer* which provides a method for coupling any difference between the input signal and feedback signal into the secondary of the transformer. If no signal is coupled, it may be assumed that the feedback voltage equals the input voltage.

(2) The *amplifier chain* which converts the single voltage input into push-pull outputs by inverting the input to one leg of the output. Two gain pots are used, one for each line. Noninverting amplifiers provide amplification of the signal to motor windings.

(3) The *drive motor* which reacts to the amplifier inputs based upon the amplitude of the signal; one signal wire is in phase and the other is 180° out of phase with the reference winding. The motor rotates, and its shaft rotates the wiper arms on three pots.

(4) The *three pots*. *Er* is an AC pot which provides a feedback voltage for servonull and provides an AC range voltage to the console through the line driver board. *Vr* is a DC pot which is mechanically linked to the motor shaft and provides a DC range voltage through an amplifier board. The *AZ gain* pot provides a rate control to the azimuth servoloop by regulating the rate of change, depending upon range of target data.

(5) *Reference voltages* which are provided for the motor and for pickoff voltages for the pots.

(6) The *GAMI* and *LDRI boards* which provide adjustable outputs to other functions.

12-12. Before proceedings with step 3, let's review the extent of the work involved:

- All controls are pots; therefore, they are measurable on meters as AC or DC and on oscilloscopes.
- Two gain amplifier controls are included in the amplifier chain.
- Each output circuit has a gain control.
- A level control is also included in both output circuits.
- Potentiometer controls on the assembly are mechanically positioned by the shaft of the motor.

12-13. Step 3 instructs us to identify the interrelationship of other functions to the basic function. Therefore, we must establish where the data inputs are coming from and how they are derived.

12-14. Range voltage, as an input to the servo, is a product of digital-to-analog conversion. It is composed of two distinct and separate sources which are electronically combined in a servo unit. This brings these points into the analysis:

- Generation of X and Y data.
- Range data (X and Y coordinates).
- Digital-to-analog conversion.
- Resolver action to combine the coordinates into one range value.

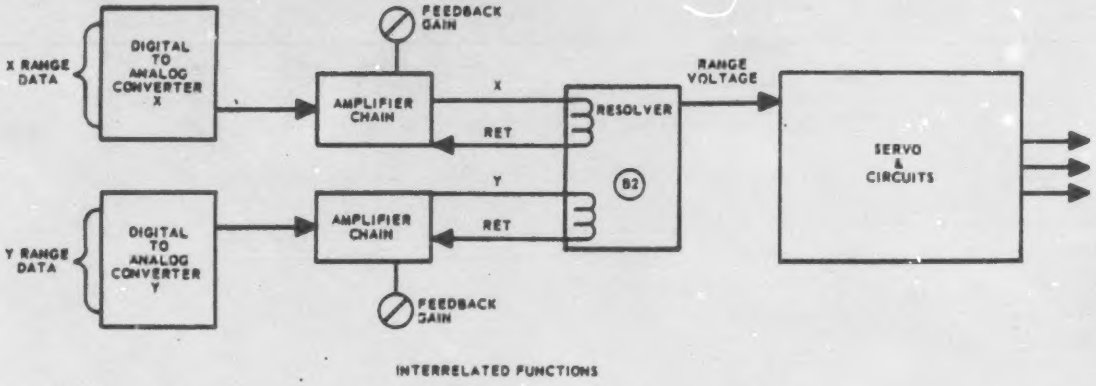


Figure 80. Interrelated functions and servo unit.

12-15. Taking the reverse method of identifying the interrelated functions shows that the resolver feeds the range voltage to the servo unit (refer to fig. 80). The resolver has two inputs: an X coordinate range voltage and a Y coordinate range voltage. These voltages (AC) are developed from the amplifier chain and digital-to-analog converter circuits from X and Y digital range data.

12-16. A review of the text on this circuitry gives us the following specifications about the interrelated functions:

(1) X and Y data can be programmed by selecting the off-line test mode of operation, and a range coordinate of 64 miles is equal to the reference voltage of 5VAC.

(2) The feedback pot of the amplifier chain is 10K ohms in series with 100K ohms and is thereby limited to 10 percent. Further, since the signal is in AC in the range of 5VAC, a 10 percent or less change is not measurable on an oscilloscope; an RMS (AC meter) is required.

12-17. From these items, we can see that a definite interrelationship of functions exists. The following prerequisites are given which now have meaning:

(1) The alignment is performed in off-line test mode.

(2) Selected switch settings are used to provide X and Y range data to the D/A converters.

(3) Gain ratios of related functional amplifier chains are to be in unity.

(4) Resolver B2 (part of the azimuth servo) must be properly oriented.

12-18. These four prerequisites definitely establish a sequence of operations which must be properly verified before alignment of the servo unit. At this point, we are substituting the complete pictorial of the servo and interrelated functions in figure 81 (printed as a foldout in the workbook). We do this now so that you can grasp the full significance of this discussion.

12-19. Step 4 requires that a sequence of alignment be established with reference to interrelated functions. Refer to figure 81, and locate the test chart between the D/A converters. This chart shows test 4 with 64 miles in an X coordinate and test 5 with 64 miles in a Y coordinate.

12-20. The next phase is that of determining the sequence of functions of interrelated units. Obviously, the D/A converter and amplifier chain preceding the servo unit must be aligned properly in order to align the servo accurately. Since there are two paths, one for X and one for Y, we have a parallel situation. Either one may be aligned first. Verification of range data in binary form as inputs to the D/A converter is a prerequisite. Verification of the 5-VAC reference voltage is a prerequisite. Operation of the azimuth servo unit (since resolver B2 is a part of this unit) is a prerequisite.

12-21. *Prerequisite verification.* Step 1: verify digital data. Step 2: verify unity gain from amplifier chain for both X and Y measured at AZA4XA7-6 and XA8-6 of driver boards respectively. Step 3: verify that output from R3 measured A2A2XA8-4 is equal to output from amplifier chain. This completes the verification of interrelated functions. One factor not identified, but significant, is that for verification of R3 output to equal 64 miles, either disabling of X while measuring Y or disabling of Y while measuring X is paramount. A combination of X and Y results in a coordinate range other than 90° or 180°.

12-22. *Align the servo unit.* The fifth step requires the alignment of the servo unit. Two points are examined: first, a new unit is to be installed and aligned. and, second, an existing unit is aligned.

a. Before installation positioning of the pots *Er, Vr,* and AZ gain, adjustments must be made. Using an ohmmeter, set all three pots for very close to a short: for *Er,* pins 2 and 3; for *Vr,* pins 7 and 8; and for AZ gain, pins 9 and 10. After installation and power check, alignment is performed on zero amplifier boards A2A5XA7 and XA3, which are shown on the right-lower portion of the drawing.

b. The remainder of the alignment is the same for either a new installation or realignment of an existing unit. Use a pure 64-mile either X or Y into the servo. *Er* must measure 5VAC. With proper operation of the null point transformer, measured voltages at both test points in the servoamplifier chain are set. The output of the line driver board processing *Er* signal is set to a gain of unity. Finally, the GAMI board gain is set to the value of 17.24VDC with the entire test problem 4 inserted (X and Y, reference chart). The alignment is complete. All internal subunits operate properly. All interrelated functions have been identified and verified or aligned. A complete picture of the unit is presented, and an understanding of its operation, purpose, and function is clear.

12-23. **Perform Keyboard-Printer-Punch Space Alignment Study.** Title: *Space Magnet, Space Pawl Stop Plate, and Space Pawl Clearance.* Objective: *The purpose of this alignment is threefold. The first requirement is to adjust the clearance between the space pawl and carriage rack teeth when the armature is energized. The second requirement is to position the space magnet and armature when the armature is energized. The third requirement is to adjust the clearance between the stop plate and the space pawl when the armature is energized.* This alignment may be completely foreign to many computer technicians because it involves mechanical alignment; therefore, we provide this brief review of the printer. In the operation of this impact printer, two characters are activated within a specific time interval (print cycle). The characters are printed on the paper by hammers. After printing the characters, the carriage is moved to the left, and the operation is repeated. A space between words is treated by the machine as a character. A rather complex mechanical assembly (fig. 82), controlled electronically, is incorporated into the printer. The logic package provides decoding which releases a pawl for spacing and allows a spring to pull the carriage to the next position. It is in this carriage that the alignment must be performed.

12-24. *Spacing theory.* An explanation of the spacing theory follows:

a. The spacing mechanism (fig. 83, printed in the workbook) consists of a magnet (coil), armature, bail, rack, pawl, and carriage feed spring. The carriage feed spring exerts a constant pull to the right on the carriage. The carriage is kept from moving by the engage-

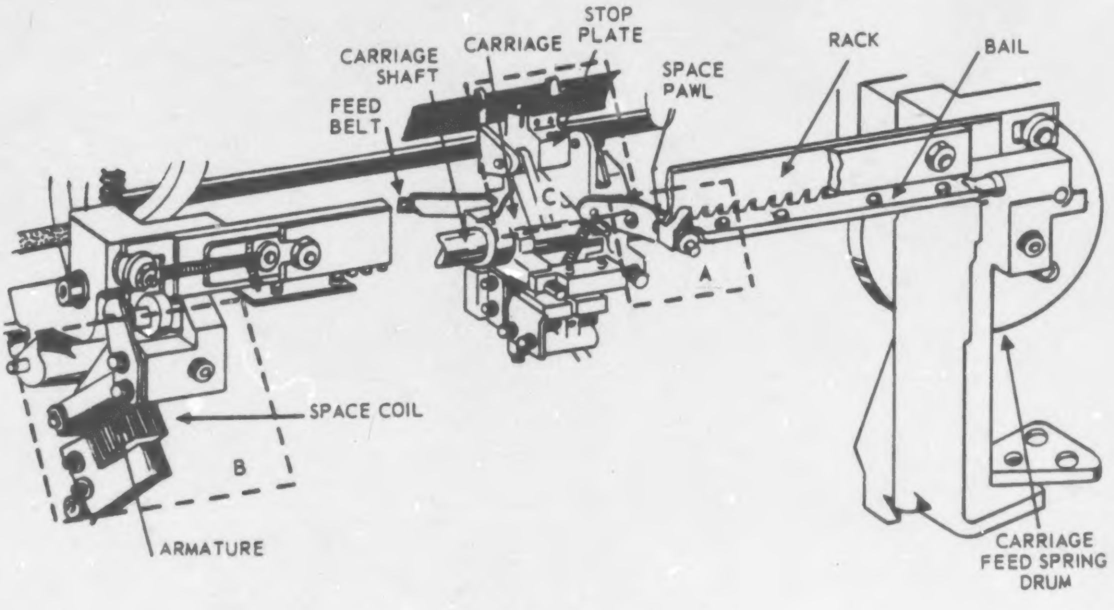


Figure 82. Mechanical printer carriage.

ment of the pawl in the rack. The pawl is mounted on the carriage in a way that allows it to engage the spacing rack. When the circuit emits a space impulse, the magnet energizes and causes the armature to move down. As it does, the bail rotates counterclockwise when viewed from the left side. The bail contacts the bottom of the spacing pawl, causing the pawl to move down and out of engagement with the rack.

b. The magnet is held energized for approximately 4-6 milliseconds. This is just enough time to get the pawl out of engagement and allow the carriage feed spring to pull the carriage a short distance to the right. When the magnet deenergizes, the mechanism is reset by the bail spring and the pawl spring.

c. The rack is spring-loaded to the left. When the pawl leaves engagement with it, the rack spring causes it to move toward the left. As the pawl reengages, the rack will move slightly. This slight movement is enough to absorb the energy which the carriage has built up. The rack stops against a small rubber bushing which cushions the bounce.

12-25. *Two methods of spacing.* Two methods result in providing ground to the space coil and thereby activating the space mechanism. These are shown in figure 84 (printed as a foldout in the workbook). The first method is that of depressing the *spacebar* on the keyboard. This action results in bail latches closing and generating a binary code of 0000010. This code is detected in printer logic in the *function detection*, and is sent through the *function register* to the manual input of the *space circuit*. The second method is the automatic sensing of the end-of-print cycle. Since time is allocated for printing two characters before spacing, the print cycle ends with detection of both hammers fired. This action sets the automatic detection gates in the space circuitry and provides a ground to the coil.

12-26. *Align the printer space elements.* The second element of figure 66 (printed in the workbook) requires identification of subunits of the function to be aligned. To do this, refer again to figure 82. This figure is a view of the carriage assembly and shows each of the elements of the space mechanism. To repeat them and identify each as shown, they are:

(1) Magnet (labeled space coil), lower left.
(2) Armature, lower left.
(3) Bail, upper right.
(4) Rack, upper right.
(5) Pawl, upper center.
(6) Carriage feed spring, lower right.
(7) Stop plate, upper center.

12-27. The three objectives of this alignment are shown in the blocked-in areas. *A* is for space pawl and carriage clearance, blocked-in area *B* is for the space magnet and armature, and area *C* is for the space pawl and stop plate. Each of the blocked areas is expanded for discussion in figure 83 (printed in the workbook). When studying this figure, combine the use of figure 82 and those in blocked areas A, B, and C. Specific tolerances of individual adjustments are not included now but are listed in the final element.

12-28. Step 3 (fig. 66, printed in the workbook) requires identification of interrelationship with other functions, and figure 84 (printed in the workbook) shows these. The mechanical assemblies and electronic assemblies are shown in block-diagram form: the mechanical in dash-enclosed blocks and the electronic in solid-line enclosed blocks.

12-29. The interrelationship serial and parallel sequence as required by step 4 is as follows. Refer to figure 84. Before the alignment of space pawl clearance, space magnet and space pawl/stop plate adjustments, the space pawl rack clearance is accomplished. Before this alignment, space bail is positioned. Before these two alignments, space armature and shaft end play adjustments are made. This shows you that four elements are prerequisite to the alignment in this analysis in the mechanical area.

12-30. In each case of this alignment, the coil must be energized. Therefore, an electrical path is obtained through ground to energize the coil. Already identified are the two paths for obtaining ground—manual and automatic. Note in figure 84 that R4 of the space circuit is a control in the single-shot circuitry, and it provides a variable pulse width. Consideration must be given to this circuit output when operation of the printer spacing is performed. Too short a time interval may provide insufficient time for proper operation and may mislead a technician into adjusting space clearance. The opposite is also possible if too long a time could cause a skip or double space and again lead the technician astray. Farther back in the circuitry, the hammer control circuits also have pulse-width controls. Improper adjustment of these may influence the spacing and cause improper selection of space timing. Finally, although this subject of troubleshooting is not included, a processing or decoding failure could lead the technician into realignment of these units when misalignment is actually not the cause.

12-31. For the final element, figure 83 (printed in the workbook) provides an exploded view of areas A, B, and C, as noted above. In each case, specifications of tolerances are included for visual acknowledgment. The routine requires:

a. Verification of input data, completion of prerequisite spacing alignments, and power.

b. Alignment instructions which identify each screw to be turned, loosened, and tightened, and the final securing of screws.

12-32. Completion of the task is relatively simple. Verification of mechanical prerequisites requires use of one of the systems outlined in the first part of this section. Verification of correct pulse width of the ground enable pulse is measurable on an oscilloscope. Complete understanding, verification of prerequisites, validation of entries, and accurate alignment of the steps listed in the routine insure operational capability.

13. Memory Units

13-1. The coverage of memory devices presented in the chapter on adjustments defines in detail the many types of these devices currently in use. The different adjustments were discussed. Alignments of memory units require, in many cases, a repetition of the adjustment tasks. For example: *Adjust a drum read/write head.* Normally, one set of instructions establishes the procedure, and each head is adjusted the same way with the same instructions. Completing adjustment of all the heads constitutes a complete alignment. The same situation exists for read/write amplifiers, tape heads, disk heads, and other memory devices. Consequently, this section does not present an example alignment. It does present some significant data about the types of memories, principles, classification, and a comparison of the read/write cycles most frequently used.

13-2. **Types of Memory Units.** At present, there are approximately 11 different types of memory devices. Each one is capable of providing data to a machine in language that the machine understands. However, not all of them can accept data from the machine for storage. In the interest of clarity, we list the types according to two classes: (1) those that can receive, store, and provide data, and (2) those that can provide data only.

Class 1 Receive, Store, and Provide	*Class 2* Provide Data Only (read only)
a. Cores	*a.* Storage tube
b. Drums	*b.* Integrated (program memory) circuit (IC)
c. Disk	*c.* Capacitor read only storage (CROS)
d. Delay line	*d.* Transformer read only storage (TROS)
e. Thin film	*e.* Programs
f. Tape	

13-3. Similarities exist between the two classes in the sense that all require, at a minimum, each of the following functional areas:

- Timing.
- Addressing.
- Interface circuits.
- Read logic.
- Memory device.

13-4. By contrast, although class 1 devices require *write control logic* and *erase control,* the *read only memories* do not.

13-5. **Types of Access.** The similarities of different memory devices can be further defined by the type of addressing media used. Currently, the two modes used most extensively are the *random access* mode and the *sequential access* mode. The two modes are well defined, and you have studied each. The random access mode allows for rapid entry or recovery of data without limitations, while sequential access requires an address to await its turn to memory. The systems in the table given above can be categorized once again into the address modes. The following table shows the access commonly used with the system:

Random	*Sequential*	*Either or Combined Mode*
a. Core	*a.* Drum	*a.* Disk
b. Storage tube	*b.* Delay line	*b.* Thin film
c. IC	*c.* Program	*c.* Program
d. TROS		*d.* Tape
e. CROS		

13-6. **Types of Memory Address Circuitry.** Four types of address circuits are widely used in computer systems. They are:

- Registers.
- Counters.
- Decoders.
- Matrices.

13-7. Each of these types may be composed of a variety of circuits. Most extensively used is the flip-flop; it is used in the register, counter, and decoder. Combinations of flip-flops, transistors, or integrated circuits can be used to form ring counters or stepping counters. In addition, resistive ladders can be used in registers and decoders. Diodes, ICs, and transistors are used extensively with matrices and decoders.

13-8. **Types of Read/Write Cycles.** There are two basic types of read/write cycles—the *destruct* (volatile) and *nondestruct* (nonvolatile). The destruct read/write cycles which are most commonly used in core memory units require that a change in state (usually hysteresis) take place in order for current induction into the read logic circuits. Then the data is usually rewritten into the same location for future use. In the nondestruct read/write cycle, data from memory is sampled by various modes with no change to the memory media. The representative examples of this type of memory are magnetic tapes, disks, drums, thin film, punch tapes, and delay line. Also included in the class of nondestruct readout memory units are the *read only memories.* These units are fixed program elements which are activated by input control and sampled during read.

14. Message Processors

14-1. Message processors (MPs) provide a distinct function for data processing. They accept input data and convert it to a language acceptable to the machine. They also prepare data for transmission media. Of necessity, one of the primary requirements for circuitry within the unit is modulation and demodulation.

14-2. **Requirements for Circuitry.** To achieve modulation or demodulation, many methods may be selected. Along with the variety of methods is a wide range of circuits. Functionally, though, a limited number of requirements can exist. These requirements must be satisfied through design of circuits which are compatible with parameters of the system.

14-3. *Serial-to-parallel and parallel-to-serial conversion.* Almost without exception, messages are transmitted over a media in serial form. Also, data is processed in EDP units in parallel and serial form. We know from our study in Chapter 2 of this volume, that the EDPs are presently operating at rates up to 3 megahertz, but serial transmission operates at audio rates (1300-2400 Hz). Message processors, therefore, often contain conversion circuits. The various types may be flip-flops, binary cores, and monolithic shift registers. These circuits are almost always operated with timing as the controlling factor. Two or more separate timing gates or pulses are frequently used. For example, refer to figure 85. It shows a shift register. Assume that the input (parallel data) is loaded at a megahertz rate. Only one timing pulse of 1 microsecond duration is needed to dump the data into storage. Assume that the data message which is dumped is properly formatted for serial transmission. Clocking of each stage of the register results in a shift. If the clock is 1300 Hz, then, bit by bit, the data is shifted out. The same type of unit may be used to receive data. In this case, serial data is received and shifted into the register. Upon receipt of the last bit, a megahertz timing pulse triggers a readout in parallel. So, one functional requirement which is usually needed for message processing is an ability for serial-to-parallel or parallel-to-serial conversion. You might have also associated the speed times and their changes. Speed of data flow is a functional consideration.

14-4. *Speed reduction/increase.* When receiving or transmitting, data messages are caused to change their rate of speed per bit. This element is called frequency conversion. The primary condition to be maintained during the frequency conversion is the absolute accuracy of data content. To accomplish this a frequency divider may be used when data stored is shifted out at the rate of 1 bit each time that the divider produces a pulse. Data, for instance, may be loaded into a cyclic register (fig. 86, printed in the workbook). Timing, coincident with the data bit following the previously transmitted bit, causes succeeding bits to be selected during each cycle. The process slows transmission. An example of this method is shown in figure 86. The cyclic storage loop loads data at a rapid rate; 1 bit per timing bit 1. However, data bits are shifted out at a much slower rate. Notice that timing 2 is set to occur once each cycle plus 1 bit. Therefore, each time that coincidence occurs at the gate, a succeed-

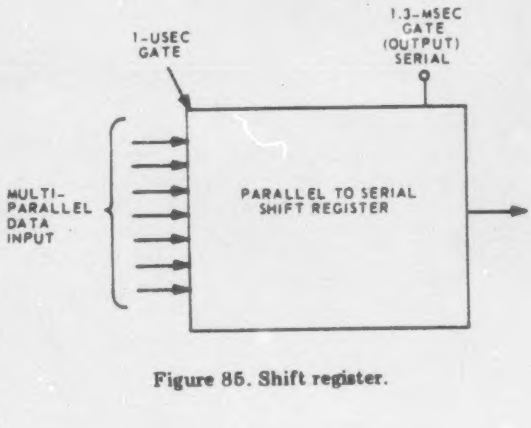

1-USEC GATE
1.3-MSEC GATE (OUTPUT) SERIAL
MULTI-PARALLEL DATA INPUT
PARALLEL TO SERIAL SHIFT REGISTER

Figure 85. Shift register.

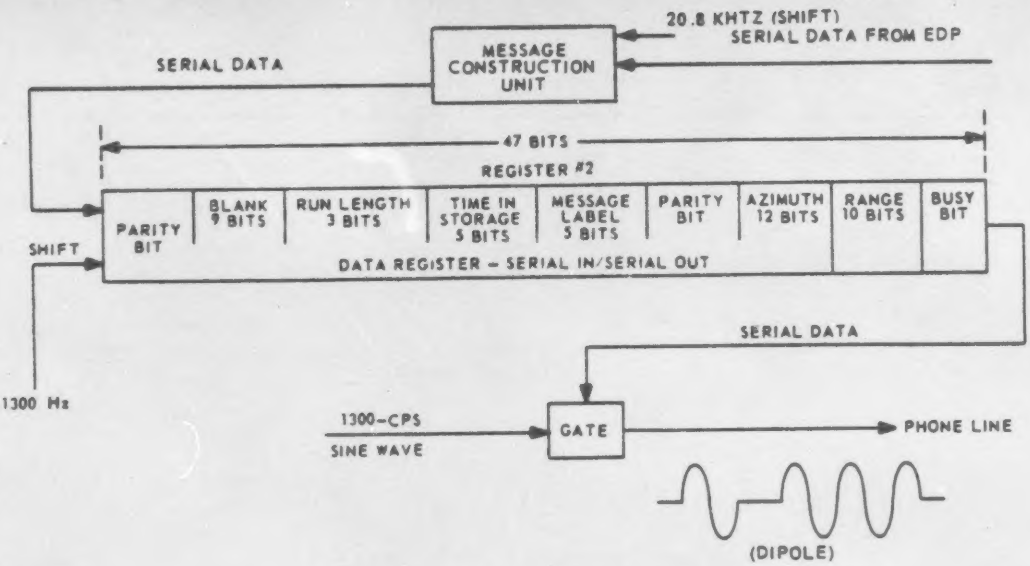

20.8 KHTZ (SHIFT)
SERIAL DATA FROM EDP
MESSAGE CONSTRUCTION UNIT
SERIAL DATA
47 BITS
REGISTER #2
PARITY BIT
BLANK 9 BITS
RUN LENGTH 3 BITS
TIME IN STORAGE 5 BITS
MESSAGE LABEL 5 BITS
PARITY BIT
AZIMUTH 12 BITS
RANGE 10 BITS
BUSY BIT
SHIFT
DATA REGISTER – SERIAL IN/SERIAL OUT
SERIAL DATA
1300 Hz
1300–CPS SINE WAVE
GATE
PHONE LINE
(DIPOLE)

Figure 87. Data processing (output).

ing bit of the message is gated out.

14-5. This same cyclic loop may be used to input data messages into an EDP. Received data can be loaded at the receive transmission rate. When loaded, timing 1 initiates a high-speed shift out. Timing also brings into focus another functional consideration—*time sharing*—which is sometimes called time division or multiplexing.

14-6. *Time sharing*. A message processor may be designed to transmit data to, or receive data from, a number of different stations or devices. A system of priorities may be established to accommodate all stations. Sequencing, on a recurring cycle basis, may be used to allow all media to gain access. To accomplish this function, time sharing is incorporated and various forms of circuits are available. Some of the typical circuits used are:

- Switches.
- Counters.
- Switching networks.
- Triggering.
- Decoder units.
- Encoder units.

14-7. Switches, triggering circuits, decoders, and encoders may use an assignment of numerics representing a specified priority system for the processing of multimedia data messages. Counters and switching networks often operate on a recycling principle. Through the priority circuits, all channels may have equal time for access, or selected (high-value) channels may have more than one access period per cycle. Now that you know something about message processor requirements, let's examine some of the different types of message input/output processors.

14-8. **Typical Message Input/Output Processing.** The objective to be attained in the study made here is to identify the common goal of preparing messages for transmission to another media without real concern for mes-

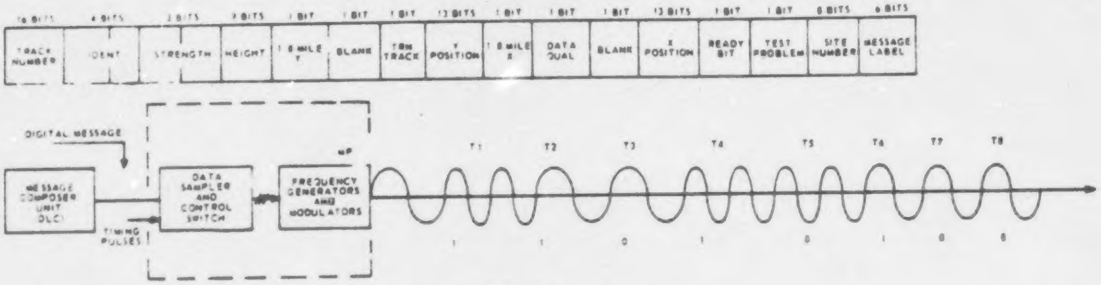

TRACK NUMBER
IDENT
STRENGTH
HEIGHT
BLANK
Y POSITION
DATA QUAL
BLANK
X POSITION
READY BIT
TEST PROBLEM
SITE NUMBER
MESSAGE LABEL
DIGITAL MESSAGE
MESSAGE COMPOSER UNIT (DLC)
TIMING PULSES
DATA SAMPLER AND CONTROL SWITCH
FREQUENCY GENERATORS AND MODULATORS
T1
T2
T3
T4
T5
T6
T7
T8
1
1
0
1
0
1
0
0

Figure 88. Message processor.

sage content. The study presents a few examples of conversion of digital messages into forms of voltage patterns which are acceptable to transmission media.

14-9. In figure 87, data from the target processing equipment is routed through the message construction unit which slows the data bit rate (frequency converts). The data message is then shifted out serially with a 1300-hertz shift pulse. It goes to an output gate where each binary one produces one cycle of a 1300-hertz sine wave, and each binary zero produces a voltage level. In figure 88, the digital message is composed in the unit preceding the message processor. You can see from the figure that this message contains many more bits of data; however, coming into the message processor, the similarity is close. The data sampler and control switch circuits consist of flip-flops. Each binary one causes a change in states. The output of the data sampler triggers the appropriate frequency generator (one of three), and the generator produces continuous outputs until the data sampler unit senses another binary one. A change in the state of a flip-flop results in selection of another frequency generator, and the cycle repeats. The resultant output is known as *frequency shift keying*.

14-10. The third example, shown as figure 89, represents a type of message which contains data other than machine initiated data. This is the portion of the message labeled *operator inserted data*. Using a keyboard, an operator types his message and the machine converts it to digital (we discussed this under *keyboards* in Chapter 1). Data bits which form the message are loaded into the output parallel-to-serial shift register where they are serialized and modulated into a complex waveform. This waveform contains phase shifting and amplitude modulation of a basic carrier frequency. The data bit groups (8 bits) are converted into *tones* within the modem. The tone is dependent upon the ones and zeroes combination in each character and the transmit bit rate. The tone generators cause a composite phase shift equal to the sum of the detected data. The phase shift signal is superheterodyned into the phone lines at a 0-to 3-kHz rate.

14-11. Alignment instructions, given in the technical order, prescribe exact prerequisites for sequence.

14-12. **Perform a Data Detection Circuit Alignment Study.** Title: *Signal Level Detector Alignment*. Objective: *The purpose of this alignment is to adjust the receiver sensitivity to inhibit message processing of incoming data when the received signal level is too low.* This alignment is performed in a modem unit, and the circuit functions similarly to the noise canceler circuit in a quantizer. If the receive level of a transmitted data message drops below a specified db level, the data-to-noise ratio drops. Below a specified ratio, noise can be interpreted as data just as noise can be interpreted as radar video input to a quan-

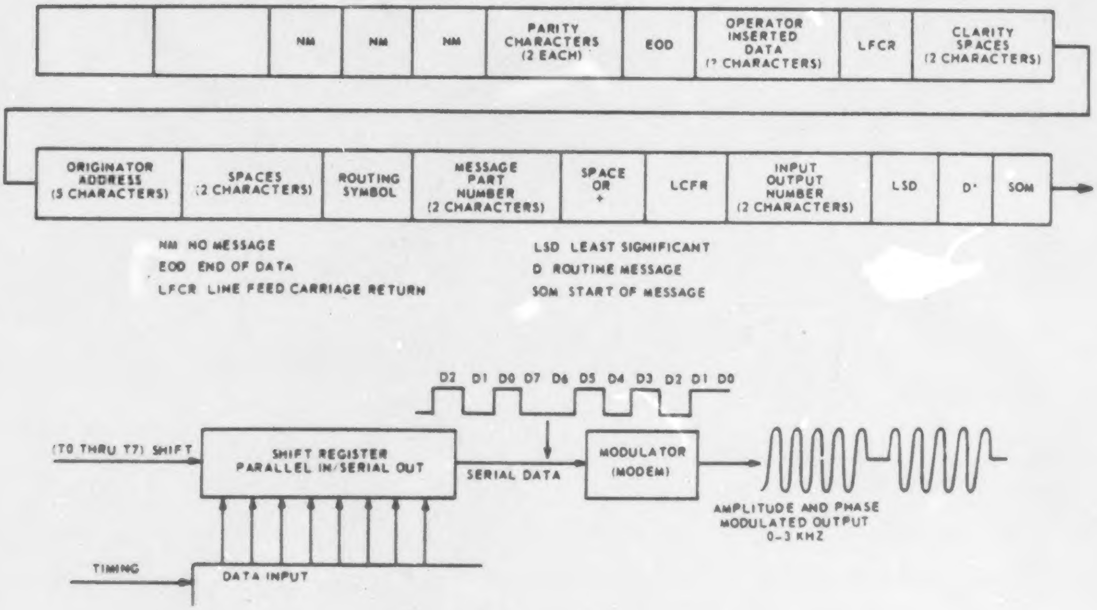

NM
NM
NM
PARITY CHARACTERS (2 EACH)
EOD
OPERATOR INSERTED DATA (? CHARACTERS)
LFCR
CLARITY SPACES (2 CHARACTERS)
ORIGINATOR ADDRESS (5 CHARACTERS)
SPACES (2 CHARACTERS)
ROUTING SYMBOL
MESSAGE PART NUMBER (2 CHARACTERS)
SPACE OR +
LCFR
INPUT OUTPUT NUMBER (2 CHARACTERS)
LSD
D'
SOM
NM NO MESSAGE
EOD END OF DATA
LFCR LINE FEED CARRIAGE RETURN
LSD LEAST SIGNIFICANT
D ROUTINE MESSAGE
SOM START OF MESSAGE
D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0
(T0 THRU T7) SHIFT
SHIFT REGISTER PARALLEL IN/SERIAL OUT
SERIAL DATA
MODULATOR (MODEM)
AMPLITUDE AND PHASE MODULATED OUTPUT 0-3 KHZ
TIMING
DATA INPUT

Figure 89. Modulator output unit.

tizer. Therefore, this alignment is performed to insure that only data received at the proper db level is processed, and that noise received at a low db level is inhibited.

14-13. *Processor theory.* The demodulator section of this modem receives a frequency shift modulated (FSM) signal input from a 600-ohm balanced transmission line. When no data is being received, the input to the demodulator consists of alternate ones and zeroes.

14-14. When incoming data is received, the front end of the unit references the data to modem ground, amplifies the signal, and detects the data. It also causes the data to be synchronized with the receiver timing.

14-15. An automatic gain control (AGC) circuit is also incorporated into the front end and regulates gain of the amplifiers much as a radio AGC circuit does. This AGC circuit also influences the level detection circuit operation.

14-16. The normal flow of data, as shown in figure 90 (printed in the workbook), is indicated by the heavy line passing through the blocks. The signals pass through:

- Bandpass filters.
- Equalizers.
- Shaping circuits.
- Phase shift networks.
- Discrimination circuits.

14-17. *Align the level detection unit.* Step 2 (fig. 66, printed in the workbook) requires an identification of the circuits within the alignment. To facilitate illustrations and unify the text, the heavy blocked-in area containing the level detector is included with the interrelated circuits. This is normally a function of step 3 (fig. 66).

14-18. Interrelationship of the level detector circuit to other functions shows (in fig. 90, printed in the workbook) that it is almost like a generator. It is nearly independent, and all other circuits are dependent upon its operation. The TR pulse is a feedback pulse and is generated as a result of all circuits functioning. The TR pulse provides a DC level plus pulse to the AND gate which is processing data. Should it be an improper level, no data processes.

14-19. This alignment presents us with a situation slightly different from those previously discussed. The level detector circuit is an input control device and causes all other control devices to be dependent upon its setting. In this analysis, it is necessary to look ahead to find that understanding. Interruption of data is directly related to the operation of this circuit. Verification, then, of data, valid data, or no data may be directly related to positioning of the level detector pot.

14-20. For the alignment to be performed, substitution of input db level signals is made by use of a signal generator, electronic counter, AC voltmeter, and multimeter. Refer to the level detector circuit in figure 90 (printed in the workbook).

14-21. The input to the level detector should be approximately +3V. If the adjustment has been made correctly, Q19 is held at cutoff, and Q20 conducts while Q21 is held at cutoff. This provides a +5V level and enables the data to be processed. Should the input drop below this acceptable level, Q19 conducts, Q20 cuts off, and, with Q20 cut off, a positive voltage is felt on the base of Q21 causing it to conduct. Since Q21 is conducting, its output goes to a low logic level and prevents the data from passing through the inhibit gate.

14-22. Establishing the proper operating level of the detector circuit requires that a 6- to 24-microvolt RMS transformed input signal provide a 5VDC detector level output and that a 5-microvolt RMS input signal provide a 0VDC level output. This indicates that 100 percent of the noise is inhibited with a magnitude input of 5-microvolt RMS or less. Also, this indicates that weak data and strong noise with magnitude between 5 and 6 microvolts RMS cause the detector output to be 5VDC, and above 6 microvolts RMS, the output provides a 5VDC level. The TR (transition) level arms the data gate.

14-23. Based upon information presented in this section, we can see that for alignment to be meaningful:

- Incoming and outgoing data conversion must be understood.
- A unit usually processes data in serial fashion, and later in processing converts the data to parallel.
- Multiple input source use of message processors may be used but on a time-sharing basis, again restricting the processor to coding or decoding individual messages.
- Alignment routines generally require extensive use of AC (RMS) meters, frequency and electronic counters, signal generators, and oscilloscopes.
- Steps in alignment are usually sequenced to allow for proper processing procedures.
- Prerequisites are usually identified.

CHAPTER 4

Programming

AS THE AIR FORCE entered the space age, the need and use of electronic computer systems increased. One of the first large-scale computers to evolve was the AN/FSQ-7. This computer was, and still is, used in the Semiautomatic Ground Environment (SAGE) System which is an aircraft control and warning system. The mission of SAGE requires its computers to perform specific operations rapidly, accurately, and most important, reliably. Because of the immense size of an AN/FSQ-7 computer (it uses approximately 50,000 vacuum tubes and thousands of other electronic components), a team of engineers was assigned the task of determining its reliability. Their study showed that this computer would experience its first failure after approximately 32 hours of operation. Even more astounding was the fact that once the initial failure was corrected and power restored to the equipment, another failure would occur almost immediately. In order to increase the reliability of this system, two complete AN/FSQ-7 computers were used. (You will recall that this is known as duplexing or redundancy.) Also, a marginal checking system was used to increase the mean time between failure (MTBF). Marginal checking provided for the detection of weak components before they had a chance to fail. In an attempt to simplify AN/FSQ-7 troubleshooting and reduce downtime, maintenance programs were developed. The first printouts that were provided by these programs contained large amounts of information, some of which was in no way related to the problem area. Only after considerable refinement were these programs and their printouts useful as a maintenance tool.

2. As the saying goes, "You've come a long way, baby," so too have our computer systems. Computers have advanced through vacuum tubes, transistors, and microelectronics into modular systems. Newer computer systems have virtually eliminated the need for duplexing and marginal checking. Improvements in the quality, effectiveness, and instruction complement (less instructions needed to perform the same functions) of the software have resulted in greater reliability and maintainability of computer systems. In other words, your job as an electronic computer systems repairman continues to be simplified as the computer industry continues to make state-of-the-art improvements. With all of these improvements, you will find that many of the basic theories associated with the software and hardware of the first large-scale computers can still be related to many of the newer systems of today.

3. In this chapter we are primarily concerned with programming, but we do not intend to try and make a programmer out of you. The programming we will study here is maintenance programming. A repairman doesn't need the depth of programming knowledge that a computer programmer needs, but he does need enough knowledge of maintenance programs to:

- Analyze computer maintenance programs.
- Interpret computer maintenance program printouts.

15. Analyze Computer Maintenance Programs

15-1. You are probably thinking, "These guys have got to be kidding if they think that a CDC can teach me how to analyze all the maintenance programs associated with my computer system." We will be the first to admit that analyze is a big word. The part of the definition of analysis, as found in most dictionaries, that we are concerned with here is limited to: *the separating or breaking up (of any whole) into parts so as to find out their structure, proportion, relationship, and function.* This is what we intend to do. We will look at maintenance programs as a whole; in other words, how does a maintenance program function in the hardware to identify and isolate malfunctions? You will recall that earlier we stated, "Many of the basic theories used in the software (in this instance, maintenance programs) for the first large-scale computers can still be found in the software of the newer systems." This fact would seem to enforce the adage, "The theory doesn't change but the application does." Think about that.

15-2. **Maintenance Program Defined.** Just what is a maintenance program? What is its function, and how does it perform its function? These are questions that should be answered one at a time:

a. A maintenance program is any program designed to indicate whether or not a computer is capable of performing its intended function. When improper operation occurs, the program must specify the cause of the failure, and, if possible, it must designate the corrective action to be taken by you, the repairman. From this, you can see that the term "maintenance program" includes reliability, diagnostic, overall, and confidence-diagnostic programs as well as hard wired programs. Many programs such as the *on-line* (on-line as used here is synonymous with active, operational, and main control) and *utility* programs may give some indication that an error is present within the system, but normally they provide very little aid to the immediate maintenance effort.

b. The primary function of a maintenance program is to *insure system integrity*, i.e., to locate any existing or impending failure.

c. To adequately perform its function, the maintenance program must attempt to *treat all circuits in a manner which approximates the ultimate applications of the computer.* This criterion can only be met by treating computer circuits as strenuously as possible.

15-3. A maintenance program is used as a maintenance tool much as an oscilloscope and a screwdriver are used. Therefore, it is necessary that you know the functions, capabilities, and limitations of the maintenance program just as you must know the functions, capabilities, and limitations of the handtools that you use on the job. Your ability to select and use the right handtool for a particular job comes through experience. This fact is also true with maintenance programs. Your ability to select and use the right program for a particular failure will increase as you gain more experience on the job.

15-4. **Maintenance Program Considerations.** Recall from your earlier training that there are two basic classes of automatic computers: (1) special-purpose, and (2) general-purpose. Special-purpose computers are designed for one specific purpose and usually require only one program. This program is permanently stored or wired in the computer. The term normally associated with this type of computer is *fixed program.* The general-purpose computer is designed to be used for a variety of purposes. This type of computer is a stored program computer which employs some type of electronic mass memory.

15-5. Your technical school training should have taught you that a program, whether fixed or stored, directs the computer to perform a series of actions in accordance with a specific plan. The computer automatically calls out each instruction in sequence, interprets it, and performs as the instruction commands. The wired-in logic which controls the automatic functions is, in fact, a wired program, but it is classified as system hardware along with all nonlogic components of the computer. A stored program, whether stored in memory or on any other media inside or outside the computer, is classified as system software.

15-6. **Fundamentals of Maintenance Programs.** In performing its primary function of insuring system integrity, the maintenance program performs two fundamental tasks: (1) fault detection, and (2) fault isolation. Fault detection is the action of the program in recognizing malfunctions which might exist. Therefore, it is the most important task of the maintenance program. Fault isolation is the action of the program in isolating the malfunctions. To perform these tasks, maintenance programs are designed to:

- Exercise the hardware by using programmed instructions.
- Check program results against known standards, constants, and programmed instructions.
- Alert the repairman whenever malfunctions are detected and isolated. This can be done through the use of machine printouts, indicator lights, CRT displays, programmed error halts, audible alarms, or a combination of these.

15-7. Later in this chapter we will present and discuss examples of several maintenance program flow diagrams. This should reenforce your understanding of how program routines detect and isolate malfunctions.

15-8. **Failure Classification.** The design of the maintenance program is based on the particular system's hardware, its function, and the type of task the program must perform—i.e., detect and/or isolate failures. System failures fall generally into one of the three categories discussed next:

a. Catastrophic. This type of failure is continuously present (steady state) until it is repaired. It is normally easy to detect and isolate. The symptoms and fault indications of a catastrophic failure are very often clear enough to allow the selection of a maintenance program that will search out the trouble from a limited group of circuits within the suspected trouble area. However, at other times, it may be necessary to run a group of programs on a major unit or the entire system in order to isolate the failure.

b. Intermittent. You can really "lose your cool" and become quite frustrated when troubleshooting an intermittent failure. This type of failure is not continuously present within the hardware; it occurs only once or at random intervals. Because it appears and disappears at random, the intermittent failure presents an inconsistent set of symptoms and becomes extremely difficult to isolate.

c. Machine state. This type of failure is present only under certain conditions, such as after a certain sequence of instructions, after a specific instruction followed by a delay in time, or at a particular pulse repetition rate.

15-9. **Maintenance Programming Techniques.** There are many possible programming techniques which may be used to locate failures within the system's hardware. Five of the major techniques that are used in system maintenance programs are explained in the next five paragraphs. As you read through each technique, try and relate it to the systems maintenance programs that have become familiar to you during your training.

15-10. *Start small.* This technique, as the name implies, starts its operation by checking a small number of key circuits. These circuits are then used to check another small group of circuits. This process uses a continually expanding group of proven circuits to check out other groups of circuits until the total area within the scope of the particular maintenance program is checked. The "start small" process is thorough and well suited to diagnosing catastrophic failures and some types of intermittent and machine state failures.

15-11. *Start big.* Maintenance programs using this technique are designed to test the computer while it is operating in a manner similar to its operational mission. Because many sections of the computer are operated simultaneously when the "start big" technique is used, certain catastrophic, intermittent, and machine state failures (which would normally escape the attention of a "start small" program) are identified.

15-12. *Marginal checking.* Marginal checking is a must in many of our older computer systems. Basically, the technique is a method of preventive maintenance in which certain operating conditions are varied from their normal values in order to detect deteriorating components. The amount of variation necessary before a component malfunctions indicates its margin of reliability. Since component values normally change with age, the marginal check is a valid indication of how soon a component will need replacing. The most widely used methods of marginal checking found in many of our computer systems are the variation of AC vacuum-tube filament voltage and the variation of DC supply voltage. In older computer systems, these voltage variations are applied automatically under the control of maintenance program instructions or manually by the repairman. Many of the newer computer systems still use the marginal checking technique, but only manual voltage variations are used.

15-13. *Multiple clue approach.* Once an error is detected, a program using the multiple clue approach attempts to obtain the same error using varying sequences of instructions. If the error can be detected in a variety of ways, it is only necessary to locate the common conditions in isolating the error.

15-14. *Process of elimination.* You will find that certain errors in the computer system are very difficult to analyze. However, it is possible for a maintenance program using the process of elimination technique to aid you in locating errors. In this technique, sets of programmed routines are used to vindicate one area after another and, by a process of elimination, to infer the error to be in the remaining area not checked.

15-15. **Types of Maintenance Programs.** The terminology associated with the various types of maintenance programs employed in your computer system may be different from those in the following paragraphs. However, from the explanation of each type, you should be able to relate their functions with the programs in your system's program library.

15-16. *Reliability program.* The basic task in this type of program is to verify that a specified portion, or logical area, of the system is functional. Therefore, the reliability program stresses fault detection and generally minimizes isolation. Theoretically, if this type of program runs successfully (without a failure indication), the circuits checked are in proper operating condition.

15-17. *Diagnostic program.* The diagnostic-type program is constructed to isolate known failures. The emphasis is on isolating failures to a restricted area and, when possible, to the component that failed. Generally, a diagnostic program doesn't attempt to integrate large-scale operations or to isolate failures associated with the operation of widely divergent areas of the system. It may begin by checking a circuit and then include another small increment of circuitry for each successive test. This process is extended until all circuits included in the program have been checked. The diagnostic programs used in modern day computers combine reliability and diagnostic programming. Thus, the maintenance function is enhanced since one program exercises the circuitry and provides for detection and isolation of malfunctions.

15-18. *Overall program.* Major applications of this type of program are in such areas as drums, disks, inputs, and outputs. The overall program *starts big* using the entire area under test, and then it uses the *multiple clue* and *process of elimination* techniques for error detection. Normally, an overall program consists of the reliability, diagnostic, and marginal checking (if used in the system) routines necessary to check an equipment area.

15-19. *Confidence-diagnostic program.* This type of maintenance program is normally cycled in conjunction with the operational program, and in some instances is part of the operational program. Basically, confidence-diagnostic programs provide the particular computer system with the ability to monitor the operation of on-line and backup (sometimes called standby) hardware. Confidence-diagnostic programs are capable of detecting and isolating failures in the on-line and backup hardware, as well as monitoring hardware status.

15-20. **Causes of System Failure.** We could list numerous causes of system failure here, but we do not intend to list them all. The ones that we list are the most typical causes of trouble encountered in most computer systems today. The order in which we list them doesn't necessarily indicate the frequency of their occurrence in the particular system that you are maintaining. These failures are listed to enable you to recognize the need for maintenance program versatility to the extent that they can detect and isolate a variety of failures:

- Failing cards (opens, shorts, bent pins, etc.).
- Loss of voltage.
- Timing.
- Interface problems.
- Spurious or continuous output.
- Operator error.
- Program.

15-21. **Methods of Failure Detection and Isolation.** The typical causes of failure listed above will ultimately reveal themselves as belonging to the failure classifications which were described earlier—i.e., catastrophic, intermittent, or machine state. As we indicated, each class of failure requires that maintenance programs use specific programming techniques in the detection and isolation process. The programming techniques discussed previously are used to apply special fault-finding test routines. These routines may range from simple pattern control routines to lengthy and detailed timing checks. In general, the electronic construction of the area being tested determines the type of test routines to be performed by the maintenance programs. It is beyond the scope of this course to list and explain all of the maintenance program test routines associated with each computer system. However, the test routines that we will explain are representative of the maintenance program routines used in many of the computer systems in your career field. Along with some of our explanations, we will present a flow chart of the test routine to enchance its understanding. For a review of the more frequently used flow chart symbols, refer to figure 91 (printed in the work book), and the explanations below:

(1) Direction of flow (A). The direction of flow line is used to connect all symbols and indicate the flow. If the direction of flow is in the normal direction (left to right or top to bottom), it is not necessary to use the arrowheads.

(2) Operations (B). This symbol is used for all program operations not involving reading, writing, decisions, or modifications.

(3) Decisions (C) and comparisons (E). Many notations are used with the decision and comparison symbols. Some of the more frequently used notations and their functions are:

Notation	*Function*
= or EQ	On equal
≠	On not equal
> or HI	On greater than
< or LO	On less than
≥	On equal or greater than
≤	On equal or less than
+	On positive
-	On negative
= 0	On zero
≠ 0	On not zero
Y	On yes
N	On no
T	On true
F	On false

(4) Modifications (D). This symbol denotes an alteration in the address or operation part

of an instruction. It may also be used to denote changes which are essentially counting in nature.

(5) Connector (F). This symbol is used to connect remote portions of a flow chart with one another without the use of long or crossing lines. An *exit connector* terminates a flow line. It is normally labeled with a number or letter reference. The program will then continue at an *entry connector* symbol which is labeled with the same number or letter reference.

(6) Stops (G). All programmed halts are indicated by this symbol. The word HALT and the number of the halt are usually placed within the symbol.

(7) Data entry symbols (H, I, J, and K). The symbols shown indicate sources of data entry.

15-22. *Computer test program.* A computer test program includes routines that check the logic circuits within the computer for correct operation. This is done by performing various computer instructions with the use of selected data constants. The instructions performed by the computer are checked in a sequence which assures that each instruction has been checked before it is used in later tests. Therefore, the computer circuitry whose correct operation has not been verified is not used in checking other circuitry. Normally, each instruction tested is exercised only to the extent necessary for verifying the correct operation of its logic circuits. These routines do not exercise all possible variations of the instructions in the computer. Therefore, the logic circuits involved in these variations are checked through the use of other instructions which use the same logic circuits.

15-23. For a close examination of the operation of a computer test routine, refer to figure 92 (printed in the workbook). Here you will find a small portion of a typical flow chart for a computer test routine. The flow chart indicates that the add class instruction is to be checked. There are many programming methods of performing this type of check. The method shown in figure 92 performs the check as explained below. Notice that each lettered paragraph corresponds to a lettered box in the flow chart:

a. The number 4 connector indicates entry from the control portion of the maintenance program. Upon entry to this particular ADD class routine, the control program performs the required housekeeping routines, such as loading the required constants to be used by the routine, clearing various counters, and performing any other control functions required by the routine. For this particular routine, the constants used are all 1 bits located in memory location 100. Other memory locations are loaded with the predetermined sum for each add operation to be performed.

b. The accumulator (also referred to as the working register) is cleared, and the pass counter is reset.

c. The contents of memory location 100 (all ones) are added to the cleared accumulator. When this addition is completed, the accumulator should should contain all ones.

d. The contents of the accumulator are compared with the memory location containing the predetermined results for this addition (a constant loaded by the housekeeping routines of the control program).

e. If the accumulator is not equal to the predetermined sum, the test routine determines the failing bit or bits and stores this error information in a specified memory area. All error information is printed out, and the program halts. The printout and any other failure indications are analyzed by maintenance personnel to determine the required corrective action. Once corrective action is taken, depressing the continue pushbutton (PB), or its equivalent, restarts the program at step *b*, connector 6; the same addition check will be cycled in order to confirm the corrective action.

f. If the sum of the first addition is equal to its predetermined sum, the pass counter is checked to determine if it has been stepped to 1. The pass counter has two primary functions: (1) its count determines whether the program branches (jumps) to step *c* or the next test routine, and (2) its count is used to determine what predetermined sum, from the memory constants, is used to compare with the results of a particular pass. For example, when the pass counter is equal to zero, the predetermined sum used is equal to all ones. When the pass counter is equal to one, the predetermined sum used is equal to the sum acquired when all ones are added to all ones.

g. The pass counter is stepped to one, and the program branches to step *c*. The second check (which will be a different variation) of the add class instruction is performed. Location 100 is added to an accumulator that contains all ones. Recall that after the first pass the sum in the accumulator was equal to all ones and, as the program returned to step *c* from step *g*, the accumulator was not cleared. Therefore, during this pass we will be adding all 1 bits from location 100 to all 1 bits in the accumulator. In addition to checking the circuits which were checked in the first pass, the carry, overflow, and end around carry circuits will also be checked during this pass. If an error occurs during this second pass, the program halts. After the necessary corrective action has been completed, the program is continued by depressing the continue PB. The program will return to the first pass and cycle through the entire routine again. When step *f* is reached and the pass counter is equal to one, the program branches back to the control portion of the maintenance program (this is indicated at connector 5 of the flow chart).

15-24. Let's suppose that you were running a maintenance program that contained an add class test routine similar to the one just discussed, and the routine continued to fail during the first pass. You have taken all the corrective action indicated by the printout and other failure indications to no avail. What do you do now? Give up? Giving up is a "no-no" in our Air Force. What about setting up a loop in the area of the routine that is failing? You would then be able to scope the addition operation from point to point. Will it work? You better believe it will. Looping a routine while scoping the circuits being exercised is one of the best, if not the best, troubleshooting techniques for isolating a failure when all other techniques have failed. How do you set up a loop? Must you be a programmer to set it up? To answer these questions, let's set up a loop using figure 92 (printed in the workbook). We will assume that our failure is occurring in the first addition process at step *c*. The program writeup would be checked to determine where to insert an unconditional branch instruction. Remember, an unconditional branch instruction causes a program routine to jump to the address it specifies regardless of program conditions. Actually, for our particular routine, all you need to do is determine (from the program writeup) the memory location of the first instruction at steps *b* and *e*. Once you determine these locations, you change the first instruction in step *e* to an unconditional branch. The address portion of this unconditional branch instruction must contain the address of the first instruction in step *b*. Now our program will continue to loop through the add instruction, and you can scope the circuits involved.

15-25. The maintenance programs associated with many computer systems make provisions for you to establish a loop upon request. As a matter of fact, many program writeups contain instructions for establishing loops. These instructions are very detailed. They include explanations of routines that cannot be looped because of interaction with the control portion of the program. Therefore, when you set up a loop (other than a program directed loop) in a portion of a test routing, you should check to be sure that you are not interrupting other portions of the routine or control program. In other words, your ability to set up a loop within a maintenance program will primarily depend on your ability to analyze the flow of the particular program.

15-26. *Memory test program.* This type of program includes test routines that exercise all memory modules associated with the particular system in an attempt to verify their operation. The maintenance program techniques used within the memory test programs perform step-by-step checks of each function associated with the module being tested. These functional tests include routines which are designed to uncover faults resulting from marginal operation of the particular storage media and associated logic circuits. The test routines use various test patterns that are designed to exercise the storage media and logic circuits as rigidly as possible. A few of these test routines are described below. These routines are typical of those used in many of the memory test programs being used in the field today:

(1) Memory access and logic circuit test routine. The first portion of this routine tests the ability to gain access to and write all zeroes in specified memory locations. The data is then read and checked for correctness. In the second portion of this routine, the operation of the first portion is repeated, this time using all ones instead of zeroes.

(2) Beat test routine. There are two basic beat tests. The first writes all zeroes in each address of the memory module under test, and then one address is beat with ones. Beat is the process of performing the same operation (writing data, in this case) several times. All addresses (except the one beat) are then read and checked for a 1 bit. The second beat test writes all ones into the memory module under test, and one address is beat with zeroes. All the addresses (except the one beat) are then checked for a zero. A routine of this type checks for disturbance of the storage media and the sensitivity of the sense amplifiers.

(3) Core plane crosstalk test routine. Recall that crosstalk is the term used to express the effect that adjacent memory cores and core planes have on each other during write and read operations. This test uses a special test pattern to check each core within a memory module for possible failures resulting from crosstalk. Basically, this special pattern is

made up by alternately writing all ones and zeroes throughout the entire memory module so that facing core planes contain opposite test patterns. The contents of each location are read and checked for correctness.

(4) Addressing test routine. The primary function of this test is routine to check the address registers and decoders. Normally, this testing is performed by storing the address of each memory location into its respective memory location. Once the entire memory is loaded, a read and compare process of each memory address is performed. Refer to figure 93 (printed in the workbook) for a flow chart of a typical addressing test routine. An explanation of the flow chart follows. Notice that each lettered paragraph corresponds to a lettered box in the flow chart:

a. Entry to step *a* is from the control portion of the memory test program. At this time, the control program performs the required housekeeping routines.

b. The first memory location to be checked is read from memory. Each time that the routine returns to this step, a different address is read from memory.

c. The contents of each memory location are checked at this step to determine if the contents are equal to the memory address of that memory location.

d. The correct address of the memory location read from memory and the erroneous address contained in that memory location are stored in a specified memory area for future error analysis.

e. The error computation routine determines the failing bit position(s) and, if possible, the faulty addressing circuits.

f. The address of the memory location just checked is looked at to determine if it is the last location in the memory module under test. If it is not, the address counter is stepped and the routine branches back to step *b* of the flow chart. If the last memory location has been checked, the routine branches to the print error routine at step *g*.

g. When all the stored error data is printed, the routine branches back to the control portion of the maintenance program.

15-27. *Input/output (I/O) test program.* An I/O test program is normally made up of several individual test routines that are used to test the various peripheral equipments associated with a computer system. However, several of the older computer systems use separate test programs for each of their peripherals. I/O test routines perform test operations on such peripheral equipment as:

- Input/output keyboards.
- Card readers.
- Card punches.
- Printers.
- Message processors (or composers).
- Magnetic drums and disks.
- Magnetic tape drives.
- Paper tape punches and readers.

15-28. The following flow charts, along with their explanations, are presented to help you understand typical I/O test routines that you might be required to use in the field:

(1) Card reader and magnetic tape unit test. Refer to figure 94 (printed in the workbook). For this particular test, we are using five standard punched cards that are punched in a row binary code. Each card contains 24 words (30 octal).

a. At step *a*, the test checks for a reader *ready condition*—i.e., cards in hopper, power on, etc. If *not ready*, the program will cause an alarm condition. Once the alarm condition is corrected, the program continues.

b. One card is read and check summed. Recall that a check sum is a programmed check in which the bits read are summed. This sum is then checked against a previously computed sum to verify the data read.

c. If a check sum error occurs, a printout is provided identifying the error. After corrective action is completed, the program is continued.

d. If the last card has not been read, the program returns to step *a*. A determination for the last card being read is made by checking a word counter for a count of 120 (five cards with 24 words each). This type of counter is stepped as each word is read (or written). Thus, its count indicates whether the desired number of words has been operated on.

e. As at step *a*, a check is made for the *ready condition* of the particular I/O device. If the magnetic tape unit is *not ready*, or if it is *file protected* (this condition prevents writing), the program will cause an alarm condition to occur. Once the alarm condition is corrected, the program continues.

f. Tape is positioned to effect a write operation of 120 words. Other setup conditions, such as clearing certain counters, would also be performed at this time.

g. At this step, a check is made to determine if 120 words have been written. The same word counter used in step *d* could be used here for this check. If 120 words are not read, the program causes an alarm condition. Once the alarm condition is corrected, the program continues.

h. The programmer knows the operation, the device, and the number of times the operation is to be performed. He also knows how much time is required to perform a certain operation with a given I/O device. With these facts, the programmer can check (using programmed instructions) the device's ability to perform a given operation in a specific amount of time. In our program flow chart, the programmer is set up to write one record consisting of 120 words. At step *h*, he checks the tape drive's ability to complete the write operation in the time he allotted.

i. If enough time remains to complete the operation, the program returns to step *g* and checks the word counter to determine if 120 words have been written.

j. The elapsed time error routine first determines if, in fact, 120 words were written. If not, the number of words actually written and the total time used to write them are printed out. Depending on the system, other information is provided at this time. Once corrective action has been completed, the program will continue at step *e*. If the program then runs to completion, this indicates that the corrective action did the trick.

k. If 120 words are written in the allotted time, an end-of-record (EOR) indicator is written on the tape. The program then causes the tape to backspace to the beginning of the record which was just written. A read operation is now performed.

l. At this step, the data read from the tape is compared with the data read from the cards. A printout is provided if any errors are detected. Once corrective action is completed, the entire test is cycled again to affirm the corrective action. If all data compares at this step, the program continues on to the card punch test (indicated by connector 6).

(2) Card punch test. Refer to figure 95 (printed in the workbook). This test determines whether the card punch can perform its function correctly.

a. At this step, a check is made to insure that the punch is *ready*. If the punch is *not ready*, the program will cause an alarm condition to occur. Once the alarm condition is corrected, the program is continued.

b. Now, five cards will be punched. The data that is punched is the same data that was read from the tape at step *h* of figure 94 (which is actually the original data read from the cards at step *b* of fig. 94, printed in the workbook).

c. Here a check is made to determine if five cards have been punched. This is done, as before, by checking a word counter for the count which indicates that 120 words were operated on.

d. As in our last test in figure 94, step *h*, a check is made to determine if the I/O device performed its operation in the time allotted by the programmer.

e. If enough time remains to complete this punch operation, return to step *c* and check to see if five cards have been punched.

f. An elapsed time error routine is used to determine if, in fact, 120 words were punched. If not, the number of words actually punched and the total time used to punch them are printed out. Once corrective action has been completed, the program is continued at step *a*. If the program then runs to completion, this indicates that the corrective action did the trick.

g. At this step, the operator is told to check the cards punched against the cards read at step *b* of figure 94. If punching errors are noted, the required corrective action is taken, and the punch test is recycled according to the instructions in the particular program writeup.

h. We have indicated a halt here, but the particular program could branch to another test of another I/O device.

15-29. The maintenance program routines associated with the computer system that you are now receiving training on may not be identical to those we have discussed in this chapter. However, as you become familiar with more of the program routines used in your system, you will note many similarities to the routines presented here. As a matter of fact, as you gain more experience on the job, you will even detect many similarities among the maintenance programs used by your system. The knowledge of these similarities should aid you in isolating failures. For example, let's assume that you were running the I/O test program routines explained in the preceding paragraphs and the last routine (punch test) failed. In examining the failure printout and other indications, you found that the I/O word counter had not stepped. Would you immediately start out to troubleshoot the I/O word counter circuits? In view of the fact that the magnetic tape and card reader test routine (it also used the I/O word counter) cycled without failure before the punch test routine, the logical point at which to start troubleshooting would be within the punch control circuits. More explicitly, check the punch control circuits that provide the pulse and/or level which affects the stepping of the I/O word counter. You should not rule out the word counter circuits completely, but they definitely should not be the first ones to check. Along with the knowledge of maintenance program similarities, you will need to become proficient in the art of interpreting maintenance program printouts if you are to become an effective troubleshooter.

16. Interpret Maintenance Program Printouts

16-1. As stated earlier, many of the failure printouts which were generated by the older computer systems left a lot to be desired. However, as the software improved, so did the usability of the failure printouts. Your effectiveness as a repairman will depend a great deal on your ability to interpret the failure printouts provided by the various programs in your particular computer system. It might be hard to believe, but work centers have often suffered excessive downtime because maintenance personnel misinterpreted a particular failure printout. Our Air Force has expended large sums of money to provide you with the best maintenance program publications available. Your on-the-job training will include many hours of studying these publications. This study will be rewarded by the respect you gain from your coworkers and supervisors every time that you interpret a failure printout correctly and take the right corrective action. Normally, depending on the system you are assigned to, maintenance program descriptions can be found in chapter 4 of the TO or section 4 of the appropriate manufacturer's service manual. As your training progresses and you become familiar with more of the maintenance programs in your system, one thing that should quickly become apparent to you is the standardization of these programs.

16-2. **Standardization of Maintenance Programs.** In each computer system, program standardization is essential in order to reduce the cost of the system and increase its usability. Within a given system, most programming aspects have been standardized—particularly program organization and operator communication.

16-3. *Program organization.* This is the most important aspect of a successful programming system. Each program that is written must be organized in consideration of its functional relationship to the total system. Some maintenance programs are *executive control oriented;* that is, they are designed to be operated in conjunction with (or by) some type of control program. Other maintenance programs do not require external control and are designed to be *self-control oriented.* Other areas of program organization that you will see during your training are flow charts and tagging.

16-4. Flow charts. Recall that flow charts consist of a series of blocks, each containing a description of a computational function. As explained before, the particular flow chart symbols may change from system to system.

16-5. Tagging. Tagging makes a program easier to prepare and easier to understand by the original programmer, succeeding programmers, and those who use the program flow charts and descriptions. Many methods can be used in tagging instructions. In one method, a program listing is divided into blocks of logical functions. Each block has a header giving its name, function, and communication data. All data words, or constants, which are referenced in the block are grouped together and placed at the end of the block. Within the functional block itself, instructions and data can be tagged with a three-part tag to show block identification, type of reference, and a digit to distinguish several references of the same type. For example, the third part of a particular function tag, N4, might be any of the following:

- E - Entry
- F - Exit or final.
- M - Instruction that is modified.
- C - Constant (unmodified).
- T - Temporary constant.
- I - Input communication word.
- O - Output communication word.

In conclusion, the functional block N4 might have internal tags N4E, N4M1, N4M2, N4F, N4C1, N4C2, or N4T.

16-6. Control program. A maintenance control program is a package of control and helper routines that facilitates the loading and operation of the various maintenance program routines. The control program portion of a maintenance program provides special routines that fulfill common requirements of the program's test routines, thus preventing needless duplication of programming effort. For example, the same print, interrupt, or manual intervention routine is used by the various test routines in a maintenance program. A maintenance control program can be included as part of the on-line (active or operational) program, as well as a backup (standby) program. In this environment, it is time shared with the on-line and backup program, and it provides confidence-diagnostic checking of the system hardware. However, a maintenance control program can be strictly associated with an off-line environment (for example, scheduled maintenance period).

16-7. *Operator communication.* Depending on the particular system, operator communication can take on many forms. The more standardized types include interrupts, manual intervention, and printouts.

16-8. Interrupts. You are able to interrupt the processing of a maintenance program by initiating an external request from such devices as an external keyboard, a status maintenance console, a display console, or a test simulator. The method used by the control program to honor your requested interrupt is an interrupt processing routine. Once the control program recognizes the interrupt as a legal request, control is given to the requester. He can then enter additional data, initiate or change specific switch settings, or make ready and identify other hardware for testing.

16-9. Manual intervention. The manual intervention and interrupt are similar. In order to distinguish between the two, think of the manual intervention as being preprogrammed by the programmer. That is, at specified points in a given maintenance program, the program requests specific actions to be taken by the operator. These actions include setting specific switches, preparing card or tape inputs that will furnish needed information for the test, or making ready and identifying other hardware for testing.

16-10. Printouts. Standardization of maintenance programs is insured to some extent if a set of print routines (within the control program) is used by the various maintenance program test routines. The following items are considered essential to uniformity of program printouts, and the maintenance programs of the many systems normally adhere to them:

- Program heading.
- Results of program run.
- Error information—data failure, control failures, etc.
- Indicated repair statements.

16-11. Uniformity of Maintenance Program Error Printouts. Each computer system's maintenance program library insures uniformity of the format of its error printouts through the use of the four essentials indicated above. However, the experienced computer repairman and technician are the first to admit that their training on a new system would be a lot easier if all systems used the same data format on their printouts. Unfortunately, uniformity of the data format contained within each of the four essential items required on the error printouts varies from system to system. The following examples are presented to point out these differences. Note the identification of the four essential elements which were presented in the previous paragraph. These elements are identified on each printout as follows: ① = Program heading; ② = Results of the program run. ③ = Error information; and ④ = Indicated repair statements.

16-12. *AN/FSQ-7 (SAGE) maintenance program printout:*

```
   ⎧ THE FOLLOWING PROGRAM WILL BE OPERATED UNDER CONTROL OF SMCP 3
   ⎪
   ⎪ CDS 1L     TAPES MC 1L    2606
   ⎪ A COMPLETE DIAGNOSTIC AND MARGINAL CHECKING TEST OF THE TAPE DRIVES,
①  ⎨ TAPE ADAPTER UNIT AND ASSOCIATED CIRCUITRY.
   ⎪ +++++++++++++++++++++++++++++++++++++++.
   ⎪
   ⎪ SS1-OFF   SS2-OFF   SS3-OFF   SS4-OFF   BSW 0.10100  1.00000
   ⎪
   ⎩ NOW TESTING LOGICAL DRIVE 3 WHICH IS PHYSICAL DRIVE ---.

②    4 . . . . E . . 2 . . . .  +150-040   FAILURE MC WORD 005 PRESCRIBED 40 ROUTINE 2

③  { TAPE DRIVE NO. 3
     REWIND DIDNT GIVE DISCONNECT

   ⎧ THESE PUS WERE MARGINED AND COULD CAUSE ERROR.
   ⎪ 13BJ
   ⎪
④  ⎨ THESE PUS WERE MARGINED BUT WOULD NORMALLY NOT CAUSE ERROR.
   ⎪ 13BS  13BL  13AP  13AJ  13AH  13BT  13BD  13BF  13BE
   ⎪
   ⎪ THESE PUS NOT MARGINED BUT COULD CAUSE ERROR.
   ⎩ 13BH  13BG
```

16-13. This particular printout is very definitive in that all the essential information is included. The program heading information, ①, is complete to the extent that it even indicates the setup condition of the program—i.e., sense switch (SS1 through SS4) and B switch (B Sw) settings. The results of the program run, ②, identifies that a margin failure using margin word 005 occurred. Also, it identifies the failure as being within marginal group 4, circuit line selection E2, and marginal voltage +150 volts. The failure occurred at the prescribed margin of -40 volts while cycling a particular test routine, routine 2. The error information, ③, identifies the tape unit that failed and includes a brief explanation of how it failed. The indicated repair action, ④, includes identification of the plug-in units (PUS) that could have possibly caused the margin failure.

16-14. *AN/GSA-51A (BUIC) maintenance program printout:*

```
MTU DIAG TEST USING COMP=1  MEM=8  CC=1 } ①

TEST=005    PCR=076152 \
                        } ④
DESC. NO    001        /

CONTROL WD. = 04 } ③

IP DR 0041040732110254  STATUS = 00 \
RS DR 0000000732522274  STATUS = 01  } ②
EX DR 0000000732522274  STATUS = 01 /

TEST WORD = 0404040404040404 \
                              } ③
WORD READ = 0101010101010101 /

FAULTY MODULE MTU 4, INTERFACE WITH CC 1 } ①
```

16-15. This printout for test 5 of the magnetic tape unit (MTU) diagnostic program is typical of the printouts provided by the maintenance diagnostic programs used in the BUIC system. The program heading, ①, includes such information as what computer (COMP), memory (MEM), and controller comparator (CC) were used during the test. The controller comparator is similar to an I/O control unit. Also included as part of the program heading is the faulty module number and the number of the controller comparator that this faulty module was interfaced with. Depending on the particular diagnostic test, the results of the program run, ②, consists of the in-process (IP), result (RS), and expected result (EX) descriptors (DR) which were processed during the test. Basically, descriptors are used to set up, initiate, control, and terminate data transfers between core memory and the terminal devices. Along with each descriptor will be an indication of certain status conditions. Status 00 indicates that the particular I/O operation was initiated satisfactorily, and status 01 indicates end of record. The error information, ③, indicates that a data comparison error occurred while reading tape unit 4. The 0 in the control word (WD) specifies a read operation, and the 4 specifies tape unit 4. If an error had been detected during the write operation, the control word printout would contain a 7 in place of the 0. The test word indicates what was written on the tape. The word that was read indicates what was actually read back from the same tape. The indicated repair statements, ④, in this type of printout are normally used with specific diagnostic tables which are contained in Chapter 5 of the particular unit's service manual (TO). Normally, the test number, contents of the PCR (program count register), and the DESC. NO. (descriptor number) are used with the diagnostic tables to determine the required corrective action. The corrective action indicated by the diagnostic tables can include, but is not limited to, the replacement of plug-in assemblies.

16-16. *AN/TSQ-91 operation central maintenance program printout:*

```
407L MAGNETIC TAPE DIAGNOSTIC PROGRAM

THE MTS DIAGNOSTIC PROGRAM HAS THE FOLLOWING SENSE SWITCH OPTIONS

SW1 - LOOP ON ERROR

SW2 - LOOP ON INTERMITTENT ERROR

SW3 - LOOP ON SYNCHRONIZER

SW4 - INHIBIT ERROR PRINTOUT

SW5 - ON AND OFF TO CONTINUE                                          ①

SW8 - OUTPUT ERROR TABLE

MOUNT SCRATCH TAPE WITH WRITE ENABLE RING AND DIAL UNIT ZERO.

PLACE UNIT AT LOAD POINT. PRESS UNIT ZERO ON LINE AND OTHER

UNITS LOCAL.

TYPE IN 7 TO CONTINUE

7

CHANGE MTS CARD CRR 000   ④
MTS ERROR TABLE
 MTS      ACT      EXP      ACT      EXP
 COM      STA      STA      DAT      DAT    ③   ②
511400   000000   500000   000000   000000
```

16-17. The program heading information, ①, for the above 407L magnetic tape diagnostic program printout includes the sense control switch (SW) options for the magnetic tape synchronizer (MTS) portion of the program. An example of the use of these switches would be SW8 ON to provide the MTS error table, SW1 ON to loop on error, or SW4 ON to inhibit the error printout while looping. Other information included here is the mounting of a scratch tape for writing and reading of test data (with a write enable ring in place to allow writing) and the identification of zero being dialed on the tape unit to be tested. A note is included in the program heading to remind the operator to make sure that the scratch tape is at load point. If the tapes were not at load point, an error indication would occur during the MTS portion of this diagnostic. Also, the tape unit is placed to an on-line status and other tape units are placed to local (effectively, off-line). The test is then started by typing in a 7 at the keyboard-printer-punch (KPP). The MTS test is the first test to be cycled. The magnetic tape synchronizer includes such circuits as tape control and computer interface. The results of the program run, ②, include both error information and indicated repair action. The error information, ③, includes detailed program data associated with the MTS test. MTS COM indicates the MTS command word generated by the program. ACT STA is the actual status word received from the MTS. EXP STA is the status word expected based on the preliminary setup conditions. ACT DAT is an indication of the actual data received, and EXP DAT indicates the expected data. Normally, this error table contains considerably more information. However, what we have presented should suffice to give you an idea of the printouts associated with the 407L diagnostic programs. The indicated repair statement, ④, CHANGE MTS CARDS CRR 000, is used with a functional card group table (located in the appropriate TO) to determine the cards to be changed. Before we jump into the middle of the MTS and start pulling cards, let's take a closer look at the error table. It is apparent from the actual and expected data indications that we did not have a data failure. However, in checking the status tables and breaking down the status words, we would find that the actual and expected status indicate that the tape unit under test was dialed to another setting besides zero. Recall that the program heading called for the tape unit to be dialed to *zero*. In other words, an *operator error* was the cause of this failure and not card group

CRR 000. Once zero is dialed into the tape drive that is under test, the program can be recycled.

16-18. Although the three printouts presented used different data formats for presenting failure information, they maintained uniformity in the sense that each printout contained the four essentials—i.e., program heading, results, error information, and indicated repair statements. *Once you are able to identify and interpret these four essentials in your system's printouts, your job of maintaining your particular computer system will be simplified.*

Troubleshooting

IN THE PREVIOUS chapters of this CDC, you gained an insight to the knowledges needed to perform the various duties associated with maintaining a computer system. As your trainer guides and directs you through the maintenance inspections and tasks associated with your particular system, this important fact should become apparent to you: *Successful mission accomplishment of a computer system is dependent on a system of scheduled maintenance inspections performed by competent maintenance personnel.* Wouldn't it be great if the effective performance of all scheduled maintenance guaranteed equipment infallibility? Of course, this is not the case since equipment failures can occur at any time. However, effective accomplishment of the scheduled maintenance inspections minimizes equipment failure. When a failure does occur in your system, you will be responsible for troubleshooting—i.e., for isolating and correcting the problem as fast as you can in order to return the system to the performance of its primary mission.

2. Troubleshooting, as we once knew it, has taken on a new dimension. With the advent of the computer and all of its shortcuts and wonders came a new age of troubleshooting. The computer figures our pay, works our math problems, and makes our life as a maintenance repairman something of a breeze. Yes, the computer can do all of these things as long as it functions properly. But, brilliant as it is, the computer (just like all of us) still has its problems. This is where you come in. All of a sudden this electronic brain (that has practically taken our jobs and made us look ridiculous because of its superior ability and speed in working math problems) has failed, and it is now at your mercy. As any good repairman dedicated to his profession should react, you will respond by curing its ills. Isn't this ironic? You may not be as fast or may not possess the abilities of that computer, but without you it is nothing more than several miles of wire and a maze of electronic hardware completely within your power. Now, while you are savoring this great feeling of power and pride, keep in mind that you will maintain your superiority only as long as you are able to maintain proficiency in troubleshooting your system.

3. Every computer system has many troubleshooting aids that are designed to make your job of isolating failures easier. Some of the more important troubleshooting aids that you might use on the job are:

- Fault indicators.
- System and unit testers.
- Performance test standards.
- Diagnostic programs.
- Flow diagrams.
- Specialized test equipment.

4. The various troubleshooting techniques presented in this chapter are representative of those used in troubleshooting most of the computer systems maintained by personnel in the electronic computer systems specialty. The computer system that you are maintaining, together with your personal abilities, will dictate the troubleshooting technique or techniques you adopt and excel in using. The troubleshooting techniques that we shall present fall within these four basic task elements:

- Analyzing logic and wiring diagrams.
- Analyzing oscilloscope waveforms and patterns, and signal tracing with an oscilloscope.
- Using and interpreting fault location guides and facility panels.
- Using the group removal and replacement method of pluggable units.

17. Troubleshooting Considerations

17-1. The basic troubleshooting procedures used in computer maintenance are generally quite logical. A good repairman will attack a problem by asking and trying to answer some simple questions. His first questions normally concern the causes of the trouble. As each question is answered, he eliminates some

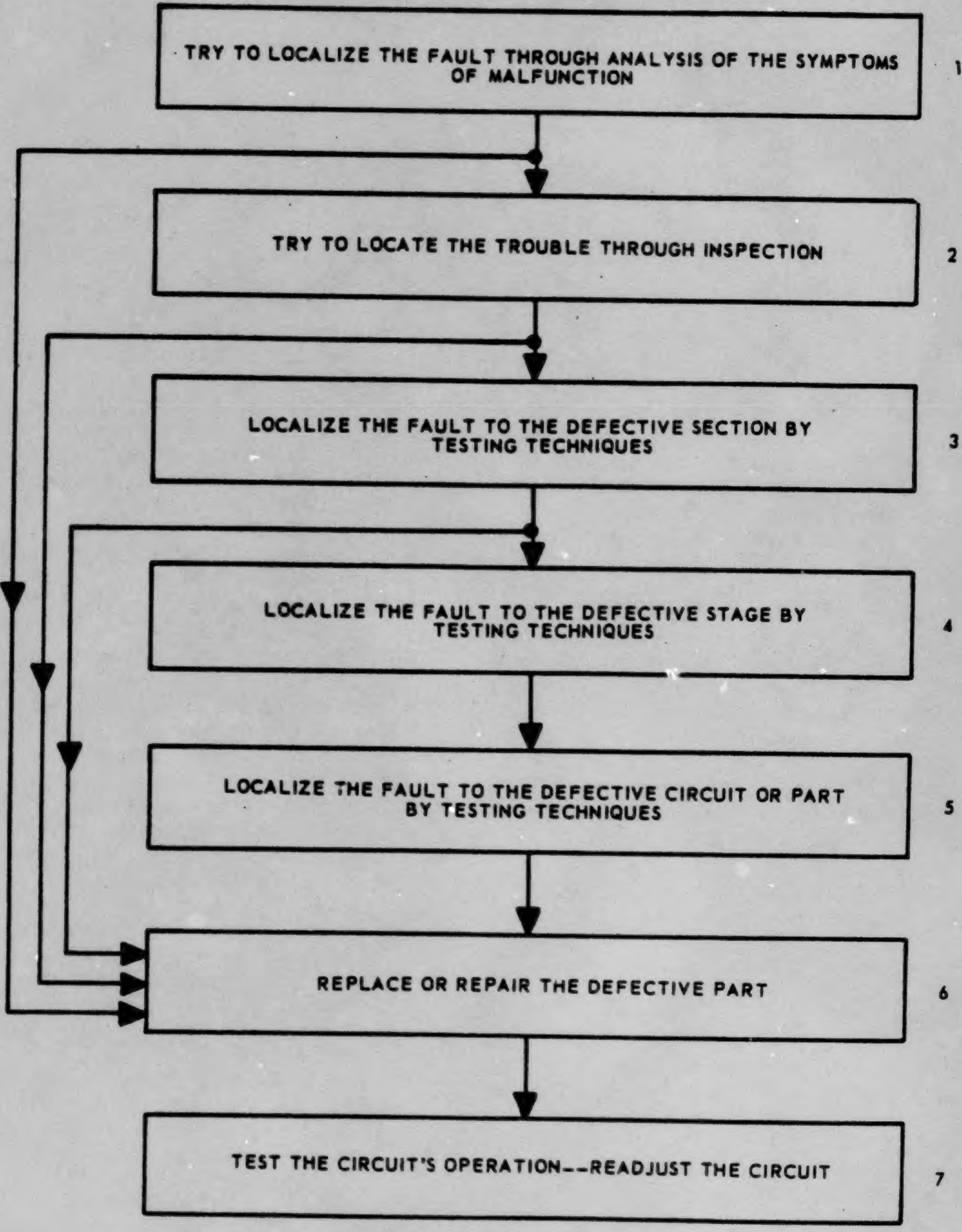

TRY TO LOCALIZE THE FAULT THROUGH ANALYSIS OF THE SYMPTOMS OF MALFUNCTION
1
TRY TO LOCATE THE TROUBLE THROUGH INSPECTION
2
LOCALIZE THE FAULT TO THE DEFECTIVE SECTION BY TESTING TECHNIQUES
3
LOCALIZE THE FAULT TO THE DEFECTIVE STAGE BY TESTING TECHNIQUES
4
LOCALIZE THE FAULT TO THE DEFECTIVE CIRCUIT OR PART BY TESTING TECHNIQUES
5
REPLACE OR REPAIR THE DEFECTIVE PART
6
TEST THE CIRCUIT'S OPERATION--READJUST THE CIRCUIT
7

Figure 96. Troubleshooting procedure.

possible sources of trouble, thus decreasing step by step the different areas which he must troubleshoot. How far he is able to proceed will depend upon his knowledge of the equipment and his ability to troubleshoot. His knowledge may permit him to locate the exact component that is causing the trouble, or it may only permit him to isolate the trouble to a cabinet or rack. However, with only a limited knowledge of the equipment and by using the correct procedure, the troubleshooter (you) will probably find the more obvious troubles.

17-2. **Know Your Equipment.** Remember, there is no substitute for equipment familiarization to aid you in troubleshooting your system. Why is this such an important consideration in troubleshooting? That's a good question. The best way to answer it is to ask you this question. If you are not familiar with your equipment to the extent that you can analyze its operation, indicators, printouts, and programs, can you isolate a failure within that equipment and take the proper corrective action?

17-3. **THINK Before You Act.** The most important step of any troubleshooting effort is to think before you act. Ask yourself, "What are the symptoms and what is most likely to be causing the trouble?" By asking and trying to answer these questions, you will be following a logical sequence of steps which will lead you to the cause of the trouble.

17-4. **Establish a General Troubleshooting Procedure.** The word "general" as used here means all-encompassing. Establish a troubleshooting procedure you can follow regardless of the particular hardware failure. Figure 96 presents a general troubleshooting procedure that can be used for just about any hardware failure encountered within a computer system. The directions given in blocks 1 through 5 are steps to be used in locating the trouble, and the directions in blocks 6 and 7 are steps to be used in repairing the unit. Steps 2, 3, 4, and 5 may sometimes be eliminated, but steps 6 and 7 must always be followed. In the paragraphs that follow we will expand this general troubleshooting procedure by incorporating specific troubleshooting techniques in steps 1 through 5. When incorporated into a troubleshooting procedure, the troubleshooting techniques presented will simplify the troubleshooting effort.

18. Analyze Logic and Wiring Diagrams

18-1. A computer is no more than a combination of simple devices which perform a few basic operations. Complexity arises from the fact that the logic is not standardized but varies according to the manufacturer. In 1960, MIL-STD-806A, *Graphic Symbols for Logic Diagrams*, was developed and approved by the Department of Defense for preparation of logic diagrams. Unfortunately, many computer systems were manufactured before this date; consequently, nonstandard logic symbols are still quite common. A point to remember is that the symbol representation varies from manufacturer to manufacturer, but the basic principle remains the same. Stated simply, no matter how it is disguised, an AND gate remains an AND gate, etc.

18-2. The manufacturers who have adopted the military standard have merely adopted the symbology but do not fully use the basic concepts. Figure 97 shows some of the variations of symbology which were developed from MIL-STD-806B, which replaced 806A in 1962. A manufacturer of a system used in the Strategic Air Command (SAC) converted all of its logic to MIL-STD-806B; however, the particular system used negative logic exclusively (thus requiring input and output state indicators on logic symbols). Therefore, the manufacturer decided to eliminate all state indicators. When using this particular system's logic, you must take for granted that the indicators are there. The idea worked until repairmen from other computer systems were assigned to this SAC system and applied the true principles of MIL-STD-806B. They found that without the presence of the state indicators, the system underwent a complete reversal and would not operate in accordance with the 806B standards they knew. It is apparent from this one example that the repairman's responsibility of recognizing the various types of logic (including the manufacturer's errors in applying MIL-STD-806B) becomes rather difficult. In order to broaden your knowledge, a variety of manufacturers' logic symbols is included in figure 97.

18-3. **Troubleshooting with Boolean Algebra.** You should recall from your tech school days that boolean algebra is a form of logic that uses mathematical symbols to describe logical processes. This type of logic was named in honor of George Boole, an English mathematician, who developed it in 1854. No practical use was made of this new type of logic until 1938. Then, C. E. Shannon, a research assistant at the Massachusetts Institute of Technology, discovered that this form of logic was perfect for indicating the logical functions of computer and telephone switching circuits. There are several advantages in having a mathematical technique for describing these circuits; it is far more convenient to calculate with equations than with schematics or logical diagrams. Just as an ordinary algebraic equation can be simplified using basic theories, equations describing logical conclusions for arithmetic operations, logical decisions, and switching networks can also be simplified. This enables the designer to devise the simplest logic to perform a function. It also enables you, the repairman, to understand and troubleshoot with the logic, thus achieving efficiency of repair and maximum operational availability. Normally, troubleshooting with boolean algebra involves the development and use of a boolean equation or truth table.

18-4. *Developing boolean equations.* A boolean equation is developed from certain

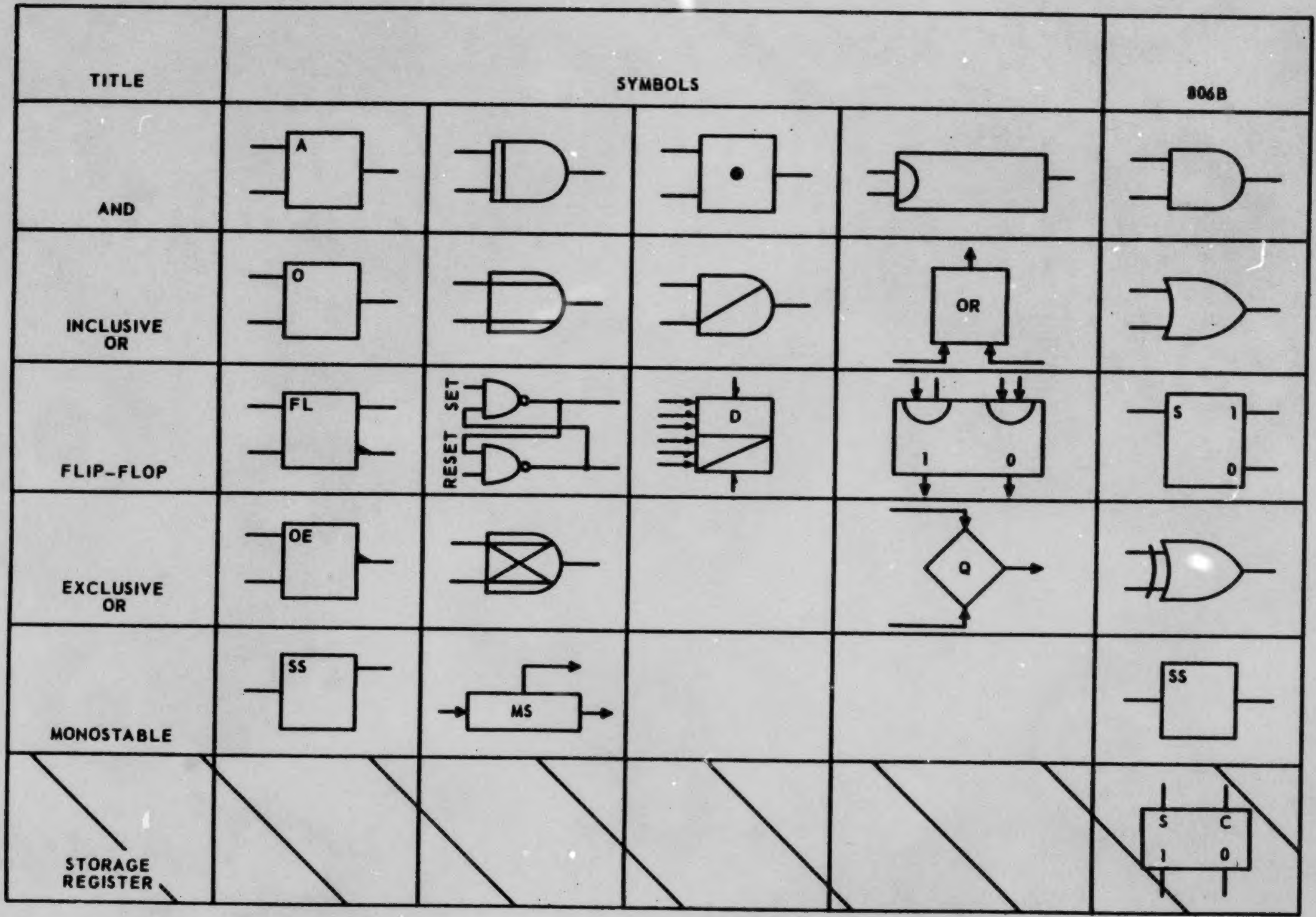

TITLE
SYMBOLS
806B
AND
A
INCLUSIVE OR
O
OR
FLIP-FLOP
FL
SET
RESET
D
1
0
S
1
0
EXCLUSIVE OR
OE
Q
MONOSTABLE
SS
MS
SS
STORAGE REGISTER
S
C
1
0

Figure 97. Logic symbols.

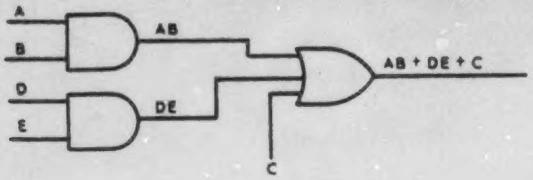


Figure 98. Logic OR function.

fundamental ideas encompassing logical conditions and operations. Logical conditions are called *variables*, and they are *represented by letters*. Logical operations are called *functions*, and they are *represented by symbols*. When a variable is used in a normal algebraic formula, it is assumed that the variable may take any numerical value. For example, in the equation "3A plus 6B equals C," the A, B, and C may range through the entire field of numbers. However, the variables used in boolean equations have a unique characteristic in that they may only assume one of two possible values, *high* or *low*, and these in turn may be represented by a *true* or *false* condition. For review purposes, let's consider the development of a boolean equation for the circuits shown in figure 98, and figure 99 (printed in the workbook). Figure 98 illustrates two AND gates feeding an OR gate, thus becoming an overall OR function. Note the lack of signs of grouping within the final equation. Figure 99 (printed in the workbook) shows two OR gates feeding an AND gate, thus becoming an overall AND function. In this case, signs of grouping (as shown in fig. 99) are used to retain circuit integrity. In developing the boolean equations for each of the figures, we start at the input and work toward the output. This is a good rule to remember, especially when you attempt to develop a boolean equation during a troubleshooting period. Based on your previous technical school training, the boolean equations just developed shouldn't have seemed all that difficult to you. What about developing a boolean equation for a circuit such as the one presented in figure 100 (printed in the workbook)? Could you do it? To enable you to do so, the next paragraph explains how to develop this equation.

18-5. The circuit that you see in figure 100 is a stepping circuit used to develop output pulses that in turn step a counter. In analyzing this circuit, a determination as to the output's origin and its duration must be made. As stated earlier, a boolean equation is developed from the input to the output. Therefore, we will develop the boolean equation by beginning at AND gate J44-13. J44 develops an output at pin 13 for its input signals $\overline{\text{Alert Message}}$ · (· indicates *and*) OPE OTH TX (output parity error signal from the other transmitter). Note the line above the signal "Alert Message." It is called the *vinculum*, and it indicates the *absence* of the signal Alert Message. OR gate J5-18 provides TFGOO + (+ indicates *or*) TFG35; observe that this expression is fed to inverter J5-28 which NOTS (inverts) the expression, thus providing $\overline{\text{TFGOO}}$ · $\overline{\text{TFG35}}$ (TFG stands for timing format generator) at pin J5-21. At J5-19, the signal ($\overline{\text{Alert Message}}$ · OPE OTH TX) + ($\overline{\text{TFGOO}}$ · $\overline{\text{TFG35}}$) is produced. This signal primes pin 24 of AND gate J3-22. J3-23 is primed by T6 (time 6 pulse), which produces an output at J3-22 as long as pin 24 is satisfied. The output of an AND gate is determined by the duration of its *shortest input*. In this particular stepping circuit, timing pulse T6 determines the duration of the output at J3-22. This time duration is 417 microseconds. The 417-microsecond output at J3-22 is written: ($\overline{\text{Alert Message}}$ · OPE OTH TX) + ($\overline{\text{TFGOO}}$ · $\overline{\text{TFG35}}$)T6. To complete the equation, we find at pin 24 of OR gate J5-22 a signal that, when present, replaces the entire equation thus far developed; this signal is EOD (end of data). The remainder of this stepping circuit consists of nothing more than an emitter follower and level restorer. Now, the output's origin and duration are known, as is the boolean equation for this stepping circuit. The complete boolean equation reads:

$$[(\overline{\text{Alert Message}} \cdot \text{OPE OTH TX}) + (\overline{\text{TFGOO}} \cdot \overline{\text{TFG35}})\text{T6}] + \text{EOD}$$

18-6. Now that the boolean equation for the stepping circuit is completed, let's determine its effectiveness in troubleshooting. For example, to determine that the stepping circuit is functioning properly, an oscilloscope would be used to check TP J77-H for a pulse that is 417 microseconds in duration. If this pulse is not present, the next logical step would be to check TP J77-F and eliminate the possibility of the emitter follower (EFP J5) and level restorer (LR J5) being defective. Should the pulse be present at TP J77-F and not present at TP J77-H, card J5 would be changed. However, if the pulse isn't present at J77-F, the boolean expression must be analyzed to determine which logical function provides the normal stepping pulses. The first portion of the equation ($\overline{\text{Alert Message}}$ · OPE

OTH TX) can be eliminated because it is an error condition that normally isn't present. Another stepping condition is EOD, which occurs only at the end of a transmission or the reception of a message. At this point in analyzing this boolean equation, it becomes apparent that the normal stepping pulses are provided when the format generator *is not* at TFGOO and TFG35. The troubleshooting approach at this point would be concentrated on the function $(\overline{TFGOO} \cdot \overline{TFG35})T6$. A check would be made at the timing pulse generator for T6 pulses. If T6 pulses are being generated, a check of TP J76-B would be made to determine the *absence* of TFGOO and TFG35. The *absence* of TFGOO and TFG35 at TP J76-B would indicate that the problem circuitry is between TP J76-B and TP J77-F (in other words, the timing frequency generator should be functioning properly). At this point, cards J3 and J5 would be replaced.

18-7. *Developing truth tables.* Another means of troubleshooting by use of the boolean equation is to disregard the full equation and develop what is known as a truth table. A table of this nature is nothing more than a means of determining an output by considering all inputs and their variables. In figure 101 (printed in the workbook), a truth table has been developed for the output of a very common computer circuit—the full adder. The circuit inputs consist of X, Y (the addends), and C (a carry input from a previous stage). The outputs are represented by S (the sum) and Co (the carry out). Look over this truth table carefully and note the binary inputs and outputs. What is happening in lines 1 through 8? Binary math? That's part of it. Something else is there—something very important to a truth table. Remember the definition of a truth table? That should give you the answer. A truth table is a means of determining an output by considering all inputs and their variables. For example, in line 1 of figure 101, 0 + 0 + 0 = 0 with a carry of 0; in line 8, 1 + 1 + 1 = 1 with a carry of 1. Now, look at all the inputs between lines 1 and 8. Here are all the other variables possible for the inputs X, Y, and C. This answers the question of what is happening in lines 1 through 8 of the truth table. A determination of the output from a full adder circuit is being made by considering all its inputs and their variables. Now the big question is, "How can a truth table help you in your troubleshooting efforts?"

18-8. When troubleshooting, the true value of a truth table is its identification of all input variables along with their outputs. The easiest way for you to see this is by setting up a hypothetical troubleshooting problem. Let's suppose a failure occurs within your computer system X, and the failing card (the full adder circuit in fig. 101) is identified and replaced. While we are supposing, let's go further and involve you. That's right, you are the repairman assigned to perform the bench check. First you read over the failure document. It reads: "Card failed during diagnostic program routines of the ADD class instruction." Not much to go on, is it? You look over the logic diagram and develop a truth table (fig. 101). Systematically you set up your tester to provide the inputs identified in each line (1 through 8) of the truth table. After setting up each test, you check TP-H (test point H) and TP-M for the output indicated by the truth table. Let's further suppose that each output checks until line 8; here you find no output at TP-M. Now you perform the following checks and get the results indicated:

- TP-G - Output OK.
- TP-L - No output.
- TP-J - No output.
- TP-E - Output OK.
- TP-C - Output OK.

18-9. From the results of the above checks, it is apparent that AND gate 6 is failing—i.e., with two good inputs (TP-E and TP-C) it produced an erroneous output at TP-J. Also, by starting at the output and checking each TP back to the input, the gates that were functioning properly were identified as well as the faulty gate. Now, you must admit that the truth table helped your troubleshooting effort. Actually, once we knew that only line 8 was failing, the contents of the truth table pointed to AND gate 6. What does this mean? For one thing, all the checks made after we found the failing variables (line 8) were not necessary.

18-10. You might be questioning the statement that indicated the contents of the truth table pointed to AND gate 6 once line 8 was identified as failing. Let's analyze that statement to determine its validity. The only time an error occurred was during the addition of 1 and 1 with a carry-in of 1. Looking at the logic, it becomes apparent that the only gate affecting the sum (S) output, when adding the inputs of line 8, is AND gate 6. This is true because its upper leg is conditioned by the carry input, and its lower leg is conditioned by the ANDed function of X · Y from AND gate 2. Also, you must keep in mind that the tests (lines 1 through 7) performed before line 8 were successful.

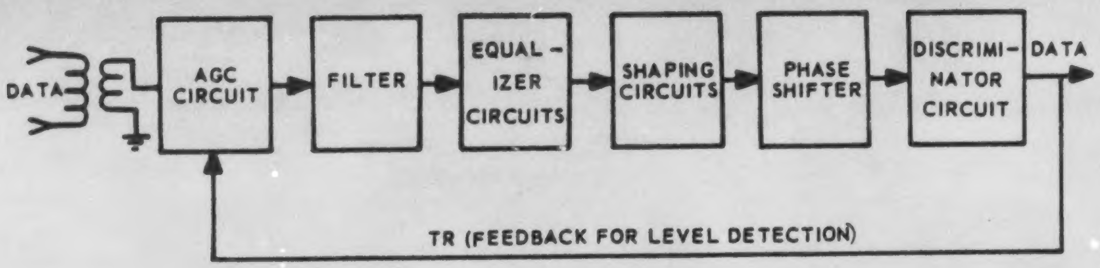


Figure 102. Demodulator unit block diagram.

18-11. Before leaving our hypothetical troubleshooting problem, let's regress to when you were looking at the card's failure document. Suppose the repairman who ran the diagnostic program identified (on the failure document) that the failing program routine was attempting to add 1 and 1 with a carry-in of 1. Just think how much easier it would have been for you to bench check the card with this information on the failure document. The repairman who prepared the document could have acquired this exact failure information by consulting the diagnostic program writeup. Now when you hear your supervisor say, "Put *all* the failure data on the failure documents," you will know why it is needed.

18-12. **Troubleshooting with Logic Analysis.** A fine line is drawn between troubleshooting with boolean equations and logic analysis. First, you devise your boolean equation and then you use it in your testing to determine if each function is present. It is during this testing and application of your boolean equation that logic analysis takes place.

18-13. *Functional area approach.* The primary purpose of the equipment in electronic computer systems is the processing of data. This is done through a logical flow of data which, in turn, is accomplished through the functioning of the equipment's circuitry. The basic functions of these circuits, exclusive of power supplies, is the generation, transmission, conversion, logical manipulation, and storage of signal voltages. When the system fails in performing any one of these functions, the cause must be found before the repair can be made. This means you must troubleshoot the system in an effort to isolate the fault to the failing functional area and then to the failing component within this functional area. The logical method of isolating a fault is through a process of elimination of the functional areas that are performing properly. This is usually done by careful analysis of the malfunction's symptoms. The effectiveness of this analysis depends upon your knowledge of the functional operation and data flow within the computer system. Once a failure is isolated to a specific functional area, further analysis of the circuitry within this area is required to isolate the malfunction to the failing component. Another name for this functional area approach is the block diagram approach to troubleshooting.

18-14. For an example of the block diagram approach to troubleshooting, refer to figure 102. Here we have a block diagram of a demodulator unit. Let's suppose that its output is absent and you are attempting to isolate the failing function—i.e., AGC, filter, etc. What approach would you take in troubleshooting this demodulator? Look over the following steps and compare them to the troubleshooting approach you would use:

(1) Check for the presence of the data input to the AGC circuit.

(2) Check the data output of the equalizer circuit. The results of this check will isolate the failure to the first or second half of the circuits in the demodulator.

(3) The first half of the circuits (i.e., the AGC, filter, and equalizer functions) would be suspect if *no data appeared* at the output of the equalizer. By checking the input and output of these first three blocks, you should be able to isolate the failure to one of them.

(4) The second half of the circuits (i.e., the shaping, phase shifter, and discriminator functions) would be suspect if *data appeared* at the output of the equalizer. By checking the input and output of these three blocks, you should be able to isolate the failure to one of them.

18-15. The method of troubleshooting explained above is sometimes called the *split-half* method—i.e., once you determine the absence of an output, you split the circuits in half and check for an output at the half-way point. When you determine that the failing circuit is in the first or second half, you split these circuits in half for further isolation of the failure. This process is continued until the failure is isolated to one function. This split-half method could also be continued once you begin troubleshooting the circuits in the failing functional area.

18-16. *Signal injection approach.* This method of logic analysis consists of inducing a normal signal (or a signal similar to that which is present under normal operating conditions) to the input of the circuits in question. The circuit conditions which result from this application are then checked at various points, using test instruments such as a vacuum-tube voltmeter, oscilloscope, or any other device which is appropriate for use as a signal indicator. By using these test instruments and injecting a signal into the circuits, you can monitor circuit operation at various stages, and localize the points of origin of such faults as distortion and hum, noise oscillation, or any other abnormal conditions. When this method of logic analysis troubleshooting has revealed a faulty stage, you can further check that stage by making voltage or resistance measurements, or by individually testing circuit components. A logical procedure along these lines is to first test those components that are easiest to check and that *experience* has shown to be the most troublesome. If a vacuum tube or transistor is involved, it is usually checked first or, in the case of vacuum tubes, one known to be good is substituted in its place. In most cases, a schematic and/or logic diagram is all that is necessary to determine where to insert the signal and where to check for its presence. In other cases, voltage charts or illustrations of waveforms may be needed for comparison purposes. However, in most of the cases involving logic analysis troubleshooting through signal injection, the important things to remember are these:

- Narrow the trouble down as far as possible by analysis of the symptoms.
- Use your schematic diagrams and logics.
- Check waveforms and voltages before checking resistances (resistance checks require the power off).
- Think the problem through before replacing components.

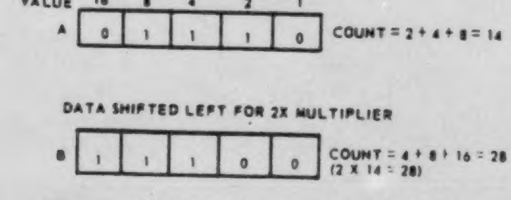


Figure 103. Left shift (times 2 multiplier).

- Check the records. Do not overlook the importance of your fellow workers' previous experience. They may have experienced the same trouble.

18-17. Troubleshooting with boolean algebra and logic analysis is a must in most electronic computer systems. Your ability in using these two methods of troubleshooting increases as you gain experience on the job, and as you become proficient in analyzing waveforms and patterns and signal tracing with an oscilloscope.

19. Analyze Patterns and Waveforms

19-1. In this section, the objective is to learn how to analyze patterns and waveforms as seen on an oscilloscope, and to use this analysis when troubleshooting. As stated in the introduction to this chapter, this is one of the specific techniques in troubleshooting. The analysis of this task exposes the many different types of digital data patterns and analog waveform presentations you may observe on an oscilloscope during your career in the electronics environment.

19-2. **Purpose of Measuring Patterns and Waveforms.** Two specific reasons for measuring patterns and waveforms are evident. The first is to analyze data content and the second is to determine if a waveform meets the prescribed specifications.

19-3. *Analyzing data content.* The digital data content in the variety of systems now being used and maintained is extremely varied. However, it generally has one common element—it is digital. This means that within a prescribed duty cycle one pulse, or its absence, represents a bit; a group of pulses represents a data word, a byte (a group of binary digits usually operated upon as a unit), or another form of intelligence. Digital data consists of information that is routed, altered, stored, processed, controlled, and displayed by the computer system. Digital data also generates visual intelligence in the form of printouts, displays, mechanical readouts, and automatic functions of console units. In addition to providing the substance for the program to operate, digital data (converted from punch cards or other inputs) controls program sequencing which, in turn, controls the actions of the computer.

19-4. *Determining prescribed specifications.* The data content we have been talking about thus far is digital; therefore, it is in informational pulse form, either voltage or current, representing a language called *binary.* From your studies in tech school, you know that binary is a two-character (1 and 0) language or number system. Now let's con-

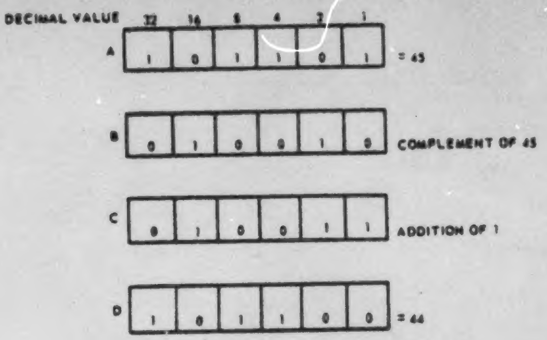


Figure 104. Binary subtraction.

sider this data as containing intelligence indicating the number of aircraft (flight size), and that the total number of positions allowed in a word for storing this data is three. This would mean that low numbers of aircraft in a formation may be cataloged individually and high numbers may be grouped under specific numerical headings. For example:

- For a flight size of 1 to 4 aircraft, the binary count would be equal to its respective count—i.e., 1 aircraft = 001, 2 aircraft = 010, etc.
- For a flight size of 5 to 7 aircraft, the binary count would be equal to 5 (101).
- For a flight size of 8 to 12 aircraft, the binary count would be equal to 6 (110).
- For any flight size consisting of more than 12 aircraft, the binary count would be equal to 7 (111).

By the arrangements shown in this example, it follows that digital data expressed in binary can be interpreted to mean specific information. More significantly, it can be processed, altered, updated, and used in a very simple and accurate form in an electronic computer system.

19-5. We also know that digital data is manipulated in parallel and serial form; that it is speeded up, slowed down, shifted, erased, and generated as the requirements dictate. For instance, if a requirement exists to multiply a number by two, a simple machine operation could perform this action. This operation is a left shift. Notice the two examples in figure 103. A of the figure shows a five-stage counter with a count of 14 in it. By applying a left-shift pulse to the counter, the data bits are moved one position left. This action causes the value of each bit to double, and now the count, as indicated at B of the figure, equals 28.

19-6. Data can also be manipulated by division of binary. Using figure 103 again, suppose a right-shift pulse were applied to the counter with the count inserted as shown at A of the figure. What count would result? If you answered 7 (00111), you would be absolutely correct. In other words, the original contents of the counter have been divided by 2.

19-7. We can also manipulate the digital count by either addition or subtraction. Using the same figure again, let's add 2 bits serially, one at a time, to the LSD of the counter. Enter the first bit of data into the LSD at A of the figure and, since the LSD contains a zero, the counter causes a one to be stored in its place. Enter the second bit of data into the LSD and, since the LSD, two, four, and eight stage now contain a one, the counter causes a one to be stored in the 16 stage and a zero in each previous stage (i.e., the LSD, two, four, and eight stage). What has occurred is that two binary bits have been added to the counter, and it has upcounted from its original count of 14 (01110) to a count of 16 (10000). A one can be subtracted from a binary counter by a complementing and adding process. Refer to figure 104 for this explanation. At A of the figure, you see the binary configuration for 45. B represents 45 in complement form. C represents the result of adding 1 to the complement (B) of 45. D represents the answer, 44, which is actually the complement of C.

19-8. In the previous paragraphs we discussed digital data as patterns containing intelligence. In the discussion that follows we must also include analog voltage and current waveforms that do not contain intelligence. Stating that analog waveforms do not contain intelligence may need further explanation. Digital data, as we have discussed, is readily interpreted into word data such as range of aircrafts, flight size, or computer instructions. Analog waveforms do not contain this translatable information. However, each waveform is, in itself, capable of transmitting an image to the human brain and causing a specific reaction. For instance, consider a console using *time sharing* for its display cycle—

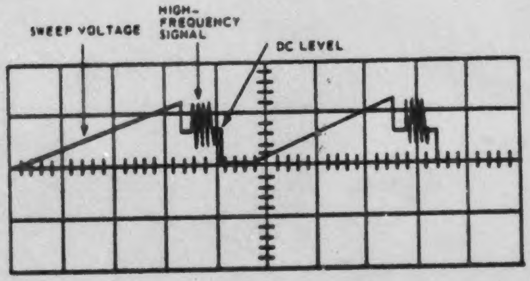


Figure 105. Time sharing.

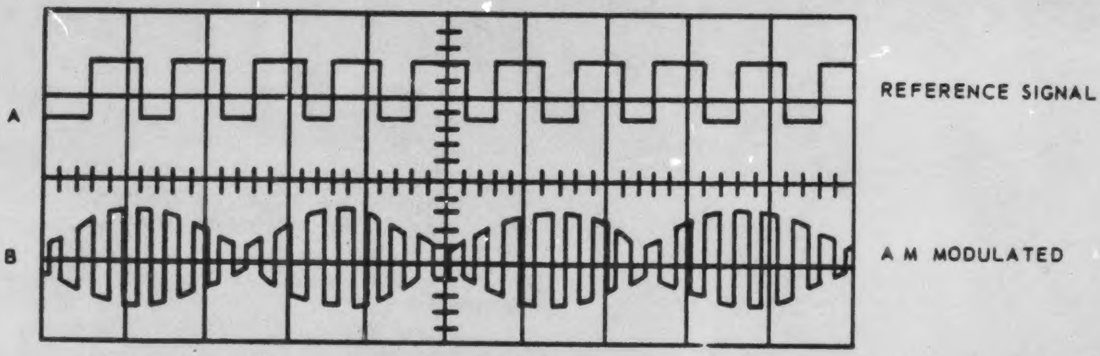


Figure 106. Reference signal compare.

where the first part of the display is a sweep voltage and the second part is a DC level with some high-frequency signal riding on it as shown in figure 105. The image displayed is converted by the human mind into the functional operation of the circuits involved in providing the sweep voltage, DC level, and high-frequency signal. Therefore, if any portion of the waveform is distorted or missing, that portion should convey a message to the repairman. What message? Well, if the sweep voltage were distorted, the logical circuit to suspect first would be the sweep generator.

19-9. If a display as seen on the scope reflects a high- or low-basic frequency, then the examination of the waveform requires use of the scope controls to verify the frequency accuracy. This is most often done by measuring the time of one cycle and then applying the formula, Frequency $= \frac{1}{\text{Time}}$. On the other hand, if a display is known to contain either *amplitude-* or *frequency-modulated* data, single pulse examination would not reveal any significant information other than information that would facilitate the measurement of the carrier frequency. Examination of *multiple cycles* reveals that data is, or is not, being received. For instance, in figure 106, A, a basic reference signal without any data is depicted. All cycles are the same pulse width and amplitude. Now insert *amplitude-modulated data* onto the basic reference frequency and *increase the number of cycles per centimeter* on the scope, and the waveform would appear as it does at B of the figure. If the signal carrier were *frequency modulated*, the signal as seen on the scope would show *no change in amplitude* as it did with amplitude modulation. However, it would show considerable change in frequency since *frequency modulation requires the algebraic summation of the data and carrier frequency*. It should be apparent, then, that knowing what effect amplitude and frequency modulation have on the carrier frequency is an aid when analyzing waveforms as a troubleshooting technique.

19-10. **Reading Techniques for Digital Data Patterns.** With the purposes of measuring data foremost in mind, let's consider the next element of the task in analyzing patterns and waveforms, i.e., "reading the data."

19-11. Oscilloscope displays provide for a left-to-right sweep presentation of digital

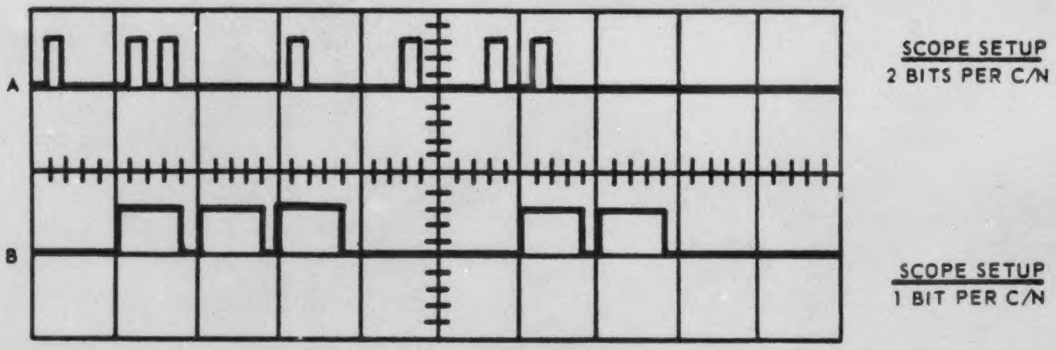


Figure 107. Digital display.

data. Therefore, when scoping serial input data with the LSD as the first input, it will appear on the left of the scope. Look at examples A and B of figure 107. Each word generated by a system that uses positive logic, although consisting of a different number of digits, shows its data starting on the left. For our discussion, assume that A of figure 107 depicts a 16-bit serial input word (LSD at the left) with 2 bits per centimeter. The data content of this display shows a binary configuration of 1011001001011000. Since the word is 16 bits long and there are just 2 bits per centimeter, only the first 8 centimeters are considered. Let's further assume that the first 13 bits (i.e., 1011001001011) represent radar range. The LSD is equal to 1/4 mile, and the MSD (bit 12) is equal to 512 miles. The sign bit (bit 13) indicates which direction, east or west (0 = east and 1 = west), the target is from the radar site. The maximum range that could be represented by the range bits (bits 1 through 12) is 1023¾ miles. The data as shown indicates an aircraft with a range of 364½ miles west of the site. For our example, this range is computed by totaling the decimal values represented by each binary 1, and since the sign bit is a 1 (indicating negative), this total range value is subtracted for the maximum range. In our example, the total range value computes to 659¼ miles; subtracting this from the maximum range of 1023¾ results in an actual range of 364½ miles. If the sign bit had been 0, the actual range would have been computed by totaling the decimal values represented by each binary 1; this computes to 659¼ miles.

19-12. In example B of figure 107, the data displayed is a Fieldata code consisting of 8 positions—1 bit per centimeter. The first 6 bits of this particular Fieldata code are used to represent an alpha or numeric character. Bit position seven of the code indicates whether the character is alpha or numeric—i.e., 1 = alpha and 0 = numeric. Bit position eight is the parity bit; *odd parity* is used. From the listing below, identify the alpha or numeric character represented in binary form using the reading technique of LSD on the left and MSD on the right:

Bit Position —	1	2	3	4	5	6	7	8		
	0	0	1	1	0	0	1	0	=	G
	1	0	1	1	0	0	1	1	=	H
	0	1	1	1	0	0	1	1	=	I
	1	1	1	1	0	0	1	0	=	J
	0	1	1	0	0	0	0	1	=	6
	1	0	0	1	0	0	0	1	=	9

The correct answer is alpha character I. Notice how each alpha character is assigned a binary code that is one value higher than the previous; i.e., G = 12, H = 13, I = 14, and J = 15, etc. Once again the reading technique was from the left of the scope to the right. By now you might be asking yourself, "How do you always obtain the LSD of a word in the first centimeter of the scope display?"

19-13. Oscilloscope synchronization plays an important role in reading a data display. It provides the basis for selection of a sweep start time coincident with the first bit of a data word or any other selected bit. By selection of a timing reference signal and use of external horizontal sweep (as previously explained in Chapter 4 of Volume 1 on test equipment), the LSD bit is placed in the first centimeter of the scope.

19-14. **Reading Techniques for Analog Waveforms.** Analog waveforms are usually easier to acquire and interpret than digital patterns. This is so primarily because analog waveforms are presented more frequently with less alteration. Primary techniques in reading analog waveforms require extensive knowledge in the use of the oscilloscope. For example, you'll need to be knowledgeable in the

- Synchronization of the scope.
- Use of the DC and AC voltage selection on the vertical preamplifier.
- Proper selection of sweep speeds.

19-15. To successfully read a waveform, knowledge and understanding of its generation make the job easier. But in the actual reading of the waveform you must be able to measure its AC and/or DC level, and understand that the DC level of an AC sine wave is its midpoint and is normally equal to zero volt DC. However, any AC waveform may be caused to ride a DC potential other than zero volt. When this occurs, use the DC switch and volts-per-centimeter control on the scope's vertical preamplifier to determine and validate the accuracy of your reading.

19-16. The average DC level of a square wave is normally zero volt DC; however, in a rectangular waveform, this average DC level is dependent upon which part of the alternation is above or below the zero-volt DC reference for the longer period. Figure 108 shows examples of the average DC level within rectangular waveforms. Notice in detail A of the figure that the positive portion is longer in duration when compared with the negative portion. This leads to an average DC level at a point above the zero-volt DC reference. Now notice that in the B section, the situation is reversed (i.e., the negative portion of the waveform is longer in duration than the

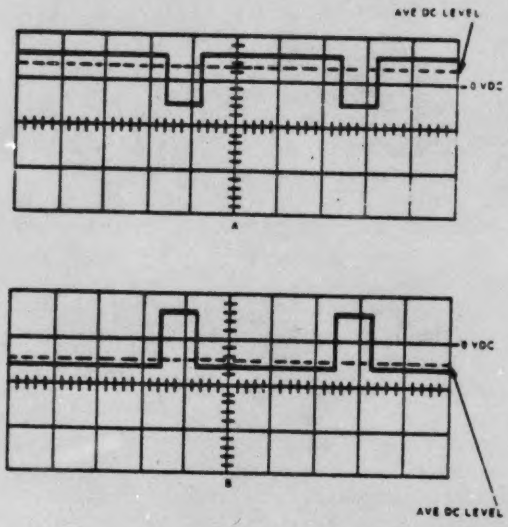


Figure 108. Average DC level compare.

positive) and the average DC level is below the zero-volt DC reference. These waveforms ~~show~~ examples of amplifier or other circuit outputs which allow signals to be displayed without clamping to a baseline. However, if the circuit generating these waveforms is designed for zero-volt DC clamping and the average DC level is other than zero volt, you know that a circuit defect exists. Before continuing with the development of our objective in this section, let's examine a few figures of various patterns and waveforms and determine whether they are or are not correct.

19-17. **Interpreting Patterns or Waveforms.** We have provided four figures for your interpretation. Preceding each figure you will find a description of what the scope presentation represents. Your job is to read and interpret the description, study the scope presentation, and determine whether it is correct or not. If the presentation is incorrect, write the reason that it is incorrect in the space provided.

19-18. *Problem 1:* A radar return from a height finder has been converted into digital form and stored. Flight plans for the particular aircraft specify its altitude at 10,500 feet. The storage space allowed for height within the data word is the first 9 bits of a 16-bit word. The LSD of height is equal to 375 feet. An ordinary binary counter is used to accumulate this height data. Now refer to figure 109 and determine if its oscilloscope presentation depicts the description given. Your answer:

19-19. *Problem 2:* While performing a bench check of a keyboard, the letter K was depressed and the configuration displayed on the scope was as shown in figure 110. For this problem, determine what the correct bit configuration is for the letter K by referring back to the page (in this section) that presented the bit configurations for letters G through J. Your answer:

19-20. *Problem 3:* A display cycle of a particular CRT is developed from a range of 0 to 210 miles. An unblanking/intensity pulse (provided by the unblanking/intensity generator shown in section A of fig. 111) provides this display cycle by unblanking the CRT. The two elements controlling the generator are shown in parts A and B of section B in the figure. They are system trigger and AGL (automatic gate length) trigger. System trigger occurs at range zero, and AGL trigger occurs after it (at 210 miles). For this problem you are to determine if the unblanking/intensity

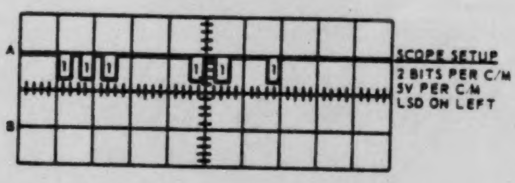


Figure 109. Data pattern (height).

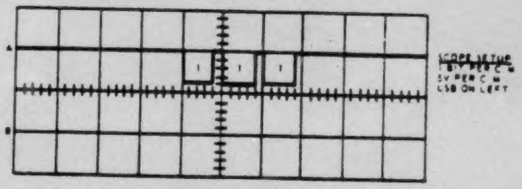


Figure 110. Letter data pattern.

generator output (shown in section C of fig. 111) is correct or not. System trigger amplitude is +35 volts (±10 volts) and AGL trigger amplitude is +15 volts (±2 volts). The output amplitude from the unblanking/intensity generator is 18 volts. CRT unblanking occurs from system trigger to AGL trigger, and blanking occurs from AGL trigger to system trigger. Based on these specifications, you are to determine if the unblanking/intensity generator output (as shown in section C of fig. 111) is correct. Your answer:

19-21. *Problem 4:* The waveform shown in figure 112 represents the output of an integrator circuit. The parameters for the standard are shown in section A of this figure. Compare these with the waveform displayed in section B and record your findings in the space provided. Note that the pulse width is measured from the start of rise time to the 50-percent point of the fall time. Your answer:

19-22. *Answer to problem 1:* With a height flight plan specifying 10,500 feet, the proper binary configuration for the data word would appear as follows:

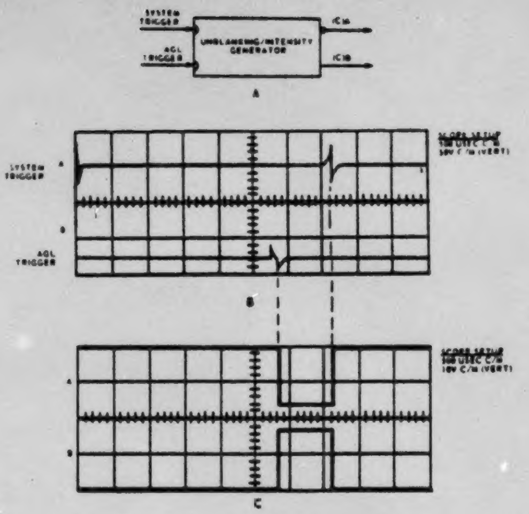


Figure 111. CRT blanking and unblanking.

The other bits in positions 12, 13, and 16 of figure 109 represent another element of data about the same aircraft, but not height.

19-23. *Answer to problem 2:* The display as seen in figure 110 is incorrect. The letter K has a binary value that is equal to 16 decimal. The character is alpha so bit 7 is a 1, and parity bit (bit position 8) should be a 1, indicating odd parity. However, the display indicates bit 6 was picked (instead of 0) resulting in the parity bit, showing up as a 0.

19-24. *Answer to problem 3:* The waveforms are correct. System trigger turns on the unblanking/intesity generator. At turn-on time output B (fig. 110, C) goes low; this low is used to gate the data to be displayed to the CRT. The unblanking pulse, A, goes high at turn-on time and brings the CRT out of cutoff. At AGL trigger time (210 miles after system trigger) the generator output is switched, thus ending the display cycle.

19-25. *Answer to problem 4:* The integrator output waveform does not meet specifications. Its amplitude exceeds the maximum of 4.3V. Its baseline is good. The pulse width exceeds the maximum limits of 3.7 microseconds. Its fall time is within the specifications.

19-26. With the solutions to the four problems given, our study of patterns and waveforms is concluded. The study you made

$\overline{375}$	$\overline{750}$	1500	3000	6000	$\overline{12000}$	$\overline{24000}$	$\overline{48000}$	$\overline{96000}$	= 10,500 feet
0	0	1	1	1	0	0	0	0	
LSD								MSD	

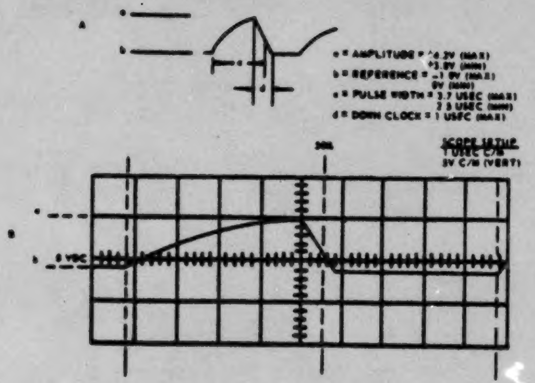

a
b
a = AMPLITUDE = +4.2V (MAX)
+3.8V (MIN)
b = REFERENCE = -1.0V (MAX)
0V (MIN)
c = PULSE WIDTH = 3.7 USEC (MAX)
2.3 USEC (MIN)
d = DOWN CLOCK = 1 USEC (MAX)
SCOPE SETUP
1 USEC C/M
5V C/M (VERT)
0 VDC

Figure 112. Integrator circuit output.

in the section on logic analysis, coupled with this one, provides you with the tools to proceed with troubleshooting tasks.

20. Signal Tracing Techniques

20-1. As the saying goes, "Let's get it all together." Let's get it all together by combining the techniques of analyzing logic, patterns, and waveforms into the technique of signal tracing. This will be done by troubleshooting a typical computer malfunction. Since you are working in a computer system environment, the chances are that you have some type of memory unit. As you know, every memory has a control unit. For our troubleshooting problem, a memory that is used to store and validate input data has been selected. The block diagram for this memory is shown in figure 113 (printed in the workbook).

20-2. **Analyze Block Diagrams.** As you can see in figure 113, the memory consists of the following:

- Input unit with converter.
- Memory control unit.
- Core memory unit.
- Error detector and lamp.

Using our figure, we can now set the scene for our malfunction. As data came in the error light went on, but by using the reset switch, the error light went out. This error light didn't come on again until later in the day. This indicates an intermittent error condition. As we stated earlier, intermittent error troubleshooting can cause a person to become quite frustrated. However, before this intermittent error turns into a solid error condition, there is a certain amount of *before the fact troubleshooting* that you can accomplish. As a matter of fact, this is where you can really make money.

20-3. In the discussion that follows, correlate the letters in parentheses with those in the block diagram. The *load level* (a) conditions the memory control unit and error detector for 1 millisecond. This is the time required to validate and store an input character into a memory address. *Data* (b) is loaded into the buffer register with a *transfer pulse* (c). The memory address to be written into is cleared with a *read pulse* (d), and data is then written into that address from the buffer with a *write pulse* (e). The buffer is reset with a *reset pulse* (f) which is developed from the *unload pulse* (g). The buffer is then loaded with data (the same data just written into core) from core by a *strobe pulse* (h) which is also developed by the unload pulse. The same memory address is cleared again with a read pulse, and the data is written back into it. The *delay load pulse* (j) which occurs 93 microseconds into the load cycle is used along with the load level for the actual detection of errors. If validation occurs on a bit-by-bit check, the error light remains off.

20-4. **Analyze Probable Trouble Areas.** The block diagram shows four distinct areas where error could occur and give an error indication:

- Buffer register.
- Core.
- Comparator/error detector.
- Control unit.

20-5. *Buffer register.* If a stage of the buffer is failing, proper comparison cannot take place. Also, a faulty control signal feeding the buffer (i.e., reset, transfer, or strobe) will result in a failure indication.

20-6. *Core unit.* A defective core is possibly, but highly unlikely. Cores seldom fail, but don't rule out the possibility of failure altogether. More likely, though, one of the control signals that affect the condition of the core (i.e., read, write, and inhibit) is defective.

20-7. *Comparator/error detector.* A defective leg of a comparator circuit could cause an error indication. Also, the error light control circuit could be defective, causing the error light to turn on.

20-8. *Control unit.* If any one of the pulses feeding or generated by the control unit becomes defective, the operation is impeded and an error indication occurs. Considering the fact that this unit receives, generates, and distributes the pulses that directly affect the core, wouldn't you say that it would be a primary suspect when the error light came on?

20-9. **Priority Order of Failure Probability.** A definite priority (indicated as follows) is apparent when certain characteristics of the four areas listed above are considered.

- Memory control unit.
- Buffer or comparator.
- Core.

20-10. *Memory control unit.* This unit contains six pulse generators: transfer, reset, write, read, inhibit, and strobe. Generators are likely places to suspect a failure because they usually have extensive circuits. If one fails, the signal may be lost, differentiated, or distorted.

20-11. *Buffer or comparator.* Both of these units present equal possibilities for failure. A buffer usually contains a bistable device made up of more than one stage that is vulnerable to failure. If the multiple input gates to these units employ diodes, you can place these diodes high on your list of probable failures when an error occurs. In comparators, AND, OR, EXCLUSIVE OR, FLIP/FLOPS, or other comparison devices are used. Frequently the transistors or diodes used in comparators open or short between their junctions. Also, a possibility for error exists when a F/F, setting to the *one* state, is used to provide the ground for the error lamp. A relay may also provide this ground to the lamp. Either type of switching without proper control could cause the error light to come on.

20-12. *Cores.* As a rule, cores do not break down and fail. However, the wiring of the cores (for addressing, inhibiting, and sensing) may short or open. More Often than not, the current driver circuits fail in a memory unit. These facts lead us to suspect that the cores themselves are least likely to cause a failure, and the current driver circuits are most likely to cause a failure.

20-13. **Selecting the Approach.** Using the priority order above, we see that no verification of the buffer, core, or comparator is possible without verification of control unit operation. Therefore, the analysis must proceed by examining the logic of the control unit.

20-14. *Determining the control signal.* These three considerations are to be made and determined from the analysis of the memory control unit logic:

- Width of the pulses.
- Polarity of the signals.
- Sequence of operation for load and unload.

20-15. Figure 114 (printed as a foldout in the workbook) includes a logic diagram of the control unit and timing charts for the load and unload sequence. As we continue to signal trace through the techniques of logic, patterns, and waveform analysis, we should begin to determine which signals must be verified first, second, third, etc. At the same time, a listing of the boards involved in the entire unit should be acquired or made. Along the side of each board identified, analysis notes should be made that include conditions which might suggest changing it. Let's analyze each of the signals:

TRANSFER SIGNAL

NOTES:

1. Pulse width: 4 microseconds.
2. Card A14, monostable multivibrator.
3. Card A12, inverter amplifier.

REMARKS:

1. Transfer pulse begins at the end of load pulse and continues for 4 microseconds.
2. *Load* must be present before transfer occurs.
3. Results if *transfer* does not generate, but *load* is present:
   a. Error light will turn on.
   b. Data will not be gated into buffer; therefore, memory loads all zeroes because the *reset* ~~cleared the buffer.~~

RESET SIGNAL

NOTES:

1. Pulse width: 4 microseconds starting with *load* or *unload.*
2. Card A14, monostable section and inverter section.
3. Card A11, OR gate one leg, and inverter section.
4. Card A13, monostable multivibrator section and inverter section.

REMARKS:

1. *Reset* pulse begins with *load* and ends at beginning of *transfer.* Results if reset does not generate:
   a. Error light will turn on.
   b. Data loaded into buffer will combine with previously loaded data.
   c. Core memory will load invalid data from buffer and comparison of data in the error detector unit results in error correlation.

READ SIGNAL

NOTES:

1. Pulse width: 4 microseconds starting and ending with *transfer pulse.*
2. Card A11, differentiator section.
3. Card A12, OR gate (one leg).
4. Card A13, monostable multivibrator.
5. Card A9, current driver.

REMARKS:

1. *Read* signal is converted to a current pulse which causes all the cores to reset

to the Zero state.

2. Read controls the generation of *write* and *inhibit*.
3. Results if read is not generated:
   - *a.* Memory will not clear.
   - *b.* *Write* and *inhibit* will not be generated.
   - *c.* Data stored in buffer cannot be loaded into core.
   - *d.* Error light will come on because core data and input data do not correlate.

WRITE SIGNAL

NOTES:

1. *Write delay* pulse width: 4 microseconds (starting at the end of *read*).
2. Write pulse width: 4 microseconds (starting with the end of write delay).
3. Card A10, two sections of monostable multivibrator are used.
4. Card A9, current driver section.

REMARKS:

1. *Write* signal is converted into a current pulse used to load the data.
2. Results if write or write delay generators malfunction:
   - *a.* Memory cores will always be zero; *read* will reset them.
   - *b.* Correlation will be improper because on the *unload* (rewrite) cycle, data stored in buffer and loaded in memory will zero.
   - *c.* Error light will come on.

INHIBIT SIGNAL

NOTES:

1. *Inhibit* pulse width: 9 microseconds.
2. *Inhibit delay* pulse width: 2 microseconds.
3. Inhibit delay pulse starts at the end of *read*.
4. Card A11, 2 sections of monostable multivibrator and inverter are used.

REMARKS:

1. Inhibit signal restricts the buffer data (*zero* bits) from loading into cores because of its polarity.
2. Results if *inhibit* or *delay inhibit* generators malfunction:
   - *a.* Improper data load to core memory.
   - *b.* Possible switch of cores when data bits are zero in buffer.
   - *c.* Possible switch of all cores in memory because of write current.
   - *d.* No correlation in detector circuit, resulting in error light indication.

STROBE AND DELAY STROBE

NOTES:

1. *Delay strobe* pulse width: 1.5 microseconds.
2. *Strobe* pulse width: 0.4 microseconds.
3. Card A12, two sections of monostable multivibrator.
4. Card A10, inverter section.

REMARKS:

1. *Delay strobe* causes generation of strobe to occur during a *read* (memory reset) time. The strobe pulse transfers the memory core data through drivers back into input buffer storage.
2. Results if strobe is not generated:
   - *a.* Rewrite into core is incomplete.
   - *b.* Memory core unit will contain zero.
   - *c.* No correlation in detector circuit, resulting in error light indication.

20-16. *Analyzing the conditions.* If any unit, buffer, core, comparator, or control fails in any part of its circuits, the error circuit provides a visual sign. The primary reason for this is that input data is routed to the comparators for later use in the comparison cycle. Further analysis shows that any one control signal including *unload* also provides a visible error indication. However, the load signal not being present (even if data is to be stored) inhibits all memory action. This is true for two reasons: (1) without load no transfer or reset action can occur, therefore, the buffers cannot be cleared and loaded, and (2) without load, the error detector cannot sample the comparator output. With this logic and function analysis completed, and a set of notes similar to the items we listed above, predicting the failing component or assembly is possible.

20-17. *Isolating the malfunction.* In this hypothetical problem, an intermittent error was indicated. From the logic analysis, we understand that:

- Load must have been present.
- Correlation did not occur.

Unfortunately, no further positive prediction can be made. However, some probable hypotheses can be assumed:

- Core memory is good.
- Error detector circuit is good because manual reset extinguished the lamp.
- Buffer and comparator may have a faulty component.
- Most likely area to validate first is the *memory control unit.*

20-18. Validating the Memory Control Unit. Now comes the time for the use of the oscilloscope and physical signal tracing. Assume that each test point is available while the unit is in an operational configuration. By synchronizing the scope (preferably a memoscope) on load, each of the pulses generated by the memory control unit can be checked. Further, each pulse can be checked for pulse width and other relationships. Since the problem is intermittent, the complete absence of a pulse is unlikely. But, examining each pulse for its desired characteristics *may* provide a clue. Signal deterioration is often a prelude to signal failure.

20-19. If you find such a clue, write a note about it, draw its measured waveform, and

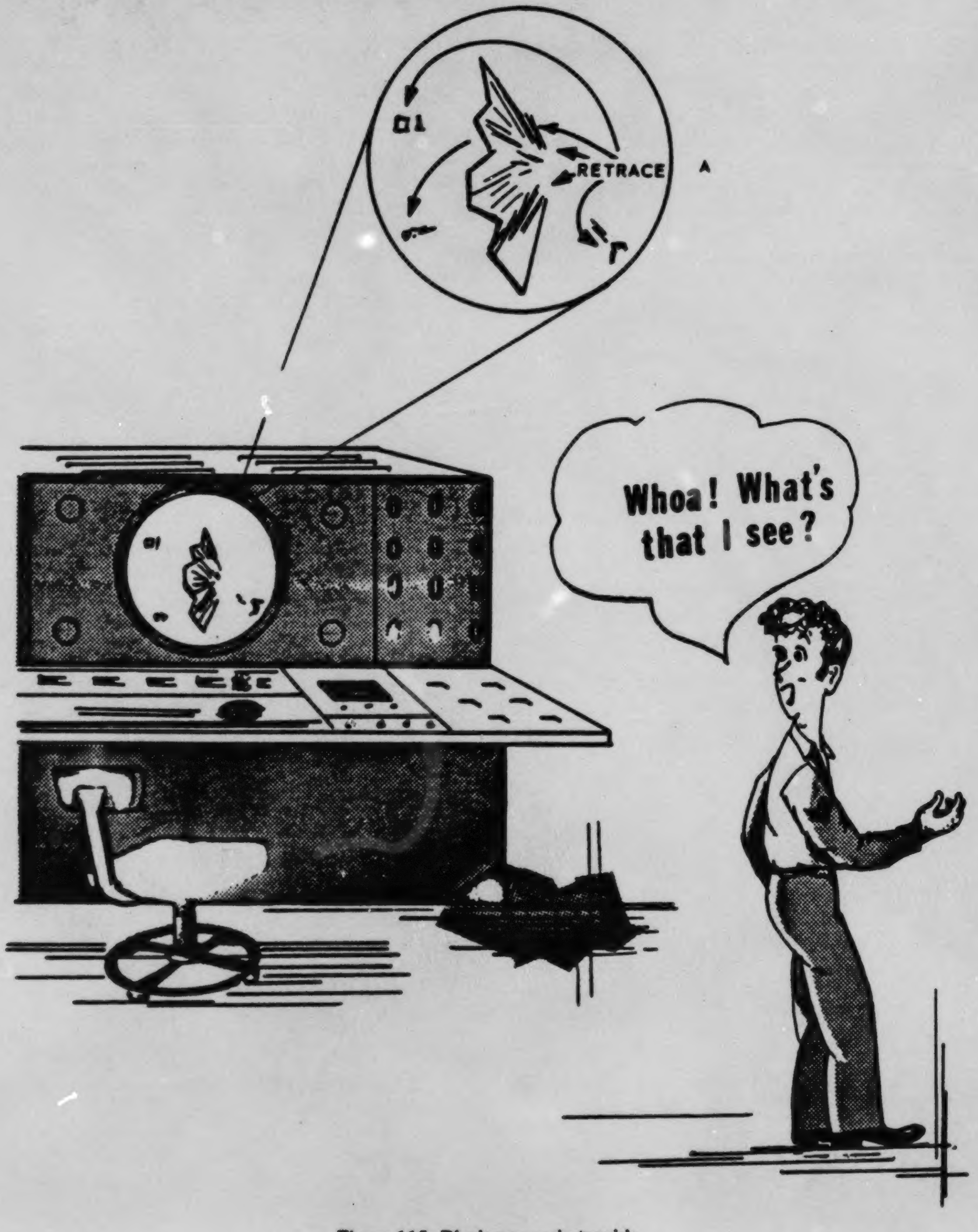

RETRACE
A
Whoa! What's that I see?

Figure 115. Display console trouble.

ask yourself, "Does the pulse width exceed its parameter? Does it have too short a pulse width? Is the pulse amplitude too low or too high? Is clamping or base reference voltage proper?" Ask any question that may lead you to develop an opinion or cause you to select a specific approach when the failure becomes *solid.* If you find the slightest clue, write it down and list the specific assemblies (PCB cards) involved. If you are proven right later, you will know just what cards to remove. If all signals look, measure, and recur as specified in the performance standard, begin the same procedure for the buffer, then the comparator, and finally, the sense amplifier and address control cards within the memory unit. As we stated earlier, do not discount the cores themselves as a possibility; just consider this possiblity as very unlikely.

20-20. The example just completed showed one instance in which the oscilloscope was used in troubleshooting. We could present numerous other examples of different parts of systems where the oscilloscope is used for signal tracing during troubleshooting periods. Rather than do that, let's develop some problems in certain areas of a computer system and determine when the oscilloscope should be used.

20-21. **When to Use the Oscilloscope.** If someone tells you that the scope will be used for every troubleshooting problem that is encountered, don't you believe it. Just because you get an error indication doesn't mean that you must scope the computer.

20-22. *Problem 1:* Look at the repairman in figure 115. He saw something on the display unit that triggered his trouble button. Can you pick out what he saw? If you see the retrace from the map outline, you've got it. Our repairman walks back to the console. He takes a real close look at the display and finds retrace from the *track dot, tag,* and *symbol* (A in fig. 115). Where is the trouble? This is no time for an oscilloscope since he already has what amounts to one in front of him. Why not use it? Okay, now our man goes through several tests with the console itself. The checks he makes include:

a. Reducing intensity with the front panel intensity control. The retrace gets lighter and, just before losing all signal, it disappears. That won't help.

b. Selecting different operating modes. All have the same indications. The problem seems to be localized to the Z-axis (unblanking/intensity). It might include:

- High voltage.
- Improper voltage levels in intensity or unblanking
- Improper timing (consider this as an unlikely possibility because the symbols seem to be proper).

20-23. Our repairman knows that with the front intensity control at maximum no retrace should be visible. Without going into voltage levels (because of the variety of them), it is apparent that retrace is a function of blanking/unblanking. Further, retrace occurs at the end of a sweep cycle when the sweep generators are allowed a short period in which to return to their starting point. If blanking is improper, the return energy produced by the generators is amplified and presented as *retrace.*

20-24. Now our man knows where to look. What should he do? Get the oscilloscope? Not yet. First, examine the logic and alignments to see which control is involved in the blanking/unblanking circuit. Then ask:

- What cards are involved?
- What controls are involved?
- Is there an alignment for correcting this problem?
- Can the work be done on line?

20-25. He answers these questions, and then he gets the oscilloscope. From his list of test points he quickly and accurately measures the controlling waveforms and records his findings. From his findings he researches the alignment for the waveform test point that is improper. He compares the waveform with the standard. Can the *pot* or *variable capacitor* range far enough to correct the problem? This data should be available in his own notes or it definitely can be located in the pertinent TO. A quick look verifies a misalignment or a malfunction. If there is a misalignment, realign; if a malfunction exists, change the card and then align.

20-26. In this problem the oscilloscope came into play after research and display manipulation were completed. A definite precise area was identified in the research as *most probable.* Verification of opinions and conclusions was performed quickly and accurately with the oscilloscope, performance standards, and notes about the signal area.

20-27. *Problem 2:* While the computer is cycling, a failure occurs. From the study of diagnostic programs completed in Chapter 4, you know that the problem must first of all be localized. Clearly, then, this is not the time to use the oscilloscope. However, it is the time to run the diagnostics. Selection of the proper diagnostic may be possible if interpretation from error lamps, failure printouts, and operational printouts provides a clue. In any event, running a diagnostic is the first logic step—not troubleshooting with the oscilloscope.

20-28. Interpretation of the diagnostic printout may identify the exact card or card group replacement that will correct the malfunction. Should this be the case, the oscilloscope would not be used. However, if the card replacement doesn't succeed, then what? Back to the drawing board and on with more function and logic analysis while recycling the diagnostic. Only this time, the diagnostic will have a loop set up in it, allowing us to check the functional area that is suspected to be failing. The function and logic analysis identifies data peculiar to the circuit. It also identifies specific waveforms, data patterns, and voltage amplitudes.

20-29. With the probables listed, additional cards listed, specifications for the patterns and waveforms at hand, and a loop program (manual or software) set up, the oscilloscope can now be used. The loop that is set up in the diagnostic (as explained in Chapter 4) allows point-to-point signal tracing. The oscilloscope is used to verify each point and, at these points, you can make a comparison of measured data or waveforms with the specifications.

20-30. If you are beginning to think that signal tracing with an oscilloscope is a last ditch troubleshooting technique, don't you believe it. Troubleshooting with the oscilloscope is indeed a technique used after considerable study and analysis has been performed. Exercising the equipment, researching technical data, and applying knowledge of their functions to components are usually performed first. These elements may take from a few seconds to many hours to accomplish. Your expertise on the equipment may be so good that you know just what action is required and that signal tracing pin 17 of card A5 will provide the solution to the problem. Or, your expertise and notes may have been leading you to the conclusion that pot R5 is deteriorating, and a scope display will verify it.

20-31. Referring back to paragraph 17-3, where the advice to think before you act was given, this advice applies extremely well to the use of oscilloscope when troubleshooting. THINK the problem out before you jump into the middle of it with a scope. Analyze the problem and its symptoms; check the fault and facility panels for the various error indications that usually accompany equipment failures. The indications provided by this panel can give you a definite starting point for troubleshooting.

21. Analyze Fault Location Indicators

21-1. The use of fault location indicators is another in the series of troubleshooting techniques to be discussed in this chapter. Fault indicators, as the term implies, identify (through the use of various types of lamps) where a malfunction occurred within a system. An indicator may be installed anywhere that is convenient for visual observation. In order for these indicators to convey any meaning to maintenance personnel, they must be appropriately labeled, and the labels or labeling must be kept in a readable condition at all times.

21-2. Since you are training on a computer system, you should already be somewhat familiar with its fault indicator assembly. Therefore, a study of selected fault indicator assemblies of different systems would be of little use to you here, especially when analysis proves they are all the same in principle. This text is used to present a study of these units in terms of their:

- Uses.
- Types.
- Technical order information.

21-3. **Use of the Fault Indicator Assembly.** The two uses provided by the fault indicator assembly are the identification of a failing function or subfunction and the identification of correct or incorrect data flow. Regardless of the extent of coverage that the indicator has on a panel, only one of these two uses is possible. For both uses to be present on a panel, at least two indicators must be used. Let's examine this thought more thoroughly.

21-4. A fault indicator or data flow indicator lamp is frequently located on the panel or assembly containing the circuit it represents. This arrangement is convenient for verification of that function or subfunction of the system. It does, however, have a distinct limitation; that is, each cabinet, rack, chassis, or drawer must be inspected in order to locate the inoperative function. This system is cumbersome, time-consuming, and inefficient. To overcome this limitation, additional indicators are installed at a centralized, convenient location within the system. Notice the words *additional indicators*. The need for primary indicators, those located at the function, is necessary in addition to those remoted to the more convenient location. Some of the most used locations of conveniences are:

- Front doors of cabinets.
- Fault and facility panels.
- Fault indicator and confidence indicator consoles.

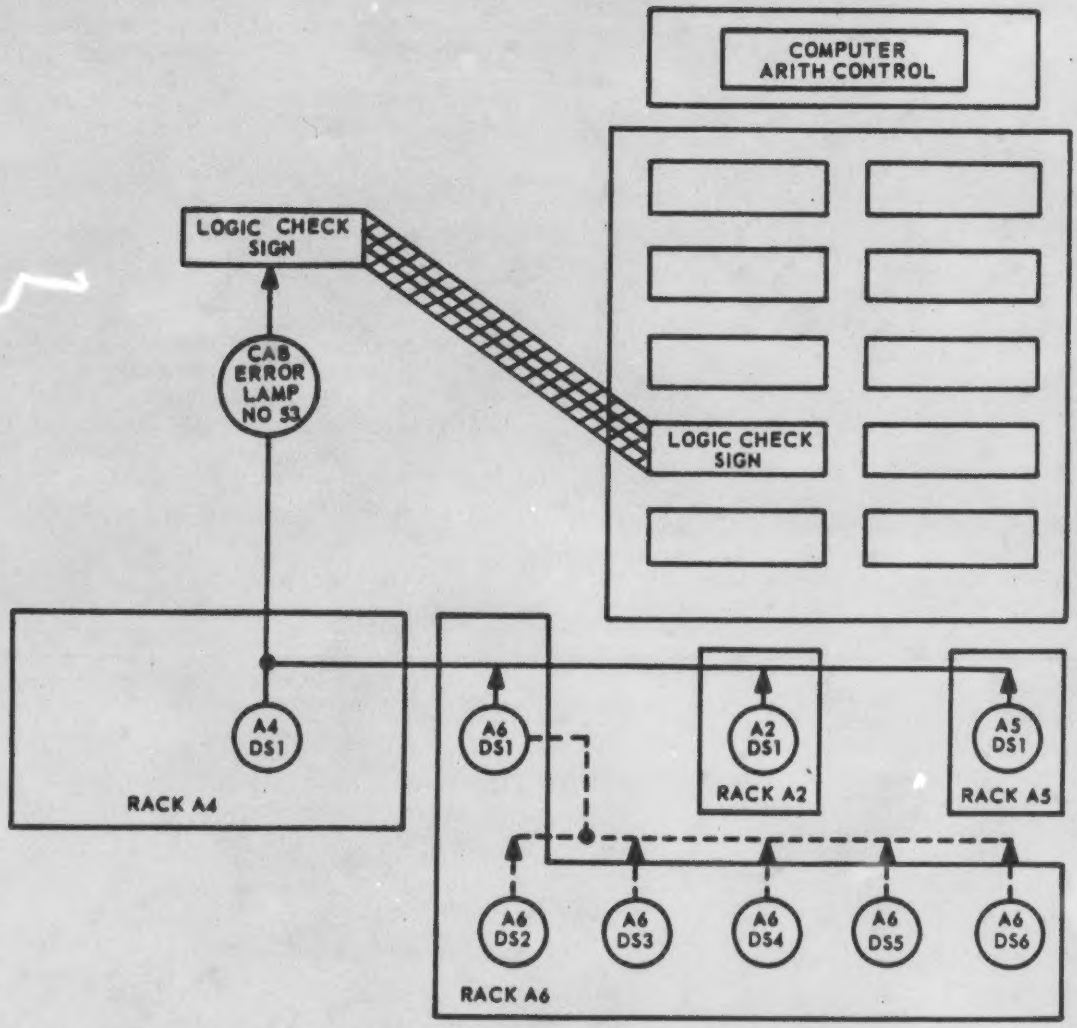


Figure 116. Typical fault facility panel.

21-5. Thus far we have established that each function or subfunction within a system will likely have an indication of operation or failure. Further, because of the volume of circuits and placement of units, a conveniently located fault indicator assembly is made. This assembly, called by various names, provides at a glance the status of all, or most all, equipment within the system. We also identified the two uses for this assembly (para. 21-3). Let's examine each.

21-6. *Identify the status of the function.* The indicators are positioned in groups that are associated with specific functions of the equipment. Figure 116 illustrates this arrangement. The block to the right represents a portion of the central fault panel. It has a functional title, *computer arith control*, and has 10 lamps representing indications of subfunctions within the arithmetic control unit. For explanation and use in this study, only the *logic check sign* indicator is examined. Before identifying when the lamp would light, review the other elements of the figure. Only cabinet 53 is involved, but within the cabinet, racks A2, A4, A5, and A6 provide some control over the logic check sign fault indicator. The light will turn on when an incorrect *check sign* (parity) error occurs from a subfunction in rack:

- A2 when A2-DS1 lights.
- A5 when A5-DS1 lights.
- A4 when A4-DS1 lights.
- A6 when A6-DS1 lights.

Shown in the figure are five additional fault indicators for rack A6. They are DS2, 3, 4, 5, and 6. If one or more than one of these

497

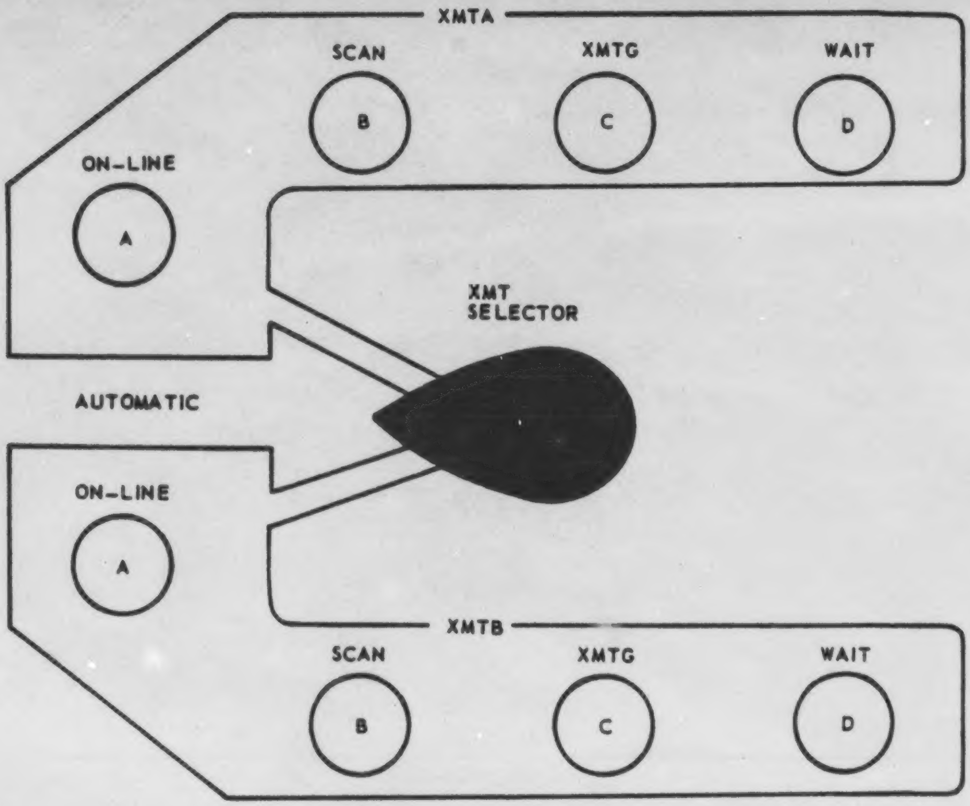


Figure 117. Transmit status panel.

indicators turn on, the rack A6-DS1 lamp lights also.

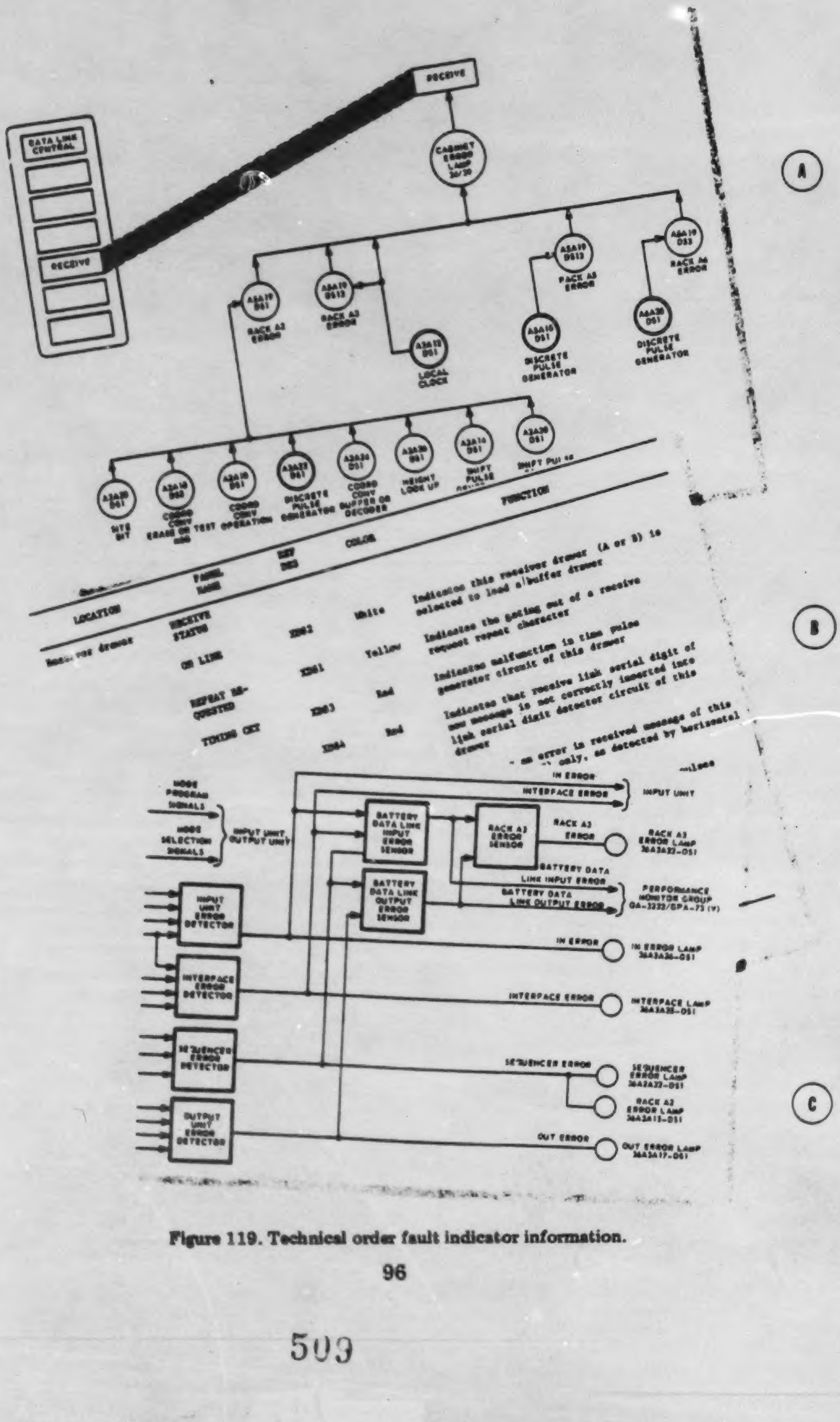
21-7. Lamps A2-DS1, A4-DS, A5-DS1, and A6-DS1 are rack lights and receive their inputs from circuit indications. The breakout of racks A2, A4, and A5 is similar to that indicated for rack A6 in the figure. For this study, the detail in the figure is sufficient. If any rack light comes on, it provides the necessary input to the cabinet light which, in turn, provides the input to the fault indicator —*logic check sign* located in the *arith control* area of the fault facility panel. From this indication, we determine that a problem exists in the arithmetic control circuits and, as a troubleshooting aid, the fault indicator has directed attention to a local area. But, what about data flow?

21-8. *Identify the status of data flow.* Circuit lamps installed on panels are used in various methods to identify data flow. In figure 117, four lamps are used to display the status of a transmitter (XMT A or B) during transmission time. In this system only one lamp is on at any given time. For example, when data is being transmitted by XMT A, a sequence occurs in which lamps B, C, and D are lit and go off. This sequence is repeated each time data is transmitted and, when the cycle is completed, lamp A returns to the ON state.

21-9. Another example of data flow is that of lamps associated with a register or counter. In a register, grouping of its lamps provides a display which, when read, reveals the data stored. This is contrasted with counter operations where each lamp turns on and off at a predetermined rate, thus making count determination difficult. However, the experienced repairman can look at the lamps of a counter and determine if it is stepping correctly by its stepping sequence and rate. All of these examples show the second use of fault location indicators, i.e., data flow. To give you some idea of the more common equipment configurations of fault indicator panel assemblies, we will identify various types.

21-10. **Types of Indicator Panels.** Figure 118 (printed in the workbook) portrays many of the different arrangements of indicators used for the two purposes stated. For identification correlate their use as indicated below with the letter that corresponds to a callout letter in the figure:

508


A
RECEIVE
DATA LINK CENTRAL
RECEIVE
CABINET ERROR LAMP 3A/30
A3A19 DS1
RACK A2 ERROR
A3A19 DS12
RACK A3 ERROR
A3A12 DS1
LOCAL CLOCK
A5A19 DS12
RACK A5 ERROR
A5A15 DS1
DISCRETE PULSE GENERATOR
A6A19 DS2
RACK A6 ERROR
A6A20 DS1
DISCRETE PULSE GENERATOR
A2A20 DS1
SITE BIT
A2A18 DS2
COORD CONV ERASE OR TEST
A2A18 DS1
COORD CONV OPERATION
A2A22 DS1
DISCRETE PULSE GENERATOR
A2A24 DS1
COORD CONV BUFFER OR DECODER
A2A20 DS1
HEIGHT LOOK UP
A2A16 DS1
SHIFT PULSE
A2A20 DS1
SHIFT PULSE
B
C
MODE PROGRAM SIGNALS
MODE SELECTION SIGNALS
INPUT UNIT OUTPUT UNIT
INPUT UNIT ERROR DETECTOR
INTERFACE ERROR DETECTOR
SEQUENCER ERROR DETECTOR
OUTPUT UNIT ERROR DETECTOR
BATTERY DATA LINK INPUT ERROR SENSOR
BATTERY DATA LINK OUTPUT ERROR SENSOR
RACK A3 ERROR SENSOR
IN ERROR
INTERFACE ERROR
INPUT UNIT
RACK A3 ERROR
RACK A3 ERROR LAMP 36A3A22-DS1
BATTERY DATA LINK INPUT ERROR
BATTERY DATA LINK OUTPUT ERROR
PERFORMANCE MONITOR GROUP OA-3232/GPA-73 (V)
IN ERROR
IN ERROR LAMP 36A3A26-DS1
INTERFACE ERROR
INTERFACE LAMP 36A3A25-DS1
SEQUENCER ERROR
SEQUENCER ERROR LAMP 36A2A22-DS1
RACK A2 ERROR LAMP 36A2A13-DS1
OUT ERROR
OUT ERROR LAMP 36A3A17-DS1

LOCATION	PANEL NAME	REF DES	COLOR	FUNCTION
Receiver drawer	RECEIVE STATUS	XDS2	White	Indicates this receiver drawer (A or B) is selected to load a buffer drawer
	ON LINE	XDS1	Yellow	Indicates the gating out of a receive request repeat character
	REPEAT RE-QUESTED	XDS3	Red	Indicates malfunction in time pulse generator circuit of this drawer
	TIMING CKT	XDS4	Red	Indicates that receive link serial digit of new message is not correctly inserted into link serial digit detector circuit of this drawer
				… an error in received message of this … only, as detected by horizontal …

Figure 119. Technical order fault indicator information.

almost in the center. The chart gives the following information:

- Rack.
- Row (the card is located in).
- Card number.
- Type of card.

The malfunction is in rack A1, row 700, cards 21 through 30. Note that the card types vary from inverter (INV) to single-shot (SSA). This is important to note because it tells you immediately that your remove and replace action will involve different card types. Therefore, you must be extra careful in getting the right card with the right part number in the right location. You may be thinking that this is no big thing, and it isn't until you get careless and insert the wrong card in a location. Normally, when this happens you can expect maximum smoke and/or more downtime. But, what really hurts is the fact that you feel like a dwarf among giants looking for a hole to hide your head in. Now you remove and replace cards 21 through 25 and, if this clears the fault indication, you have removed the faulty card and the equipment is again operational. If this action doesn't clear the problem, you then remove and replace cards 26 through 30.

22-3. Another type of remove and replace technique is that which is used in conjunction with a programmed diagnostic test. A message as indicated below is provided by a control program once the diagnostic is called in from the storage media. You respond to this message for program operation. Note that the printout is in two parts. The first part indicates program options, and the second part (titled "Enter Data Control Unit (DCU) and Console Configuration") contains pertinent information regarding the running of the diagnostic:

```
DISPLAY DIAGNOSTIC PROGRAM
DEFINITION OF SENSE SWITCH FUNCTIONS
SW1 LOOP ON SOLID ERROR
SW2 LOOP ON INTERMITTENT ERROR
SW4 INHIBIT TYPEOUT
SW5 CONTINUE TEST
SW6 INHIBIT ELECTRONICS CONSOLE TEST
SW7 INHIBIT DISPLAY BUFFER AND DCU TEST
SW8 DUMP ERROR TABLE
```

```
ENTER DCU AND CONSOLE CONFIGURATION
Y  IF UNIT IS IN THE SYSTEM
N  IF NOT IN SYSTEM
*  TO TERMINATE AND LEAVE REMAINING
ENTRIES UNCHANGED
/  TO RESPECIFY
D  TO DISPLAY CURRENT CONFIGURATION
DCU              CONSOLE
01 02 03 04 05 06 07 08 09 10 11 12 13 14
```

22-4. One of the five characters listed in this second part of the message is printed out for each DCU and console. Each response for a unit is a single typed entry. The diagnostic test performs the required checks in accordance with your selection. If a solid error is detected (for instance, on the loop on solid error check), a message is printed on the keyboard which reads: CHANGE DISPLAY CARD GROUP XXXXXX CON XX. On the actual printout, the Xs would be replaced by either a letter or a decimal number. Figure 121 (printed in the workbook) shows that the alphanumeric code printed is a card group. Let's assume card group B802 is typed out. Referring to the self-test table (fig. 121), you look for card group B802. The columns next to the card group designate the rack DBSG, row 10, and cards 36 through 41. Additional information is given in self-test tables in the form of the part numbers of the cards involved. This information is provided for two primary reasons. First, for replacement purposes, and second, for reference purposes to find out from a parts list (IPB) the type of card.

22-5. We have presented only two examples of the group removal and replacement technique of troubleshooting. There are other applications, but their techniques are the same in principle. It is probable that this technique of group removal and replacement will be the front runner in newer computer systems, especially where integrated circuits and modular units are involved. This technique provides for quick restoration of equipment; therefore, it is an effective technique that is often used on simplex equipment. Be on guard, though, since a card removed as faulty but not repaired creates a catastrophic situation. If you or your fellow workers fail to uphold the integrity of the quality of maintenance, the technique fails.

(1) Counters and registers in operation (A).

(2) Information registers displaying memory core data (B).

(3) Confidence indicators detecting fault conditions (C).

(4) Fault and facility panel showing fault status (upper portion) and data transfer (lower portion) (D).

(5) Status panel displaying status of the computer and associated equipment (E).

(6) Confidence indicator console panel indicating status of the entire system (F).

21-11. **Technical Order Information.** Many portions of the technical orders describe or identify each of the indicators on the panel, board, drawer, assembly, or cabinet. The parts of technical orders and their series which provide data for interpretation and information on the use of indicators are listed below:

- Circuits and diagrams: -3 series.
- Operations chapter of the service manual: -2 series.
- Principles of operation chapter of the service manual: -2 series.
- Maintenance chapter of the service manual: -2 series.
- Fault location guides: part of the maintenance chapter.
- Control and indicator tables: within the operations chapter.

21-12. Figure 119 shows three examples of the various methods in which indicator lamps are shown in technical orders. These three examples are not the only methods used, but they represent the extremes. Figure 119, A shows all the indicator lights, their locations, their purposes, and their connections. When any one of these lights turns on, the RECEIVE light also turns on. Figure 119, B shows a portion of a table which identifies each lamp on a status panel by number, title, and color. Under the *function* heading of the table, a brief description of the lamp's purpose is given. Finally, in C of the figure, the indicators show a rack (36A2, rack A3) error light as well as the functional error lights. Notice that any functional error causes an output from a higher order sensing unit (input or output) to the highest order sensing unit within the cabinet. For example, the figure indicates an input unit error causes an output from the higher order battery data link sensor which, in turn, provides an input to the rack A3 sensor.

21-13. It is evident that the repairman's job of troubleshooting is simplified when system TOs contain fault detection information as outlined in figure 119. Simplified, that is, if he knows how to use the information in working back through the error indicators to the end item—the failing unit. Once at the failing unit he must know how to troubleshoot it; he surely can't remove and replace all the circuit cards within the failing unit, or can he? Depending on the computer system, *group removal and replacement* is an acceptable and adaptable method of corrective maintenance.

22. Group Removal and Replacement Troubleshooting Technique

22-1. Certain systems within the Air Force inventory are built on a simplex mode that does not allow the maintenance man much time for repair. In this case, an accepted method of troubleshooting is group removal and replacement of circuit cards. For instance, if you are called to repair a malfunction, your first action would probably be to analyze the symptoms by use of fault lights, printouts, facility lights, etc. Let's suppose that the fault indications showed a timing error. You now have one of two approaches to choose. First, with a schematic or block diagram, isolate the error to a certain area or group of cards. Second, use charts that identify the trouble symptom and list the cards to be removed. For systems designed to use the group removal and replacement technique, the second method is faster. For example, see figure 120 (printed in the workbook) for a chart that shows equipment arranged by "alarm groups." The equipment is arranged in this way for repair purposes. Each group contains from three to 14 cards. The group removal and replacement concept dictates that removal and replacement is restricted to one-half of the cards, not to exceed seven. If after removal and replacement of the prescribed cards the trouble has been cleared, the cards are taken to the card tester for checkout and location of the faulty component. If the trouble still exists within the group, removal and replacement of the second half of the cards is performed.

22-2. Let's try a sample case in using the alarm group chart. While checking system operation, you find a fault light indicating an azimuth counter error. Referring to the block diagrams, you find that the failing circuit is located in rack A1 (see fig. 120, printed in the workbook). Turning to the alarm condition charts in the technical order, you note the page that lists rack A1. The rack number and alphanumeric designator are, in most cases, in the lower center of the page within the TO. The azimuth counter circuit is shown as being located in the lower one-third of the chart,

Equipment Familiarization (17-2)
Error Indication
  areas (20-4)
  buffer (20-5)
  comparator (20-7)
  control unit (20-8)
  core unit (20-6)
  priority (20-9)
Error Intermittent (20-17)

F

Failure
  catastrophic (15-8)
  causes (15-20)
  characteristics (20-9, 10, 11, 12)
  classification (15-8)
  detection (15-21)
  intermittent (15-8)
  isolation (15-21)
  machine state (15-8)
  random (15-8)
  solid (20-19)
  steady state (15-8)
Fault
  detection (15-6, 16)
  indicators (21-1, 2, 3, 4)
  isolation (15-6; 18-13, 14)
Flood Gun (8-16)
Flow Chart
  computer test (15-23)
  I/O test (15-28)
  symbols (15-21; 16-4)
  tagging (16-5)
Flow Diagrams (15-7)
Frequency
  adjustment (7-14)
  shift keying (1-29; 14-9)
  shift modulation (14-13)
  variations (7-2-6)

G

Group removal and replacement, definition (22-1)

H

Height-Finder
  nod (1-13)
  radar (1-10)
Horizontal drive unit (1-37, 38)

I

Indicator
  confidence (21-6, 7, 10)
  data flow (21-6, 9)
  fault (21-1, 2, 3, 5, 7, 9, 10)
  parity (21-6)
  primary (21-4)
  status (21-10)
Integrated Circuit (5-11)
  display adjust (8-17)
Intensity (11-4, 17, 28, 29, 30)
  unit (1-37, 38)
Interrelationships of Functions (10-16)

K

Keyboards (1-14-20; 2-11)
  operational checks (1-19)

L

Lamps and Audio Alarms (2-9)
Level Detector (14-19, 20, 21)
Line Data (2-2, 3, 9, 11)
  quality (1-30)
Logic, analysis (18-12)
  conditioned (18-10)
  equation (18-6)
  function (18-6, 12)
  functions (18-4)
  high (18-4)
  low (18-4)
  nonstandard (18-1)
  true (18-4)
  variables (18-4)
Loop (20-28, 29)

M

Maintenance Program
  add class (15-24)
  analyze (15-1)
  as a tool (15-3)
  considerations (15-4)
  defined (15-2)
  fundamentals (15-6)
  interrupts (16-8)
  loop (15-24, 25)
  manual intervention (16-9)
  primary function (15-2)
  start big (15-11)
  start small (15-10)
  types of (15-15)
Malfunction (20-25)
Marginal Checking (15-12)
Matrices (13-6, 7)
Mechanical Adjustments (8-1, 2, 3-10)
Memory Units (13-1)
  classes 1 and 2 (13-2)
Message Processors (14-1)
Meter, ohm, adjustment (4-9)
Meters (2-2)
  AC voltmeter (2-2)
  DC meters (2-2)
  differential (2-2)
Meters and dials, adjustment of (Sec 4)
  balancing (4-2)
  centering (4-3)
  ohm adjust (4-3)
Miller Circuit (5-5-7)
Mil-Std-806A (18-1)
Mil-Std-806B (18-2)
Misalignment (20-25)

Index

A
Adjust, read/write amplifier (8-12)*
Adjustments (3-7, 11; 5-14; 7-13, 14; 8-1, 2, 9, 17; 9-3)
  definition of (Intro., Chap 2)
  instructions (3-12)
Alignment (20-25)
  block diagram (10-41)
  concept (10-1)
  definition of (Intro., Chap 2)
  objective of (10-2, 33)
  panel (8-21, 22; Fig. 55)
Amplifier and Pulse Generator (Sec 5)
Amplifier, video (2-3; 9-4)
Analog Data (9-5)
Analysis
  approach (20-3)
  diagram (20-15)
  function (20-16)
Angle Mark (1-13)
Antenna, beacon (1-2)
  height-finder (1-11)
  radar, search (1-11)
Antennas, directional (1-6)
Automatic Change Pulse (1-12)

B
Beacon (1-8)
Binary (19-4)
Boole, George (18-3)
Boolean, algebra (18-3)
  equation (18-4, 5)
  variables (18-7, 8, 9)
Bracket pulses (1-8, 9)
Buffer Storage (8-17)

C
Capacitor Read Only Storage (13-2)
Capacitors (9-4)
  life span (3-7)
  trimmer (3-6)
  tubular (3-7)
  variable (3-5)
Central Processor (1-40; 2-8, 9, 11)
Charactron Tube (11-10)
Code
  alpha (19-12)
  Fieldata (1-16, 17, 18; 19-12)
  numeric (19-12)
Coincident Current (8-14)
Computers, general-purpose (15-4)
Confidence (15-2)
Controls
  adjustment (9-6)
  mechanical (9-6)
  principles of operation (3-5)
  purpose (3-2)
  types (3-3)
  variable (Sec 3; 3-2; 5-1; 7-11, 12)
Conversion, MP (14-3)
Core Memory (13-2)
Counters (13-6, 7)
CRT Display (2-3, 4, 8, 11)

D
Data Input/Output Circuit Adjust (9-1)
Decibel (1-31)
Decoders (13-6, 7; 14-6)
Deflection (11-5, 10, 17, 18, 26, 27, 34, 41)
Delay line (13-2)
  adjust (8-9)
Dependent/Independent Functions defined (10-27, 28)
Diagnostic, program (15-17)
Diagnostics (15-2; 20-27, 28, 29; 22-3)
Digital Data (9-2)
  analyzing (19-3)
  content (19-3, 4)
  information (19-3)
  manipulated (19-5, 6, 7)
  program (19-3)
Dipole Data (1-29)
Disk Memory (8-10; 13-2)
Display
  blanking (20-23, 24)
  oscilloscope (19-11, 13)
  principle of (11-6, 7, 10, 16)
  retrace (20-23)
  symbol (20-22)
  tag (20-22)
  track dot (20-22)
  unblanking (20-23, 24)
Drum (13-2)
  head adjust (8-4, 5)
Duty Cycle (7-15)

E
Electrical Adjustment, principles of (8-11-24)
Electromechanical devices, defined (12-1)
Encoder (14-6)

---

*Indicates paragraph number, unless otherwise stated.

T
Tape Head Adjust (8-6, 7, 8)
Tape Memory (13-2)
Tape Transport Units (1-21; 2-11)
Technical Orders
  adjustment instructions (3-12)
  alignment (7-16)
  maintenance chapter (3-12)
  preventive maintenance (Chap 1, Intro.)
  preventive maintenance manual (7-16)
  series (21-11)
  service manual (7-16)
Test instruments
  oscilloscope (18-16; 20-20, 21, 22, 25)
  vacuum-tube voltmeter (18-16)
Thin Film Adjust (8-13)
Timing (7-2-5; 11-3; 14-4, 6)
Timing devices, adjustment of (Sec 7)
Timing Routines (7-13)
Time Sharing (11-12, 23; 19-8)
Timing Unit (1-37, 38)
Transformer Read Only Storage (13-2)
Transistor, operation (10-13)
Transmission line, linear amplifier (1-28)
Transmission of Data (9-2)
Transmission Path (1-32)
Transponder (1-8)
Troubleshooting
  block diagram (18-13, 14)
  indications (20-31)
  instruments (18-16)
  intermittent (20-2)
  patterns (18-17; 19-1, 2)
  procedures (17-1, 4)
  sequence (17-3)
  signal injection (18-16)
  split-half (18-15)
  waveforms (18-17; 19-1, 2)
  with oscilloscope (20-30)
Truth Table (18-7, 8, 9)
Typotron Tube (11-10)

V
Video (9-4; 11-4, 24, 31)
  amplifier (see Amplifier)
Variable Capacitor (20-25)
Variable Controls (see Control)
Vertical Drive Unit (1-37, 38)
Vector Diagrams (11-7)

W
Waveform
  amplitude (19-9, 21, 25)
  amplitude-modulated (19-9)
  analog (19-8, 14, 15)
  digital (19-3-8, 11)
  formula frequency (19-9)
  frequency-modulated (19-9)
  load level (20-3, 16)
  multiple-cycles (19-9)
  patterns (19-16, 17)
  reading (19-15)
  rectangular (19-16)
  signal tracing (20-1, 18)
  square (19-16)

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Modems (1-41; 14-12)
Multiple Club Approach (15-13)
Multivibrators (7-10)

N

Noise Cancler (14-12)
North
  Magnetic (1-12)
  true (1-12)
Nulling, principle of (12-5)

O

Operational Amplifier (5-2-4)
Operator, Communication (16-7)
Oscillators (7-10)
Oscilloscope (2-3-6; 20-26, 27, 28)

P

Parity (19-12)
Performance Checks
  CRT display (1-36)
  parts of a display (1-37)
  visual examination of mechanical assemblies (2-10—
Potentiometer (3-9, 10; 4-9, 12; 5-10; 6-5, 6; 8-17, 18, 19-22; 9-4; 20-25)
  application of (4-5)
  carbon pile (3-9)
  linear (3-11)
  null adjustment (4-7)
  ohms adjustment (4-9-12)
  tapered (3-11)
  wire wound (3-9)
Power Supplies (1-45; 2-2, 9,11)
  adjustment of (6-1, 2)
  high-voltage (6-6)
  low-voltage (6-4)
Printer Power (1-34)
Printers (1-33)
  character formation (1-34)
  switches (1-34)
Printouts (1-35; 2-8, 11; 20-27, 28)
  error (16-11)
  error table (16-16, 17)
  formats (16-18)
  interpretation (16-1; 20-28)
  uniformity (16-10)
Process of elimination (15-14)
Processing, MP (14-8)
Program
  confidence-diagnostic (15-19)
  control (16-6)
  diagnostic (18-11)
  executive control (16-3)
  fixed (15-4)
  multiple clue (15-18)
  organization (16-3)
  overall (15-18)
  process of elimination (15-18)
  standardization (16-2)
  start big (15-18)
  stored (15-5)
  wired (15-5)
Programming (11-11, 14, 15, 21, 24, 25)
Programming Techniques (15-9)
Pulse Generator (5-8)
  use of RC time constant (5-9)

R

Radar
  definition (1-2)
  height finder (19-18; 19-22)
  principle of (11-16)
  range (19-11)
  returns (1-2; 1-7; 2-3, 4, 11)
  rotation(1-12, 13; 2-11)
  video (1-7)
Radar and Beacon (1-1, 2)
Radar Antenna (1-11; 2-11)
  rotation (11-18, 19)
Random Access (13-5)
Range Mark (1-13)
Radio Wave Reflection (1-3)
Rate Feedback (12-6, 8, 10)
RC Time Constant (5-9, 11, 12)
Read/Write Amplifier Adjust (8-12)
Read/Write Cycles (13-8)
Reference Voltages (2-2, 11)
Registers (13-6, 7)
Relays (9-6)
Reliability (15-2)
Routine
  addressing test (15-26)
  beat test (15-26)
  computer test (15-22, 23)
  core plane crosstalk test (15-26)
  I/O test (15-27, 28)
  memory test (15-26)
  program similarities (15-29)

S

Saturable Reactor (9-6)
Selective Identification Feature (1-8, 9)
Self-Test Tables (22-4)
Sequencing (14-6)
Sequential Access (13-5)
Serial/parallel functions, defined (10-28, 29, 30)
Servos (1-22; 2-11)
  units (2-3, 10, 11; 12-22)
Signal Tracing (20-30)
Spacebar (12-25)
Space elements, KPP (12-26)
Spacing theory, KPP (12-24)
State Indicators (18-2)
Storage devices, adjustment of (Sec 8)
Storage tube adjust (8-16)
Switches (14-6, 7)
Symbol Generator (11-8)
Symbols (10-37)
System Integrity (15-2)

TABLE OF CONTENTS

Study Reference Guide

Chapter Review Exercises

Answers For Chapter Review Exercises

Volume Review Exercise

ECI Form No. 17

Text Chart and Figures

7-4 505

30554 02 21

WORKBOOK

System Maintenance

SELF-TEACHING AIDS
CRE
VRE
SRG

This workbook places the materials you need *where* you need them while you are studying. In it, you will find the Study Reference Guide, the Chapter Review Exercises and their answers, and the Volume Review Exercise. You can easily compare textual references with chapter exercise items without flipping pages back and forth in your text. You will not misplace any one of these essential study materials. You will have a single reference pamphlet in the proper sequence for learning.

These devices in your workbook are autoinstructional aids. They take the place of the teacher who would be directing your progress if you were in a classroom. The workbook puts these self-teachers into one booklet. If you will follow the study plan given in "Your Key to Career Development," which is in your course packet, you will be leading yourself by easily learned steps to mastery of your text.

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EXTENSION COURSE INSTITUTE

Air University

CHAPTER REVIEW EXERCISES

The following exercises are study aids. Write your answers in pencil in the space provided after each exercise. Immediately after completing each set of exercises, check your responses against the answers for that set. Do not submit your answers to ECI for grading.

CHAPTER 1

Objective: To show an understanding of the requirements for and importance of performing checks on equipment.

1. List four problems that arose from early practices of performance checking. (Intro.)

2. Operational/performance checks are usually performed in input/output equipment using what type of method? (Intro.)

3. Define "radar." (1-2)

4. What type of antennas do radar sets use? (1-6)

5. Radar returns received by data processing equipment can be received in what two forms of video? (1-7)

6. MTI video is used to ____ __________________________. (1-7)

7. State briefly the function that a beacon is capable of performing. (1-8)

8. What do the letters IFF and SIF mean? (1-8)

9. How do height-finder antennas differ in operation from search radar? (1-10,11)

STUDY REFERENCE GUIDE

1. *Use this Guide as a Study Aid.* It emphasizes all important study areas of this volume.

2. *Use the Guide as you complete the Volume Review Exercise and for Review after Feedback on the Results.* After each item number on your VRE is a three digit number in parenthesis. That number corresponds to the Guide Number in this Study Reference Guide which shows you where the answer to that VRE item can be found in the text. When answering the items in your VRE, refer to the areas in the text indicated by these Guide Numbers. The VRE results will be sent to you on a postcard which will list the *actual VRE items you missed.* Go to your VRE booklet and locate the Guide Number for each item missed. List these Guide Numbers. Then go back to your textbook and carefully review the areas covered by these Guide Numbers. Review the entire VRE again before you take the closed-book Course Examination.

3. *Use the Guide for Follow-up after you complete the Course Examination.* The CE results will be sent to you on a postcard, which will indicate "Satisfactory" or "Unsatisfactory" completion. The card will list *Guide Numbers* relating to the questions missed. Locate these numbers in the Guide and draw a line under the Guide Number, topic, and reference. Review these areas to insure your mastery of the course.

Guide Numbers 200 through 221

Guide Number	
200	Introduction to Performance Checks; Sources of Data Affecting Operational Checks: Radar and Beacon–Keyboards; pages 1–6
201	Sources of Data Affecting Operational Checks: Tape Transport Units–Power Supplies; pages 6–14
202	Devices Used to Accomplish Performance Checks; pages 14–19
203	Adjustments; Characteristics of Variable Controls; pages 20–23
204	Adjust Meters and Dials; pages 23–25
205	Amplifiers and Pulse Generators; pages 25–28
206	Adjust Power Supplies; Adjust Timing Devices; pages 28–31
207	Adjust Storage Devices; pages 31–37
208	Adjust Data Input and Output Circuits; pages 37–38
209	Alignments; Alignment Concept; pages 39–46
210	Displays; pages 46–52
211	Electromechanical Devices; pages 52–57
212	Memory Units; Message Processors; pages 57–61
213	Programming; Analyze Computer Maintenance Programs: Maintenance Program Defined–Confidence-Diagnostic Program; pages 62–65
214	Analyze Computer Maintenance Programs: Causes of System Failure–Input/Output (IO) Test Program; pages 65–70
215	Interpret Maintenance Program Printouts; pages 70–74
216	Troubleshooting; Troubleshooting Considerations; pages 75–77
217	Analyze Logic and Wiring Diagrams; pages 77–82
218	Analyze Patterns and Waveforms; pages 82–88
219	Signal Tracing Techniques; pages 88–93
220	Analyze Fault Location Indicators; pages 93–97
221	Group Removal and Replacement Troubleshooting Techniques; pages 97–97

22. What are four basic portions of almost all display units? (1-36,37)

23. What is the assembly in a data processor which verifies performance? (1-40)

24. Most performance checks used in data processors require the ______________________________. (1-41,42)

25. What four elements do most power supplies have? (1-45)

26. What are the three common methods of regulation of a DC power supply? (1-45)

27. What two types of devices are usually included in DC power supplies which aid in verification of its performance? (1-46)

28. List the areas of a computer system which usually require the use of a meter while performance checking is performed. (2-1,2)

29. The oscilloscope is used extensively for equipment validation. List some of the elements within an oscilloscope display that are checked during performance checks. (2-3)

30. How is radar data entry usually verified? (2-3)

31. List the devices usually used when performing operation checks. (2-2–10)

10. What circuit is often incorporated in data processors to compensate for variations from north? (1-12)

11. A visual check for verification that the nod angle of a height finder is accurate is made by using ____________ and measuring ____. (1-13)

12. Striking a key on a keyboard results in mechanical, electromechanical, and electronic actions. For this action to be useful for a data processor or computer, what electronic action must take place? (1-16–20)

13. In what two general ways may a keyboard be used? (1-16,20)

14. An electrical error voltage is used in a tape transport unit for what purpose? (1-22)

15. Performance checks can be expected to be performed on which assemblies within the tape unit? (1-22,23)

16. How is attenuation of signals in transmission lines compensated for? (1-26–29)

17. What does the term *line quality* mean? (1-30)

18. Define "decibel." (1-31)

19. At what range does the decibel level of a signal usually enter a transmission line? (1-32)

20. What test is most often used for performance verification of a printer? (1-33)

21. What are the four areas within a printer which can be expected to be examined by performance checks? (1-34)

CHAPTER 2

Objective: To demonstrate a knowledge of how adjustment of variable components affects circuit operation.

1. Define the term "adjustment," as used in connection with circuits. (Intro.)

2. List three purposes of variable components. (3-2)

3. List six dielectric materials used in capacitors. (3-5)

4. Is the trimmer capacitor used most frequently in a computer system linear or nonlinear? (3-6)

5. What is a common problem encountered with the variable capacitor? (3-7)

6. Name the two types of variable resistors. (3-3,9)

7. Of the two types of variable resistance components, which is usually used when a wire-wound resistance is needed? (3-9)

8. Explain the "pickoff" principle of a potentiometer. (3-10)

9. List two manufacturing methods that are used to indicate the extreme ends of a potentiometer adjustment screw turning capacity. (3-10)

10. Name the two different methods of manufacturing carbon resistance deposits within a potentiometer. (3-11)

11. Which adjustment is made on a meter or dial that requires:
    (a) no voltage and (b) voltage? (4-2,3)

12. If a meter needle is in the *null* position of a differentiating measuring circuit, the load circuit is said to be ______________________________ . (4-4,5)

13. Explain how a potentiometer can be used as a rheostat. (4-5)

14. Why is zeroing of the ohmmeter necessary when changing scales? (4-9–12)

15. What are the primary objectives of the variable components used in amplifiers and pulse generators? (5-1)

16. What characteristic of an operational amplifier makes it linear? (5-2–4)

17. What must you change in order to make a Miller circuit with a variable output from an operational amplifier? (5-5–7)

18. How is the output from a variable pulse-width generator altered? (5-8–11)

19. Name four electronic component devices which are used in power supplies for regulation. (6-4)

20. What is usually the controlling component when DC power supplies are adjusted for a precise output? (6-1–6)

21. If a potentiometer is incorporated in a high-voltage power supply, how is it often installed? (6-6)

22. In addition to master timing generators, what other types of timing circuits may make use of the variable component? (7-10)

23. For what two functional uses can you expect to be using the variable component in a generator? (7-13-15)

24. When performing adjustments on storage devices, what type of storage may require mechanical adjustment as defined in this text? (8-1,2,9)

25. Drums, tapes, and disk systems use a head to read from and write onto another recording storage medium. How are these head placements performed? (8-4,6–8,10)

26. In memory units containing devices which are *not* adjustable, what circuitry associated with the memory usually has the variable component? (8-12–14)

27. What three basic characteristics of the display shown in figure 55,D, are controlled by potentiometers? (8-17–23)

28. Is the adjustment of data received or transmitted restricted to potentiometer or variable capacitor use only, or may both be used? (9-1)

29. If data (video) is being received at too low an amplitude (attenuated), which control, the variable capacitor or potentiometer, would you expect to find exercising the most control? Explain your answer. (9-4)

CHAPTER 3

Objective: To exhibit an understanding of the characteristics of alignments.

1. What is necessary in order for an alignment to be meaningful and effective? (10-1)

2. Generally, what information about the alignment routine can be obtained from the title? (10-5,6)

3. In order to obtain the basic objective of an alignment, what two basic knowledges must you define? (10-6–8)

4. What purpose is served by listing the subunits and circuits within an alignment? (10-9–15)

5. If a circuit under alignment is dependent upon external circuitry for its inputs, where would you look for prerequisites to performing the alignment? (10-16–21)

6. What does determining the sequence of interrelated functional units mean? (10-22)

7. What is an interrelated function that is classed as independent? (10-27)

8. What would make an interrelated function dependent? (10-28)

9. For what two general reasons may priorities used in alignment procedures be included? (10-31)

10. What elements of the study presented in this chapter are used when aligning the objective? (10-33–40)

11. What are four logical functions in most display units? (11-1)

12. List six significant subfunctions in the display functional areas using timing. (11-3)

13. For what are intensity unblanking circuits used? (11-4)

14. Normally, how many sweep generators does a display have? (11-5)

15. Normally, how many deflection units does a display have? (11-5)

16. State the purpose of a statistical information display. (11-6)

17. How may a binary word be inserted into a system with the result that a symbol is generated? (11-7,8)

18. List the different ways by which a DID unit presents data on the CRT screen. (11-10)

19. Of the four types of display programming, which one do you have *least* influence and control over? (11-12–15)

20. List five methods that are used to perform programming of a display. (11-15)

21. Which type of radar display has circuitry provided for *search lighting*? (11-16)

22. Alignment of search and height consoles includes azimuth orientation with north mark; however, height requires an additional alignment and it uses the ______________________________ for its orientation. (11-17)

23. When aligning servo units in the processor with radar set servos, what magnitude of difference voltage should you strive for? (11-18,19)

24. A measure of sweep linearity commonly used in displays of search and height-finder radars is the use of ____ . (11-17–20)

25. If data selection is to be limited to targets displayed on a console with only specified properties, what might some of these limitations be? (11-22)

26. As with SIDs and DIDs, radar display consoles and their circuits have alignments of their sweep generators. List four characteristics of the alignments common to these types of consoles. (11-26)

27. Alignment of intensity and unblanking circuitry in a display console usually includes three main requirements. What are they? (11-28–31)

28. When aligning a high-voltage power supply in a console, instructions usually include setting of a voltage output and ________________________. (11-32)

29. If interaction existed in an alignment of a display, in which of the four basic units would you expect to find this interrelationship? (11-34)

30. Using figure 75 printed in the text, identify the prerequisites and interrelationships. (11-35,36)

31. Using figure 76, identify the interrelated units. (11-39)

32. List the controls which are included in figure 77 for the horizontal or vertical deflection and state the purpose of each. (11-41)

33. What does "electromechanical" imply? (12-1)

34. Explain the major objective of a servoalignment routine. (12-3–5)

35. Since the servo shown in figure 79 is typical, where can you expect to find the null point in servo units? (12-11)

36. From your study of servos, can you expect to find interrelationships with other units? Explain. (12-13–16)

37. Alignment of a servo unit could probably call for what type of measurement equipment? (12-22)

38. In the three parts of a keyboard-printer-punch unit explained in the text, what is a *common* requirement? (12-23)

39. Identify the two methods which result in the carriage moving during *spacing* on the keyboard-printer-punch. (12-25)

40. Identify the serial and parallel interrelationship required to perform the spacing alignment by using figure 84. (12-28,29)

41. Define the two classes of memory units as written in the text. (13-2)

42. List the five functional areas you can expect each memory unit to contain. (13-2,3)

43. What type of circuit is most commonly used in memory address circuitry? (13-6,7)

44. List the three general requirements needed for a message processor to perform its function. (14-2–7)

45. Name the two methods by which time sharing can be designed into a message processor. (14-6,7)

46. Referring to figures 87, 88, and 89 (printed in the text), name each type of waveform. (14-8–10)

47. Explain how misalignment of the *level detector pot* could result in improper data being processed by the modem unit. (14-12,22)

CHAPTER 4

Objective: To demonstrate a knowledge of the concepts of maintenance programming, including maintenance program functions, fundamentals, techniques, and printouts.

1. What is the function of a computer system maintenance program? (15-2)

2. What must a maintenance program do in order to perform its function adequately? (15-2)

3. Identify the two basic classes of automatic computers. (15-4)

4. What is the classification of the wired-in logic which controls the automatic functions of a computer? (15-5)

5. Name two fundamental tasks performed by maintenance programs. (15-6)

6. What is the design of maintenance programs based on? (15-8)

7. Name the three categories of system failure. (15-8)

8. List five major system maintenance programming techniques. (15-9–14)

9. What factor does the reliability program stress, and what factor does it generally minimize? (15-16)

10. Explain how you would establish a program loop within a given maintenance routine. (15-24)

11. Explain the memory address test routine. (15-26)

12. What is the term associated with the design of a maintenance program that doesn't require external control? (16-3)

13. Define a maintenance control program. (16-6)

14. What do the more standardized types of operator communication provided within maintenance programs include? (16-7)

15. Identify the items that are considered essential in the uniformity of program printouts. (16-10)

16. Refer to the AN/FSQ–7 (SAGE) maintenance program printout in the referenced text. Identify the meaning of item 2 results of the program run:
4...E2... +15 -040 FAILURE MC WORD 005 PRESCRIBED 40 ROUTINE 2. (16-12,13)

17. Refer to the AN/GSA–51A (BUIC) maintenance program printout in the referenced text. What would the CONTROL WD contain if a write operation were performed on tape unit 4? (16-14,15)

18. For what are descriptors used in AN/GSA–51A (BUIC) programming? (16-14,15)

19. Refer to the 407L magnetic tape diagnostic program printout in the text. What sense control switch (SW) would be used to inhibit an error printout? (16-16)

20. Refer to the 407L magnetic tape diagnostic program printout in the text. Explain the use of the indicated repair statement: CHANGE MTS CARDS CRR 0 0 0 (16-16,17)

CHAPTER 5

Objective: To show an understanding of how to combine the various techniques of troubleshooting by analyzing the elements of the techniques.

1. List six troubleshooting aids that relate to computer systems. (Intro.)

2. What should be achieved by analyzing trouble symptoms? (17-1)

3. Why are steps 6 and 7 of figure 96 (printed in the text) *always* included in a troubleshooting procedure? (17-4)

4. Give a brief definition of boolean algebra and state what is usually involved in troubleshooting with this form of algebra. (18-3)

5. Are boolean equations usually developed from the input to the output or from the output back to the input? (18-4)

6. Why is the $\overline{\text{TFGOO}} \cdot \overline{\text{TFG35}}$ portion of the boolean equation explained in paragraph 18-5 inclosed in parentheses? (18-5)

7. In the actual use of a boolean equation for troubleshooting, is the same process used that is used for developing the equation? Explain (18-5,6)

8. Define a "truth table." (18-7,8)

9. Using the problem explained in paragraph 18-8 and figure 101, explain why the truth table clearly identified AND gate 6 as the defective one. (18-8–11)

10. Explain the "functional area approach" concept of logic analysis. (18-13)

11. What is another term for the "functional area approach"? (18-13,14)

12. Explain the "split-half" method of troubleshooting. (18-14,15)

13. Of the five *important* considerations listed in paragraph 18-16 to be used with signal injection approach, which would be used *with* the signal injection itself? (18-16)

14. Name the two reasons for measuring patterns and waveforms. (19-2)

15. What is done with the information that comprises digital data? (19-3)

16. List four ways in which digital data may be displayed. (19-3)

17. According to the referenced text the digital data count of 011 would be stored on a track having how many aircraft in the formation? (19-4)

18. If data stored in digital form represents a decimal equivalent of 10 and a *left shift* is applied, what value will the resulting action produce? (19-5)

19. If tracks and sweep presentations are to be presented on a CRT during a specified period of time, what principle of display is used? (19-8)

20. How does frequency modulation differ from amplitude modulation? (19-9)

21. Using the binary configuration in paragraph 19-11, calculate what the values would be if the first 8 bits represented:

    a. Height data with an LSD of 375 feet.
    b. Velocity data with an LSD of 50 mph. (19-11)

22. In reading the average DC level of a pulse train, if the pulse train is symmetrical, what is the average DC level? (19-15,16)

23. Define "before the fact troubleshooting." (20-2)

24. In the memory troubleshooting problems, what single reason was exposed that made the control unit a prime suspect? (20-8)

25. What facts about each of the signals generated in the memory control unit are needed to verify that the signals are correct? (20-15)

26. If a memory problem is intermittent, what would you look for when scoping the memorys' control unit generators? (20-18–20)

27. In the study in the text concerning when to use the oscilloscope, what information did the maintenance man collect before using the scope? (20-21–26)

28. At what point in troubleshooting is the oscilloscope used when a diagnostic lists cards to be replaced do not clear the problem? (20-28,29)

29. List the two uses of the fault indicator assembly. (21-3)

30. In order for a remote facility panel to properly display the status of circuits indicated by the lamps, what condition must be present in the circuits? (21-6)

31. What do the common elements of indicator panels provide for as aids for troubleshooting? (21-10)

32. List the different technical orders which identify fault and status indicators. (21-11)

33. What restriction is placed upon the technique of remove and replace? (22-1)

34. For the group removal and replacement technique to be effectively used, technical orders are prepared with what listing–tables or charts? (22-2)

35. What product of a computer system is a variation of the technical order chart showing a functional card group? (22-3)

ANSWERS FOR CHAPTER REVIEW EXERCISES

CHAPTER 1

1. (1) Decrease in operational availability.
   (2) Increase in chance for human error.
   (3) Great temperature variations in environmentally controlled cabinets.
   (4) Tinkering.

2. These methods are used:

   a. Lamps, audic alarms, and internal tests.
   b. Printouts.
   c. Meters.
   d. Oscilloscope.
   e. Display CRTs.
   f. Visual examination of mechanical units.

3. Radio direction and ranging.

4. Directional.

5. Raw/normal or processed video.

6. Distinguish aircraft returns from clouds by detection of velocity changes in returns and generate a pulse when this condition exists.

7. A beacon can identify the types of aircraft in the sky by means of codes received from aircraft.

8. Identification friend or foe, and selective identification feature.

9. Height-finder antennas usually nod up and down and can move horizontally on command, while search radars usually rotate an antenna assembly upon a fixed pedestal.

10. Automatic change pulse counter.

11. Angle marks, the intersect point of an angle mark with a range mark for the exact height readout.

12. The action must be converted digital codes.

13. As an input device and as an output device.

14. To supply voltage for servos which in turn rotate the reel assemblies.

15. Servos, motors, vacuum pump, reel assemblies, tape head, positioning, photocells, voltages, currents, and tape tension.

16. By inclusion of high-gain amplifiers inserted at repeater stations every 6 or 7 miles.

17. The degree of interference or absence of interference in a transmission line.

18. A unit of power ratio.

19. +6 to -25db.

20. Operating the machine to produce a copy (printout).

21. *a.* Switches.
    b. Power.
    c. Character formation.
    d. Mechanical assemblies.

22. *a.* Vertical drive unit.
    b. Horizontal drive unit.
    c. Intensity unblanking unit, or Z-axis.
    d. Timing unit.

23. Fault facility panel.

24. Exercising of circuits by processing with test data.

25. *a.* AC source.
    b. Transformer unit.
    c. Rectifier unit.
    d. Regulator unit.

26. *a.* Shunt voltage regulation.
    b. Series voltage regulation.
    c. Constant current regulation.

27. Meters or lamps.

28. Line data, power supplies, and reference voltages.

29. Pulse width, signal amplitude, linearity of signals, proper voltage levels, PRT, phase, polarity, noise levels, waveforms (such as ramps, timing, deflection intensity, generator outputs), and data content.

30. With an oscilloscope.

31. Lamps and alarms, printouts, meters, oscilloscope, CRT display equipment, visual examinations.

CHAPTER 2

1. Adjustment is the act whereby a device is used to alter a condition to make it fit or correspond.

2. (1) Alter bias voltage to a circuit.
   (2) Alter frequency of a circuit.
   (3) Shift a frequency.
   (4) Attenuate or amplify a signal.
   (5) Limit or eliminate distortion.

3. Ceramic, mica, glass, polystyrene, teflon, and air.

4. Linear.

5. Each component has a specific mechanical life cycle.

6. Rheostats and potentiometers.

7. Rheostat.

8. The contact attached to the pickoff terminal usually rests on a carbon resistance element. Each end of the element is in series with the source voltage or current. The position of the contact on the carbon resistance dictates the pickoff voltage or current.

9. An audible click and a pin to stop rotation.

10. Linear deposits, and nonlinear (logarithmic) deposits.

11. (a) Balancing and (b) zeroing or centering.

12. Equal to the balancing or applied voltage.

13. By connecting the pickoff output and one end of the potentiometer to a common point.

14. Each scale may have a different total resistance or it may have a different applied voltage or it may have both.

15. To alter the gain ratio of the circuit, control the pulse duration, or act as a phase-shifting device.

16. Incorporation of a high-gain amplifier.

17. Remove the feedback resistor and install a variable capacitor.

18. By control of the RC time constant with a variable capacitor or a resistor.

19. Silicon-controlled rectifiers, zener diodes, thermistors, and thyratron semiconductor devices.

20. A potentiometer.

21. It usually is installed remote for the power supply with one leg of the resistance (carbon or wire) tied to ground and the other leg left untied (infinity). The wiper is tied to the power supply.

22. Free-running oscillators, one-shot MVs, blocking oscillators, time-sharing generators, and AGL generators.

23. Frequency adjustment and duty cycle adjustment.

24. Drums, tapes, disks, and delay line (magnetorestrictive).

25. The heads are placed a specified distance above the recording surface on drums and disks. The tape heads are installed as per TO instructions and the tape tension and position are controlled by variable components.

26. Read/write amplifiers.

27. Horizontal and vertical width of each character, horizontal and vertical position of all the characters, and horizontal and vertical height of each character.

28. Both.

29. The capacitor would have the most effect upon the amplitude of the high-frequency video signal. An exception to this answer is that condition within the circuit where a potentiometer is performing a clipping or clamping action. In this case, control by the capacitor would be effective up to the clipping or clamping level.

CHAPTER 3

1. A complete understanding of the overall function of the circuits within the alignment.

2. The particular area, function, or subfunction of the equipment.

3. A definition of the objective and related part of all TOs which provide the definition, and the electronic principles involved in the function to be aligned.

4. The list provides knowledges of the purpose, place, and significance of each circuit in the alignment. It also identifies the controls and their placement.

5. (1) Substeps in the first part of the alignment.
   (2) Verification instructions.
   (3) Sequencing of other alignments with the alignment to be performed.

6. What part must be aligned first, second, and third.

7. A generator.

8. External signals are required as input for the dependent function to operate and for it to provide a discrete output.

9. (1) Interaction of waveforms with each other.
   (2) Sequence of performing steps in a routine.

10. Steps 1, 2, the portion of step 4 which relates to serial-parallel paths and priorities, and all of step 5.

11. Timing, intensity, vertical, deflection, and horizontal deflection.

12. Sweep time generation; sweep and symbol modes, time sharing; intensity unblanking and blanking; data or video control; expansion factoring; and special pulses for special display features being impressed on vertical, horizontal, or intensity units.

13. To control turn-on and turn-off of the CRT and to provide a path for the display images.

14. One.

15. Two.

16. To provide—in visual, graphic form—digital information for command personnel to monitor and evaluate.

17. A console operator depresses a pushbutton which is either prewired with a binary code or activates a code generator.

18. By use of a charactron CRT, a typotron CRT, or programmed memory intergrated circuits.

19. Hard wired matrix.

20. Switch action, tag symbol correlation, omniball or wheels attached to digital-to-analog converters, light gun correlation, and keyboard to memory program.

21. Height finder.

22. Angle mark.

23. Null.

24. Range marks.

25. Specific height groups, initial tracks, old tracks, tracks with beacon and with identification, hostiles, and weapons.

26. Sweep voltage amplitude, pulse duration, slope angle, and proper phasing.

27. Gate amplitudes, gate shaping (no overshoot or undershoot), and video levels.

28. Ripple filtering.

29. Horizontal and vertical deflection units.

30. Power, raster, front panel lights and vertical positioning, and character intensity.

31. Intensity circuitry, beam current circuitry, high-voltage circuitry, front panel control circuitry, and keyboard circuitry.

32. *a.* Zero reference–establishes a base level for circuit operation.
    b. Gain control–establishes the gain of the circuitry.
    c. Amplitude control–controls output amplitude of circuitry (character height).
    d. Position control–controls the position of the display (character) on the CRT screen.

33. Electronic and mechanical actions working together to produce a product.

34. The objective is to have all circuitry function so that a change voltage input causes a rotation to a new null. Further, once at the null, the unit rests and does not *hunt*.

35. Input circuitry (transformer).

36. Yes. A change voltage derived from some source and after adjustment must be fed to the servo for repositioning.

37. An ohmmeter, a DC meter, an AC (RMS) meter, and an oscilloscope.

38. All three require an energized coil.

39. (1) Depressing space on the keyboard.
    (2) Automatic sensing of the end-of-print cycle.

40. Alignment of interrelated assemblies is as follows:

    (1) Space armature and shaft end play (parallel).
    (2) Space bail (serial).
    (3) Space pawl rack clearance (serial).
    (4) Space pawl stop plate (serial).
    (5) Space magnet (serial).
    (6) Space pawl clearance (serial).

41. Those that can receive, store, and provide data, and those that can only provide data (read only).

42. Timing, addressing, interface circuitry, read logic, and memory device.

43. The flip-flop.

44. (1) Serial-to-parallel and parallel-to-serial conversion circuitry.
    (2) Speed reduction or increase from audio to megahertz rates or reverse.
    (3) Time sharing for multichannel operation.

45. (1) Priority system through manual or automatic programming.
    (2) Cyclic operation through ring counters, etc.

46. Dipole, frequency shift keying, and frequency shift modulation.

47. Too high a setting results in noise amplification along with data, and this invalidates the real data.

CHAPTER 4

1. To insure system integrity; i.e., to locate any existing or impending failure.

2. It must attempt to treat all circuits in a manner which approximates the ultimate applications of the computer.

3. The two basic classes of automatic computers are special–purpose and general-purpose.

4. The wired-in logic which controls the automatic functions of a computer is classified as system hardware.

5. Fault detection and fault isolation.

6. The design of maintenance programs is based on the particular system's hardware, its function, and the type of task the program must perform; i.e., detect and/or isolate failures.

7. Catastrophic, intermittent, and machine state.

8. Start small, start big, marginal checking, multiple clue approach, and process of elimination.

9. It stresses fault detection and generally minimizes isolation.

10. The program writeup would be checked to determine where to insert an unconditional branch instruction. The address portion of the branch instruction must contain the address (as determined from the writeups) of an instruction located at the beginning of the test routine.

11. Normally this testing is (performed) by storing the address of each memory location into its respective memory location. Once the entire memory is loaded, a read and compare process of each memory address is performed.

12. Self-control oriented.

13. A package of control and helper routines that facilitates the loading and operation of the various maintenance program routines.

14. Interrupts, manual intervention, and printouts.

15. Program heading, results of program run, error information (data failure, control failures, etc.), and indicated repair statements.

16. It identifies that a margin failure using margin word 005 occurred. Also, it identifies the failure as being within marginal group 4, circuit line selection E2, and marginal voltage +150 volts. Further, it identifies that the failure occurred at the prescribed margin of -40 volts while cycling test routine 2.

17. The CONTROL WD would contain: 74.

18. Basically, the descriptors are used to set up, initiate, control, and terminate data transfers between core memory and the terminal devices.

19. SW4.

20. It is used with a functional card group table (located in the appropriate TO) to determine the cards to be changed in correcting a detected malfunction.

CHAPTER 5

1. Fault indicators, system and unit testers, performance test standards, diagnostic programs, flow diagrams, and specialized test equipment.

2. Elimination of some possible sources of trouble, and locating or isolating the troublesome component.

3. The repair function validates the findings of the analysis and testing phases of the procedures.

4. Boolean algebra is a form of logic that uses mathematical symbols to describe logical processes. Troubleshooting with boolean algebra usually involves the development and use of a boolean equation or truth table.

5. Input to output.

6. To retain circuit integrity.

7. No. Generally the troubleshooting use of an equation requires starting at the output and working back to the input.

8. A truth table is a listing in table form of all possible combinations of input signals which can produce an output.

9. Checks of all elements previously validated that the function was performing properly. Only when an XY of a "1" with a carry of "1" are present does gate 6 provide any control over the output. When its results were measured and found to be incorrect, the correct diagnosis was a failing gate 6.

10. The approach uses a process whereby fault location is localized to a function, then to a subelement within the function.

11. The block diagram approach.

12. The method requires localizing the trouble to either half of the circuits or function by measuring the final output and the output of the midpoint. This localizes the problem to either half, thereby "split halving" the area of trouble.

13. Check waveforms and voltages. The other four items are primarily research in nature and are used in obtaining data about the problem.

14. (1) To analyze data content.
    (2) To determine if a waveform meets the prescribed specifications.

15. It is stored, altered, routed, processed, controlled, and displayed by the computer system.

16. As printout products, displays, mechanical readouts, and automatic functions of console units.

17. 3.

18. 20.

19. Time sharing.

20. In frequency modulation, the intelligence or data is algebraically summed with the carrier frequency, in amplitude modulation, the intelligence on data is added to the carrier frequency, causing an amplification in peak-to-peak voltage.

21. *a.* 28,875 ft.
    b. 3850 mph.

22. Zero volts.

23. Before the fact troubleshooting is a study, using all available resources, which forms ideas, opinions, and procedures to isolate a problem in equipment.

24. The fact that it generates and distributes the pulses that affect the core.

25. (1) Pulse width and PRT, and waveform.
    (2) Card or cards used in its generation.
    (3) Types of circuits involved.
    (4) Purpose and position of occurrence of the signal.
    (5) Expected results if the signal fails.

26. You would look for pulses out of specifications in pulse width, amplitude, duration, and form.

27. He identified that the problem was not caused by front panel controls, then he collected the alignment data and identified which controls could affect the retrace. Finally, he identified the cards and located the specifications.

28. After a local diagnostic fails to pinpoint the exact trouble area, and analysis of the printout cannot lead to further tests, opinions, or questions, then looping of data or forcing data while point-to-point oscilloscope measuring is performed.

29. (1) To identify a failing function or subfunction.
(2) To identify correct or incorrect data flow.

30. Operation or failure of the circuits must be related directly to the remote indicator.

31. They portray: operations of counters, information in memory, fault indications, status of each part of a system, and an entire system.

32. Service manuals (–2 series) and circuits and diagrams manuals (–3 series).

33. Only one-half of a card group up to a maximum of seven cards may be exchanged at one time.

34. Grouping of cards into functional areas (alarm groups), identifying the card location, type of card, and name of function.

35. Diagnostic printout frequently lists the card group to replace.

STOP– **1. MATCH ANSWER SHEET TO THIS EXERCISE NUMBER.** **2. USE NUMBER 1 PENCIL.**

30554 02 21

VOLUME REVIEW EXERCISE

Carefully read the following:

DO'S:

1. Check the "course," "volume," and "form" numbers from the answer sheet address tab against the "VRE answer sheet identification number" in the righthand column of the shipping list. If numbers do not match, take action to return the answer sheet and the shipping list to ECI immediately with a note of explanation.
2. Note that numerical sequence on answer sheet alternates across from column to column.
3. Use only medium sharp #1 black lead pencil for marking answer sheet.
4. Circle the correct answer in this test booklet. After you are sure of your answers, transfer them to the answer sheet. If you *have* to change an answer on the answer sheet, be sure that the erasure is complete. Use a clean eraser. But try to avoid any erasure on the answer sheet if at all possible.
5. Take action to return entire answer sheet to ECI.
6. Keep Volume Review Exercise booklet for review and reference.
7. If *mandatorily* enrolled student, process questions or comments through your unit trainer or OJT supervisor.
   If *voluntarily* enrolled student, send questions or comments to ECI on ECI Form 17.

DON'TS:

1. Don't use answer sheets other than one furnished specifically for each review exercise.
2. Don't mark on the answer sheet except to fill in marking blocks. Double marks or excessive markings which overflow marking blocks will register as errors.
3. Don't fold, spindle, staple, tape, or mutilate the answer sheet.
4. Don't use ink or any marking other than with a #1 black lead pencil.

NOTE: TEXT PAGE REFERENCES ARE USED ON THE VOLUME REVIEW EXERCISE. In parenthesis after each item number on the VRE is the *Text Page Number* where the answer to that item can be located. When answering the items on the VRE, refer to the *Text Pages* indicated by these *Numbers*. The VRE results will be sent to you on a postcard which will list the *actual VRE items you missed*. Go to the VRE booklet and locate the *Text Page Numbers* for the items missed. Go to the text and carefully review the areas covered by these references. Review the entire VRE again before you take the closed-book Course Examination.

Note to Student. This Volume Review Exercise contains 89 four-option items and 1 three-option item.

Multiple Choice

Chapter 1

1. (003–004) The use of the *north mark*, either true or magnetic, is required for orientation of

   a. height radars, but not search.
   b. search radars, but not height.
   c. both height and search.
   d. neither height nor search radars, but beacon.

2. (004) The encoder function of the keyboard described in the text is used to

   a. convert serial input data to parallel.
   b. convert seven parallel lines to voltage levels of ONES and ZEROS.
   c. generate an 8-bit data code.
   d. insert an 8-bit binary code into a transmitter each time a key is depressed.

3. (004–005) Since the keyboard discussed in the text is required to produce a binary code, you can expect that performance tests would examine all of the following *except*

   a. its capability to generate data.
   b. manual operation and mechanical conversion to electrical quantity.
   c. alignment of the levers and cams.
   d. reproduction of a character when a key is depressed.

4. (005–006) Performance requirements which may be performed on a keyboard unit usually require all of the following tests *except*

   a. operation of the internal elements of the unit.
   b. proper passing of data through interface units.
   c. control of transmission of data to output media.
   d. proper error indication if the unit is operated incorrectly.

5. (008) Of the following listed items which are in tape units, select the one which would most probably require a daily check.

   a. Reel assemblies.
   b. Vacuum pump.
   c. Tape head positioning.
   d. Tape tension.

6. (008–009) If a high-speed data rate of transmission is required, which of the following requirements would be most essential?

   a. Low-gain high-quality amplifiers are needed in repeater station circuitry.
   b. Signal loss is low, therefore linear amplifiers provide the best gain and minimize data loss.
   c. Noise-free lines on the audio transmission portion of the line must be used.
   d. Dipole data transfer would be used in preference to frequency-shift keying.

7. (009) If an input line to a communication control is monitored by a meter and the known standard is a range of 6 to 13 db, what would the meter read if a line loss of 90 percent were being measured?

   a. –4 to 1.3 db.
   b. –4 to 3 db.
   c. –.4 to 1.3 db.
   d. 16 to 19 db.

8. (009–010) Which one of the following checks made on printers would provide the most reliable results?

   a. Visual examination of all moving parts, examining for wear and tear.
   b. Measurement of power to determine accuracy of circuit operation.
   c. Operation of the unit to make it produce a copy.
   d. Measurement of tolerances of mechanical assembly parts, i.e., cams, gears, spaces, against a specification.

9. (010–012) A performance check of a CRT display unit (console) would probably have visual elements to examine. Select from the following groupings of elements those which would fall in this category.

   a. Range mark separation, retrace purity, and sweep linearity.
   b. High voltage and unblanking.
   c. Video levels, DID data, and control switches.
   d. Timing generation, symbol shaping, and focus.

10. (012) A byproduct of a performance check made on a central processor unit is that the

    a. timing is validated.
    b. power supply voltages are measured.
    c. lamp circuitry is exercised.
    d. environmental conditions are checked.

11. (014) On which of the following parts of a system may performance checking require an AC voltmeter?

    a. CRT display.
    b. Line data circuitry.
    c. Direct-current power supply.
    d. Reference voltage.

12. (015) If a performance check were accomplished using an oscilloscope, which of the following units would have checks made on pulse width and linearity of signals?

    a. Line data circuitry.
    b. CRT displays circuitry.
    c. Servo unit circuitry.
    d. Radar data processing circuitry.

13. (016) The purpose for a peaking adjustment instruction in a performance routine might be to

    a. alter the DC operating level of a video amplifier.
    b. amplify weak radar returns.
    c. alter pulse width of a square-wave generator.
    d. alter the bias level of a collector or emitter circuit in a quantizer.

14. (018) From the following list, select the unit which would *least* likely be checked with a printout.

    a. Electrographic printer.
    b. Central data processor.
    c. Line data circuitry.
    d. Impact printer.

15. (018) Select from the following list the type of data *least* likely to have lamp indications verify its existence.

    a. Line data.
    b. Tape data.
    c. Central computer data.
    d. Radar return data.

Chapter 2

16. (020) According to the text, which of the following definitions is correct?

    a. Adjustment is the act of altering an element.
    b. Adjustment is the act of bringing into line.
    c. Alignment is the act of altering an element.
    d. Alignment is the act of providing a variable component change to a circuit.

17. (020) Select the reason from the following list which is *not* a regulatory use of a variable control.

    a. Provide a change in frequency.
    b. Cause an increase in bias voltage.
    c. Frequency shift an incoming signal.
    d. Increase the gain capabilities of the circuit design.

18. (021) Trimmer capacitors used in computer systems most frequently are

    a. linear.
    b. nonlinear.
    c. variable by altering the dielectric material.
    d. manufactured with the rotor contained between two sets of stator plates.

19. (02[illegible]) What is the difference, if any, between a tubular capacitor and a button type?

    a. There is no difference.
    b. The tubular capacitors have a life cycle expectancy of 250 turns.
    c. More critical adjustments can be made with a tubular capacitor.
    d. The life turns cycle of a button type exceeds the tubular type by four times.

20. (022) What characteristic is included in the manufacture of most potentiometers that make it possible to use a metal screwdriver when making adjustments?

    a. The slider arm is connected to the center terminal.
    b. The turning screw is isolated from the slider shaft.
    c. Epoxy resin material is used to secure the turning screw.
    d. The resistive element is insensitive to the additional metal conductor of the screwdriver and therefore no signal attenuation can result.

21. (025–026) When variable components are installed in amplifier or pulse generator circuits, they provide all of the following capabilities. Select the one option which is *least* common.

    a. Alter the gain ratio of the circuit.
    b. Act as a phase-shifting device.
    c. Control the pulse duration.
    d. Attenuate input line signals.

22. (026) In order for an operational amplifier to have an increase in gain at its output, which of the following conditions must be met?

    a. The feedback resistor must be made smaller.
    b. The input resistor must be made larger.
    c. The feedback resistor must be made larger.
    d. A low-gain amplifier must be installed.

23. (027) A pulse generator is usually called by all of the following names *except*

    a. one-shot MV.
    b. single-shot MV.
    c. monostable MV.
    d. bistable MV.

24. (027) The method most frequently employed in pulse generators for altering the output pulse width is

    a. changing clamping levels.
    b. triggering the circuit more frequently.
    c. triggering the circuit less frequently.
    d. altering the RC time constant of the circuit.

25. (027) What function, if any, can the slope of an input signal provide for a pulse generator?

    a. A delay to the start of the circuit.
    b. No effect.
    c. Alter the output pulse width of the circuit.
    d. Alter the RC time constant of the circuit.

26. (028) The instruction "adjust power supply control R10 for 24V ± .001V output" indicates which type of meter should be used?

    a. Frequency meter.
    b. DC voltmeter, model PSM6 or 7.
    c. Differential voltmeter.
    d. AC voltmeter.

27. (029) High-voltage adjustment controls frequently are connected with one end to ground and the other connected

a. internally to a plus terminal.
b. internally as a rheostat.
c. externally with the end left unconnected.
d. externally with the end connected to a negative or positive source voltage.

28. (029) What component do most of the computer systems timing generators have in common?

a. Adjustable capacitors.
b. Crystals.
c. Wire-wound resistors.
d. 5-watt resistors.

29. (030) In addition to the master timing unit, all of the following units are frequently used for timing control *except*

a. free-running oscillators.
b. blocking oscillators.
c. automatic gate length generators.
d. amplitude control circuits.

30. (032) Select from the following list the type of memory which does *not* have mechanical adjustment associated with it.

a. Core.
b. Drum.
c. Disk.
d. Tape.

31. (032) Mechanical adjustments in a tape storage system vary according to the design of the unit. However, they have at least four common elements; the proper drive speed and three of those in the following list. Select the element which is *not* in common with the others.

a. Stop.
b. Start.
c. Tension.
d. Tape placement.

32. (034) Most memory systems use potentiometers to establish the proper current amplitudes. These pots are frequently found in

a. core units.
b. read/write heads.
c. read/write amplifiers.
d. inhibit amplifiers.

33. (035) The potentiometers used in storage tube adjustments control all of the following items *except*

a. scanning.
b. flood gun intensity.
c. unblanking.
d. frequency compensation.

Chapter 3

34. (039) The first step in the study of an alignment is to identify the objective. Select from the responses the one which *best* describes this purpose.

a. Understand the title.
b. Identify the area, i.e., assembly, function.
c. Relate the operational performance to intermediate functions.
d. Determine its functional operation and relationship to functional and system operation.

35. (040) The use of electronic principles as applied to identification of the objective of an alignment is to identify

a. components.
b. operational circuits.
c. variable component operation.
d. characteristic signal development by circuit design.

36. (041) What characteristic of the data accumulated in the phase of a study in alignments titled "Subunits, circuits, components of the objectives" provides the clearest understanding of what knowledge and work are required?

a. Identifying the alphanumerics of the assemblies in the alignments.
b. Identifying the titles, parameters, and purposes of the circuits involved.
c. Locating the circuits and assemblies in the various technical orders.
d. Placing the circuit or assemblies in a line showing processing.

37. (041) In which one of the listed items would detailed specifications of parameters be must useful and significant during the study of an alignment?

a. An integrated circuit 10-stage buffer.
b. A collector bias-controlled operational amplifier.
c. A resistive voltage divider.
d. A free-running oscillator.

38. (045) While performing a study of an alignment as described in the text, how can a step in the sequence be bypassed?

a. It can be eliminated by research of the alignment to determine its nonexistence.
b. Any step that is identified in the prerequisite of an alignment can be eliminated.
c. A clear title can eliminate need for step 1.
d. If only serial paths are used, the sequencing step (4) may be eliminated.

39. (046) Of the four units making a console–the timing, intensity, vertical, and horizontal–which is usually aligned first?

a. Intensity.
b. Timing.
c. Horizontal.
d. Vertical.

40. (046) From the four units listed, select the one which, when properly aligned, controls the illumination of the CRT.

a. Turning.
b. Intensity.
c. Vertical deflection.
d. Horizontal deflection.

41. (046–047) After studying the requirements for statistical display circuitry and associated alignments, linearity alignment of maps, symbols, and alphanumerics is a function of

a. intensity.
b. blanking and unblanking.
c. timing.
d. deflection

42. (047) The complexity and extent of alignments on DID units depend for the most part on the type of which of the following items?

a. CRT.
b. Symbol generators.
c. Vector generators.
d. Decoding circuity.

43. (047) In aligning a DID unit, which uses a charactron tube, the instructions would include alignment of deflection

a. plates for character positioning.
b. plates for character selection and positioning.
c. coil for character positioning.
d. coil for character positioning and plates for character selection.

44. (047) The two different types of hard-wired matrix assemblies used with DIDs are the stencil plates and the

a. core.
b. tape.
c. read only memory.
d. thin film.

45. (048) Patch panel programming usually provides

a. target outlines.
b. maps of states, countries, and elevation.
c. alphanumerics of targets.
d. beacon responses.

46. (048–049) The range position of target positioning alignment routines on surveillance consoles is a function of

a. timing.
b. deflection.
c. intensity.
d. high voltage.

47. (050) Sweep circuit alignment is often performed to bring sweep voltage amplitudes to specification as well as three of the four following selections. Select the item *not* often performed while aligning sweep circuits.

a. Pulse duration.
b. Slope angle.
c. Proper signal phasing.
d. Video gate adjustments.

48. (050) Prerequisites to aligning sweep circuits in a console usually require verification

a. of timing waveforms because errors alter duty cycles.
b. controlling and combining (time share) circuits.
c. trimmers used in the sweep circuitry.
d. of centering alignment usually performed on coupler units.

49. (050) The trimmer capacitors incorporated in intensity units are used for

a. DC level control of gates.
b. squaring leading edges of gates.
c. amplification of gates.
d. controlling basic turn-on voltages for the CRT.

50. (050) Intensity/unblanking and high-voltage alignments include all the following requirements *except*

a. pulse width.
b. pulse shaping.
c. data.
d. amplitude.

51. (052) Servos operate on a principle of

a. rate feedback.
b. summing a feedback voltage with an input signal.
c. amplifying a difference signal to drive the motor to a position which produces a null to the input unit.
d. a 180° signal feedback summed with a 0° input of the same frequency and the motor drive until both signals are of the same magnitude.

52. (053) Direction of rotation in a servo unit is the product of the

a. motor.
b. phase relationship between signals and reference voltage.
c. phase relationship between signals and reference windings.
d. relationship of phase of input signal and feedback signal.

53. (055–056) What portion of the spacing theory is essential to accomplishment of the alignment performed on the keyboard printer punch carriage unit? The fact that

a. two hammers must trip.
b. clearances must be preset.
c. coil must be energized to perform the alignment.
d. rack is spring-loaded to the left.

54. (056) If the adjustable time cycle for movement of the carriage on a KPP were too short, what alignment could a repairman be falsely led to believe would correct the problem?

a. Space coil-to-armature positioning.
b. Space pawl and carriage clearance.
c. Space pawl and carriage stop plate.

Note to Student. Consider the following information for items 55 and 56: The text classes different types of memory units according to their capabilities.

55. (057) From the following lists, select the type which does *not* belong in the class with the other three.

a. Storage tube.
b. Disks.
c. CROS.
d. TROS.

56. (057) From the following lists, select the type which does *not* belong in the class with the other three.

a. Drums.
b. Integrated (program memory) circuit.
c. Delay line.
d. Core

57. (057) The difference in requirements for a class 2 (ROM) memory device and those for a class 1 unit is that class 2 units do not use

a. addressing circuitry.
b. erase control circuitry.
c. interface circuitry.
d. a storage media.

58. (057–058) Circuits combined to form counters which are used as memory address circuitry usually include all of the following *except*

a. integrated circuits (chips).
b. flip-flops.
c. AND gates.
d. transistor circuits.

Chapter 4

59. (063) Maintenance programs perform their function by

a. the application of AC margins to circuitry.
b. the application of DC margins to circuitry.
c. treating all circuits in a manner which approximates the computer's static operation.
d. treating all circuits in a manner with approximates the ultimate applications of the computer.

60. (063) The primary function of a maintenance program is to

a. insure system integrity.
b. identify failing components.
c. identify marginal failures.
d. insure equipment maintainability.

61. (063) The two basic classes of automatic computers are the

a. active and standby.
b. on-line and backup.
c. special and general.
d. reliability and diagnostic.

62. (063) The wired-in logic which controls the automatic function of a computer is classified as

a. system hardware.
b. system software.
c. logic components.
d. peripheral components.

63. (064) In marginal checking, the amount of variation necessary to make a component malfunction indicates which of the following concerning a computer component?

a. Age.
b. Reliability.
c. Flexibility.
d. Type of component.

64. (067) When all other techniques have failed, what should you do to isolate an intermittent failure?

a. Replace all components in the failing area.
b. Call in contractor personnel to troubleshoot the failure.
c. Loop the failing test routine while scoping the circuits.
d. Drop all power and make resistance checks of components within the failing area.

65. (068) What operation cannot be performed when a magnetic tape unit is file protected?

a. Read.
b. Write.
c. Rewind.
d. Backspace.

66. (070) Flow chart symbols

a. do not use functional notations.
b. may change from system to system.
c. do not contain descriptions of computational functions.
d. require direction of flow indicators if the direction of flow is top to bottom.

67. (070) A maintenance control program

a. is only associated with an on-line environment.
b. contains a separate print control routine for each test routine.
c. combines common programming requirements of the various test routines.
d. does not contain any provisions for interrupts.

68. (071) Which one of the following is *not* a form of the more standardized types of operator communication as pertains to programs?

a. Branches.
b. Interrupts.
c. Printouts.
d. Manual interventions.

69. (071) Which one of the following is considered essential to the standardization of the maintenance programs within a computer system?

a. Time duration of the program run.
b. Uniformity of the program printout.
c. Number of instructions per program.
d. Number of margins applied per program.

Chapter 5

70. (077) Which one of the following is the most important step of any troubleshooting effort?

a. Think before you act.
b. Know your test equipment.
c. Work on each problem alone.
d. Use a general troubleshooting procedure.

71. (077) Identify the military standard that computer manufacturers are required to use for symbology uniformity.

a. MIL–STD–803B.
b. MIL–STD–804B.
c. MIL–STD–805B.
d. MIL–STD–806B.

72. (079) In boolean algebra, logical conditions are called variables, and they are represented by

a. letters.
b. numbers.
c. symbols.
d. exponents.

73. (079) When one OR gate supplies an AND gate, what sign of grouping, if any, is required?

a. Parentheses.
b. Brackets.
c. Braces.
d. None.

74. (079) The writing of an equation for a logic diagram is begun by writing the output of

a. the total diagram.
b. the input gate or gates.
c. one branch from the output gate.
d. either the output or input gate or gates.

75. (079) In boolean algebra, what function does the + sign represent?

a. AND.
b. NOR.
c. NOT.
d. OR.

76. (080) In the boolean equation A + B = X, there are how many possible numerical combinations?

a. 1.
b. 2.
c. 4.
d. 8.

77. (081) What is another name for the functional area approach to troubleshooting?

a. Truth table approach.
b. Block diagram approach.
c. Signal injection approach.
d. Schematic diagram approach.

78. (083) If a left shift pulse is applied to a five-stage register containing the binary confiuration 01010 (LSD on right), what will its contents be after the shift? (Answers are in decimal notation.)

a. 5.
b. 10.
c. 15.
d. 20.

79. (083) If a right shift pulse is applied to a ten-stage register containing the binary configuration 0111100100 (LSD on right), what will its contents be after the shift? (Answers are in decimal notation.)

a. 121.
b. 242.
c. 484.
d. 968.

80. (089) If the multiple input gates to a buffer or a comparator fail, the most probable cause could be

a. a transistor that has shorted between the junctions.
b. an open or shorted diode.
c. a flip-flop stuck in the one state.
d. an open relay.

81. (089 090) What is the function of the read signal in the control unit?

   a. Control the generation of the sense and inhibit.
   b. Cause all the cores to reset to zero when converted to a current pulse.
   c. Data stored in buffer will be loaded into core.
   d. Error light will come on because core data and input data compare.

82. (091) Which of the following conditions, if any, could be a warning to signal failure?

   a. Signal absence.
   b. Signal deterioration.
   c. Intermittent signal.
   d. None of the preceding.

83. (092) When does retrace occur?

   a. Beginning of the sweep cycle.
   b. End of the sweep cycle.
   c. 180° from the middle of the previous cycle.
   d. Middle of the sweep cycle.

84. (092) All of the following options should be considered before troubleshooting a blanking/unblanking circuit with an oscilloscope *except* determining

   a. which cards are involved.
   b. which controls are involved.
   c. which alignment will correct the problem.
   d. if the work can be accomplished on line.

85. (092) What should first be done when a failure occurs while the computer is cycling?

   a. Perform a PMI.
   b. Troubleshoot with the oscilloscope.
   c. Run the diagnostics.
   d. Turn the computer off.

86. (093) Interpreting the diagnostic may

   a. pinpoint the exact circuit.
   b. identify the exact card or card group.
   c. isolate the malfunction to a specific component.
   d. analyze the circuit function.

87. (093) Fault location indicators are used to identify each of the following *except*

   a. correct data flow.
   b. failing functions.
   c. failing subfunctions.
   d. the failing circuit component.

88. (097) The best way to simplify a repairman's job of troubleshooting is to

a. remove the printed circuit cards one by one until the fault is isolated.
b. utilize the system TO which contains fault information.
c. remove and replace the end item.
d. isolate the problem by troubleshooting with an oscilloscope.

89. (097) If a timing error were suspected on a system and you were using the "group removal and replacement troubleshooting technique," you should do all of the following *except*

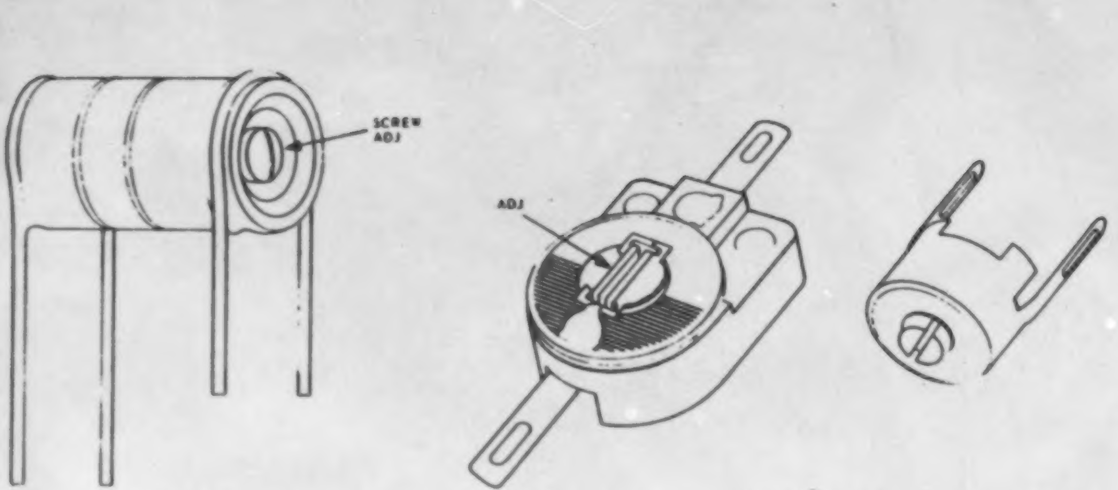
a. isolate the error to a certain card.
b. isolate the error to a certain group of cards.
c. isolate the error to a specific area.
d. identify the trouble symptom and list the cards to be removed.

90. (098) What is the main advantage of using the "group removal and replacement troubleshooting technique"?

a. Isolation of the problem to a specific cabinet.
b. Pinpointing the malfunction to a specific card.
c. Quick restoration of equipment.
d. A faster method of isolating the problem.

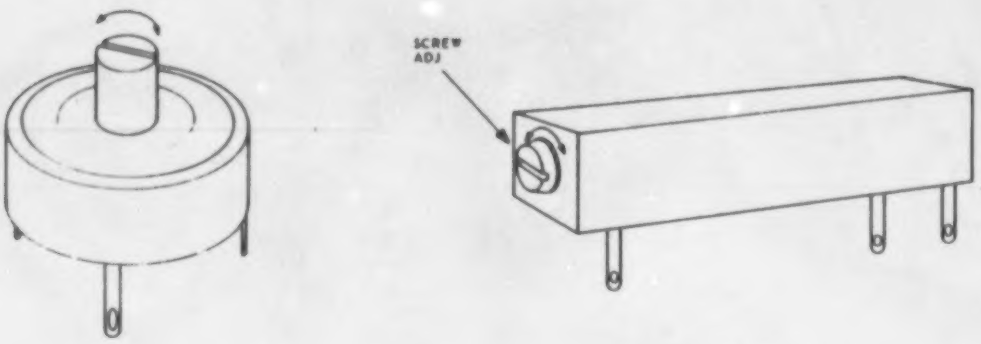
UNITS DEVICES	LINE DATA	POWER SUPPLIES	CRT DISPLAYS	SERVO UNITS	RADAR DATA	CENTRAL PROCESSORS DATA	DIGITAL DATA DISPLAYS	ELECTROGRAPHIC PRINTERS	IMPACT PRINTERS	RADAR ANTENNA ORIENTATION	PARITY CIRCUITS	TAPE TRANSPORT UNITS	REFERENCE VOLTAGES
METERS 1. AC VOLT	✓	✓											
2. DC VOLT		✓											✓
3. DIFFERENTIAL		✓											✓
4. CURRENT		✓											
OSCILLOSCOPES DISPLAYS	✓		✓	✓	✓	✓				✓			
CRT DISPLAYS			✓			✓	✓			✓			
PRINTOUTS						✓		✓	✓				
LAMPS AND AUDIO ALARMS	✓	✓				✓					✓	✓	✓
VISUAL EXAM OF MECHANICAL ASSEMBLIES				✓				✓	✓			✓	

Figure 28. Completed DPC units and performance check devices.


SCREW
ADJ
ADJ

A
TABULAR TRIMMER

B
BUTTON TRIMMERS



C
POTENTIOMETER

D
POTENTIOMETER

Figure 29. Variable Components.

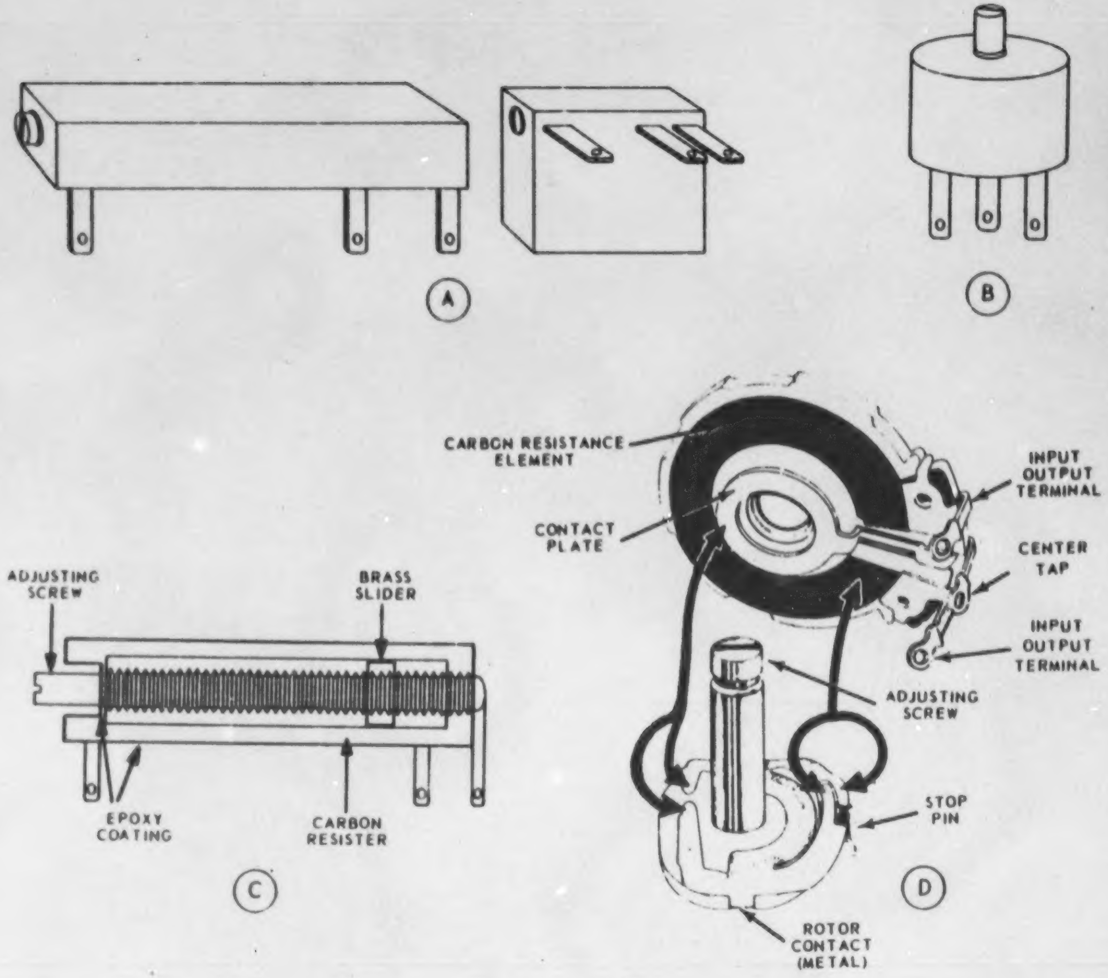

A
B
CARBON RESISTANCE ELEMENT
INPUT OUTPUT TERMINAL
CONTACT PLATE
CENTER TAP
INPUT OUTPUT TERMINAL
ADJUSTING SCREW
BRASS SLIDER
ADJUSTING SCREW
STOP PIN
EPOXY COATING
CARBON RESISTER
C
D
ROTOR CONTACT (METAL)

Figure 34. "Pots."

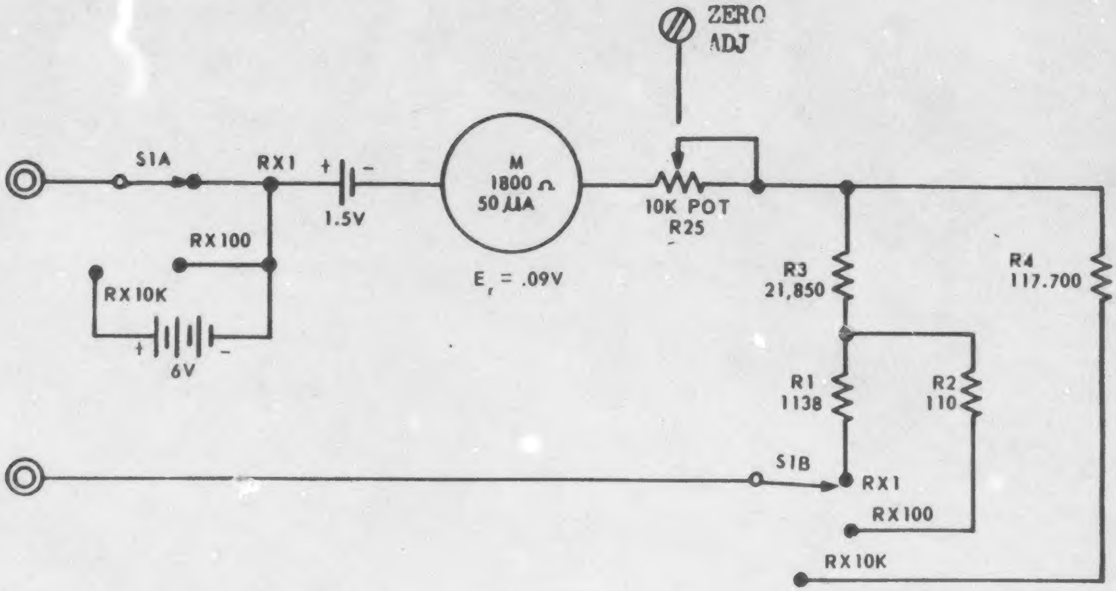

ZERO ADJ
S1A
RX1
+
−
1.5V
M
1800 Ω
50 µA
10K POT
R25
E_r = .09V
RX100
RX10K
+
6V
−
R3
21,850
R4
117.700
R1
1138
R2
110
S1B
RX1
RX100
RX10K

Figure 39. Meter zero adjust.

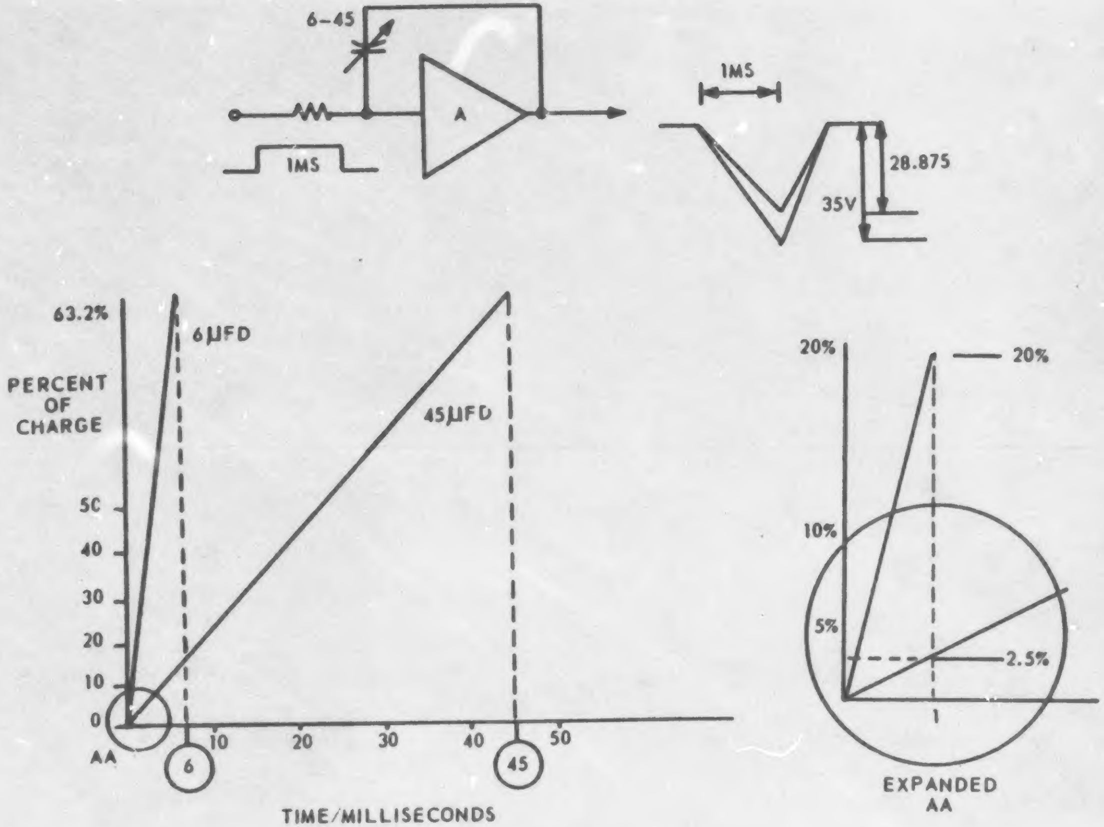

6-45
A
IMS
IMS
28.875
35V
63.2%
6µFD
PERCENT OF CHARGE
45µFD
5C
40
30
20
10
0
AA
10
20
30
40
50
6
45
TIME/MILLISECONDS
20%
20%
10%
5%
2.5%
1
EXPANDED AA

Figure 42. Miller circuit with variable capacitor.

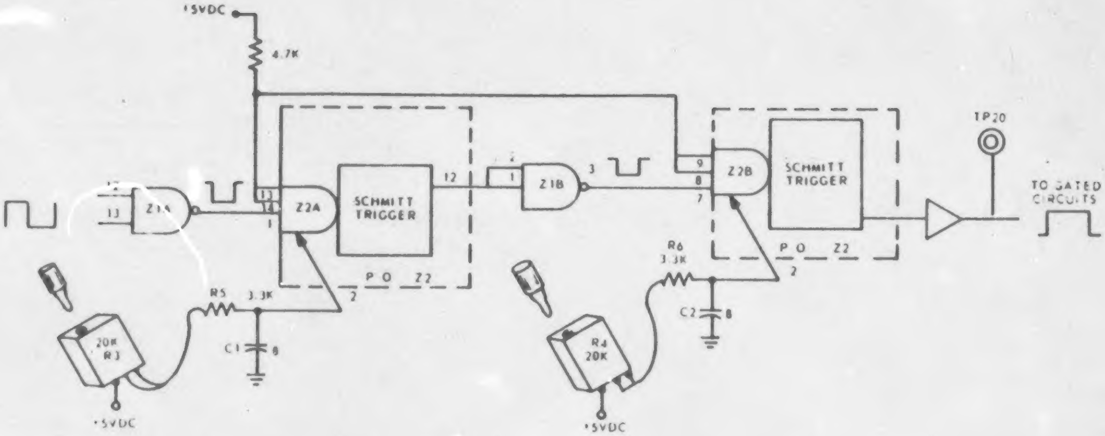

+5VDC
4.7K
12
13
Z1A
13
14
1
Z2A
SCHMITT TRIGGER
12
P O Z2
2
2
1
Z1B
3
9
8
7
Z2B
SCHMITT TRIGGER
P O Z2
2
TP20
TO GATED CIRCUITS
R5 3.3K
C1 8
20K R3
+5VDC
R6 3.3K
C2 8
R4 20K
+5VDC

Figure 43. Variable pulse-width generator (Schmitt trigger).

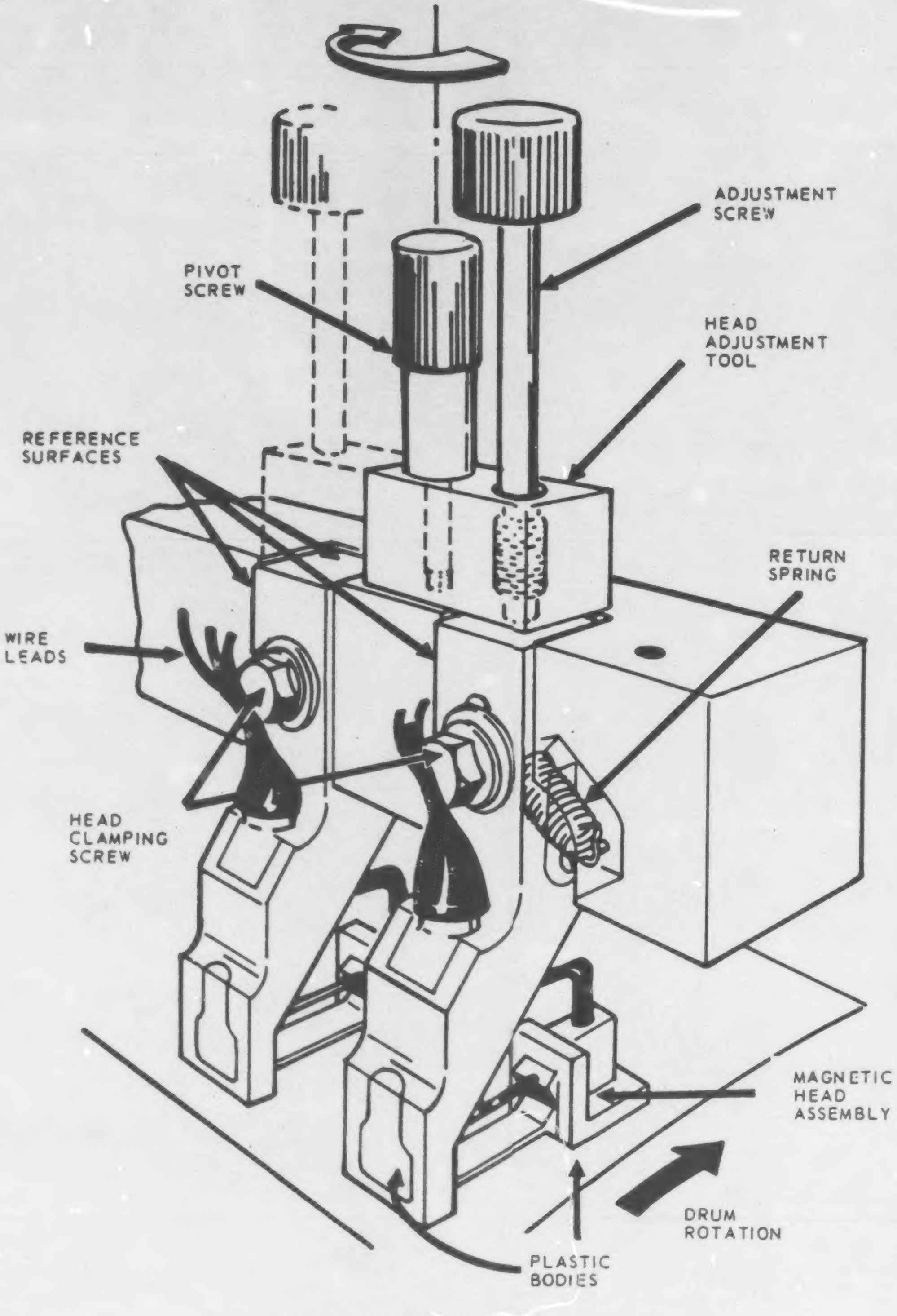

ADJUSTMENT SCREW
PIVOT SCREW
HEAD ADJUSTMENT TOOL
REFERENCE SURFACES
RETURN SPRING
WIRE LEADS
HEAD CLAMPING SCREW
MAGNETIC HEAD ASSEMBLY
DRUM ROTATION
PLASTIC BODIES

Figure 49 Magnetic head with adjustment tool installed.

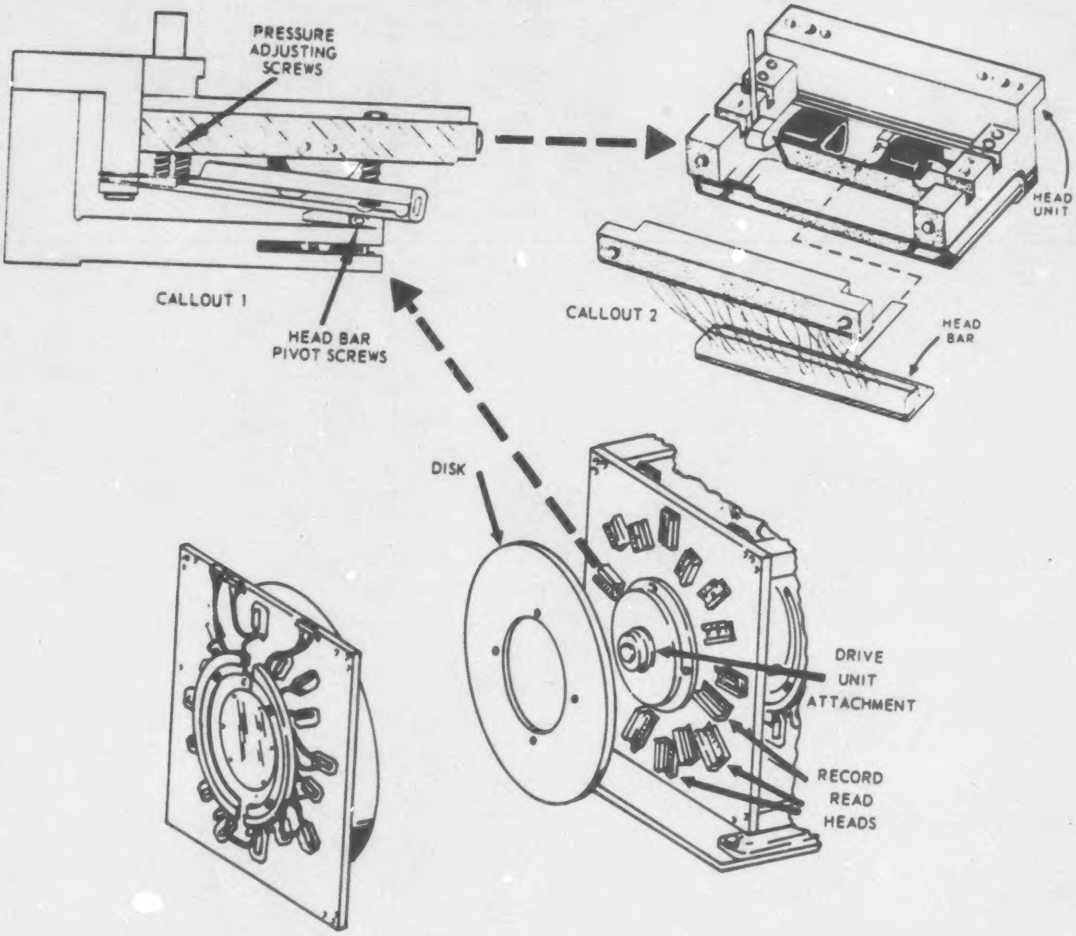

PRESSURE
ADJUSTING
SCREWS
HEAD
UNIT
CALLOUT 1
HEAD BAR
PIVOT SCREWS
CALLOUT 2
HEAD
BAR
DISK
DRIVE
UNIT
ATTACHMENT
RECORD
READ
HEADS

Figure 51. Disk memory.

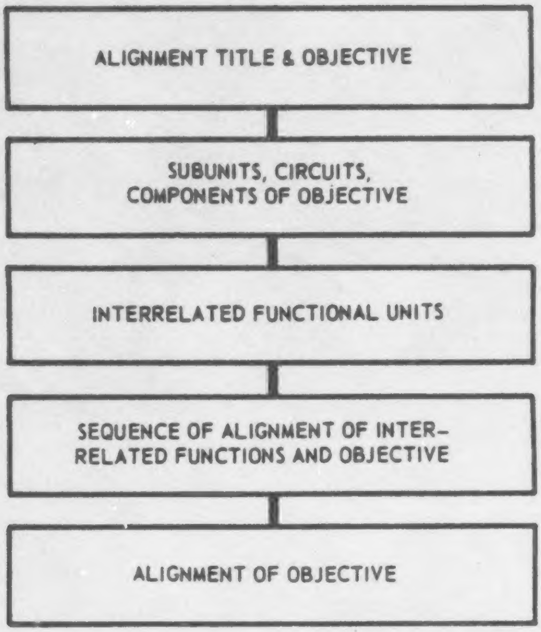

ALIGNMENT TITLE & OBJECTIVE
SUBUNITS, CIRCUITS, COMPONENTS OF OBJECTIVE
INTERRELATED FUNCTIONAL UNITS
SEQUENCE OF ALIGNMENT OF INTERRELATED FUNCTIONS AND OBJECTIVE
ALIGNMENT OF OBJECTIVE

Figure 58. Five divisions of an alignment study.

557

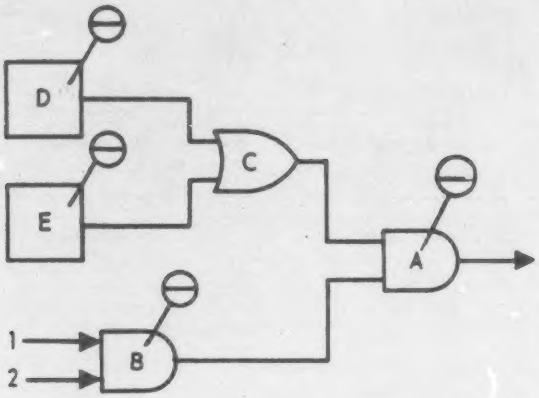


Figure 62. Functional alignment representation.

568

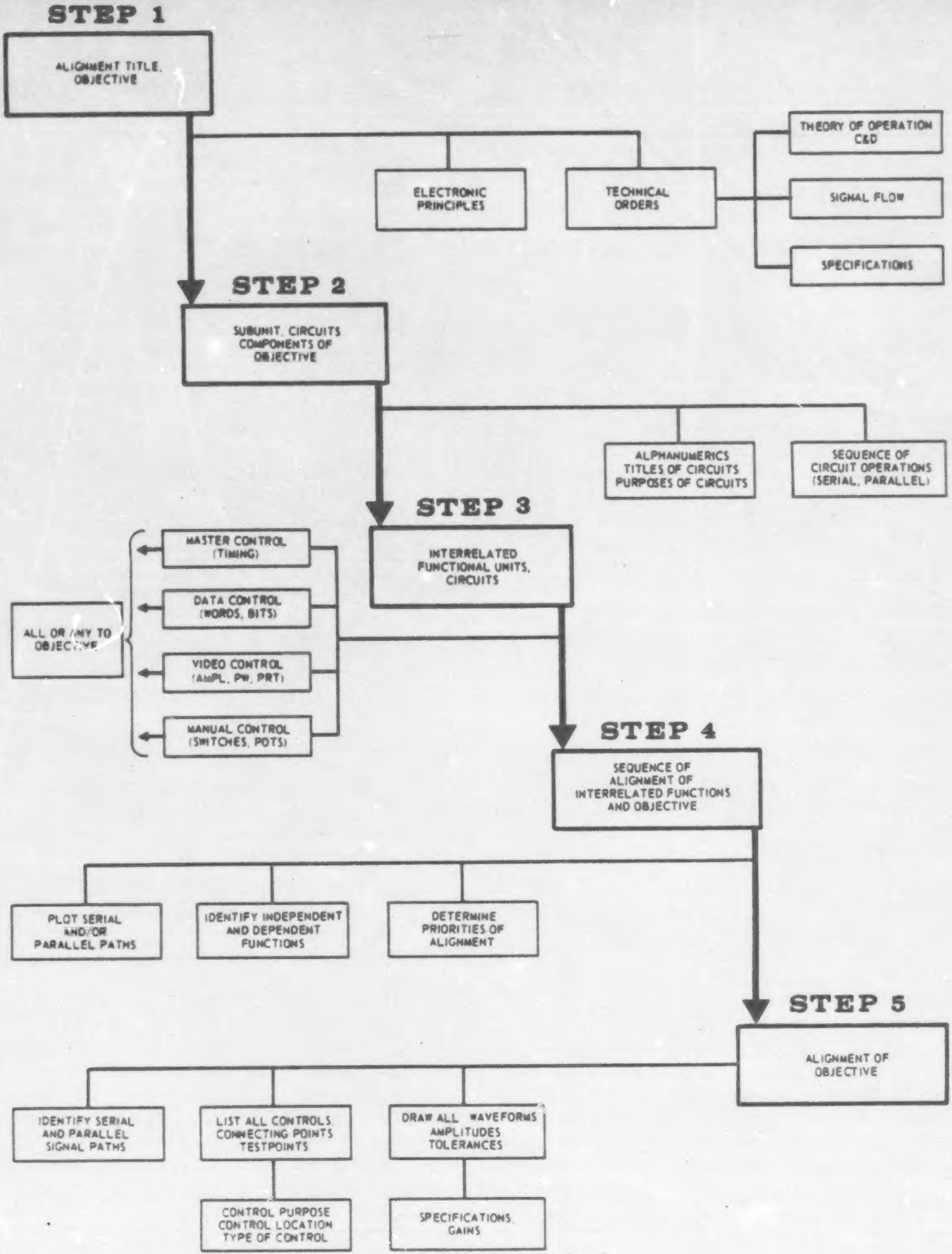

STEP 1
ALIGNMENT TITLE, OBJECTIVE
ELECTRONIC PRINCIPLES
TECHNICAL ORDERS
THEORY OF OPERATION C&D
SIGNAL FLOW
SPECIFICATIONS
STEP 2
SUBUNIT, CIRCUITS COMPONENTS OF OBJECTIVE
ALPHANUMERICS TITLES OF CIRCUITS PURPOSES OF CIRCUITS
SEQUENCE OF CIRCUIT OPERATIONS (SERIAL, PARALLEL)
STEP 3
INTERRELATED FUNCTIONAL UNITS, CIRCUITS
MASTER CONTROL (TIMING)
DATA CONTROL (WORDS, BITS)
VIDEO CONTROL (AMPL, PW, PRT)
MANUAL CONTROL (SWITCHES, POTS)
ALL OR ANY TO OBJECTIVE
STEP 4
SEQUENCE OF ALIGNMENT OF INTERRELATED FUNCTIONS AND OBJECTIVE
PLOT SERIAL AND/OR PARALLEL PATHS
IDENTIFY INDEPENDENT AND DEPENDENT FUNCTIONS
DETERMINE PRIORITIES OF ALIGNMENT
STEP 5
ALIGNMENT OF OBJECTIVE
IDENTIFY SERIAL AND PARALLEL SIGNAL PATHS
LIST ALL CONTROLS CONNECTING POINTS TESTPOINTS
DRAW ALL WAVEFORMS AMPLITUDES TOLERANCES
CONTROL PURPOSE CONTROL LOCATION TYPE OF CONTROL
SPECIFICATIONS, GAINS

Figure 66. Block diagram of study.

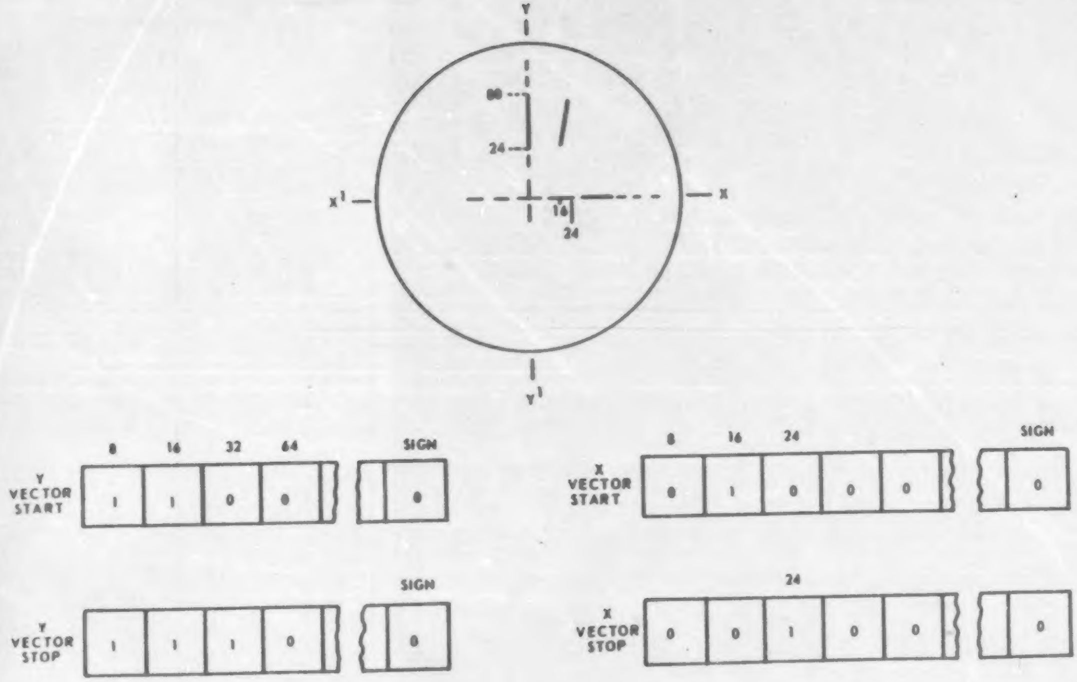

Y
80
24
X¹
X
16
24
Y¹
8
16
32
64
SIGN
Y VECTOR START
1
1
0
0
0
8
16
24
SIGN
X VECTOR START
0
1
0
0
0
0
SIGN
Y VECTOR STOP
1
1
1
0
0
24
X VECTOR STOP
0
0
1
0
0
0

Figure 68. Coordinate vector generator.

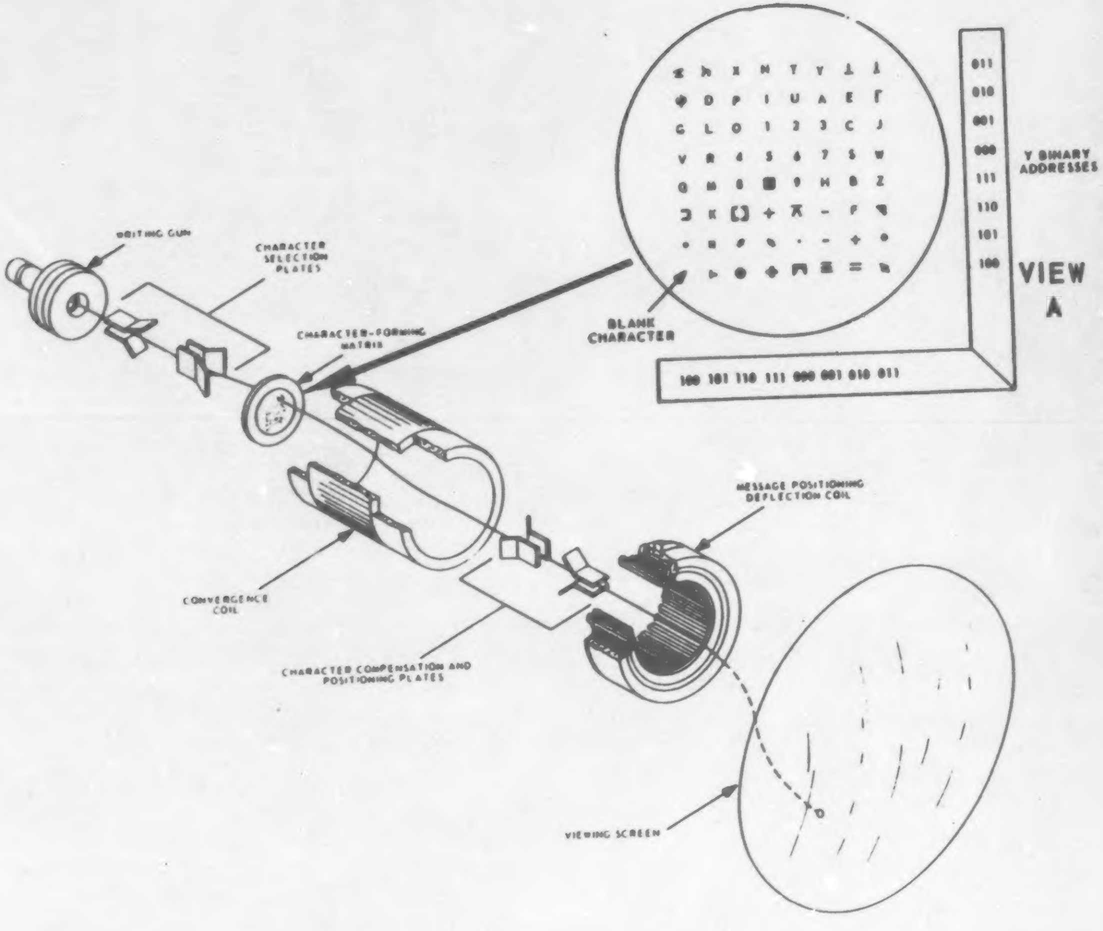

WRITING GUN
CHARACTER SELECTION PLATES
CHARACTER-FORMING MATRIX
D P I U A E
G L O 1 2 3 C J
V R 4 5 6 7 S W
BLANK CHARACTER
011
010
001
000
111
110
101
100
Y BINARY ADDRESSES
VIEW A
100 101 110 111 000 001 010 011
CONVERGENCE COIL
MESSAGE POSITIONING DEFLECTION COIL
CHARACTER COMPENSATION AND POSITIONING PLATES
VIEWING SCREEN

Figure 69. Charactron storage tube.

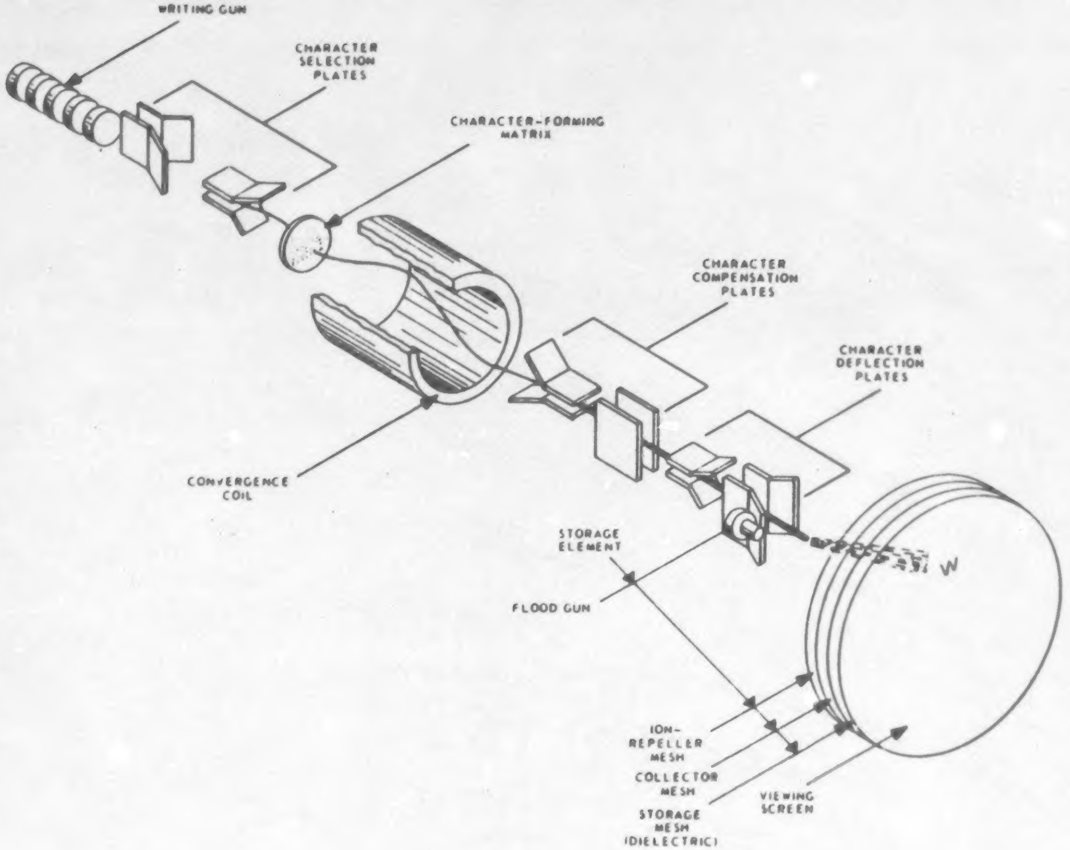

WRITING GUN
CHARACTER SELECTION PLATES
CHARACTER-FORMING MATRIX
CHARACTER COMPENSATION PLATES
CHARACTER DEFLECTION PLATES
CONVERGENCE COIL
STORAGE ELEMENT
FLOOD GUN
W
ION-REPELLER MESH
COLLECTOR MESH
STORAGE MESH (DIELECTRIC)
VIEWING SCREEN

Figure 70. Typotron storage tube.

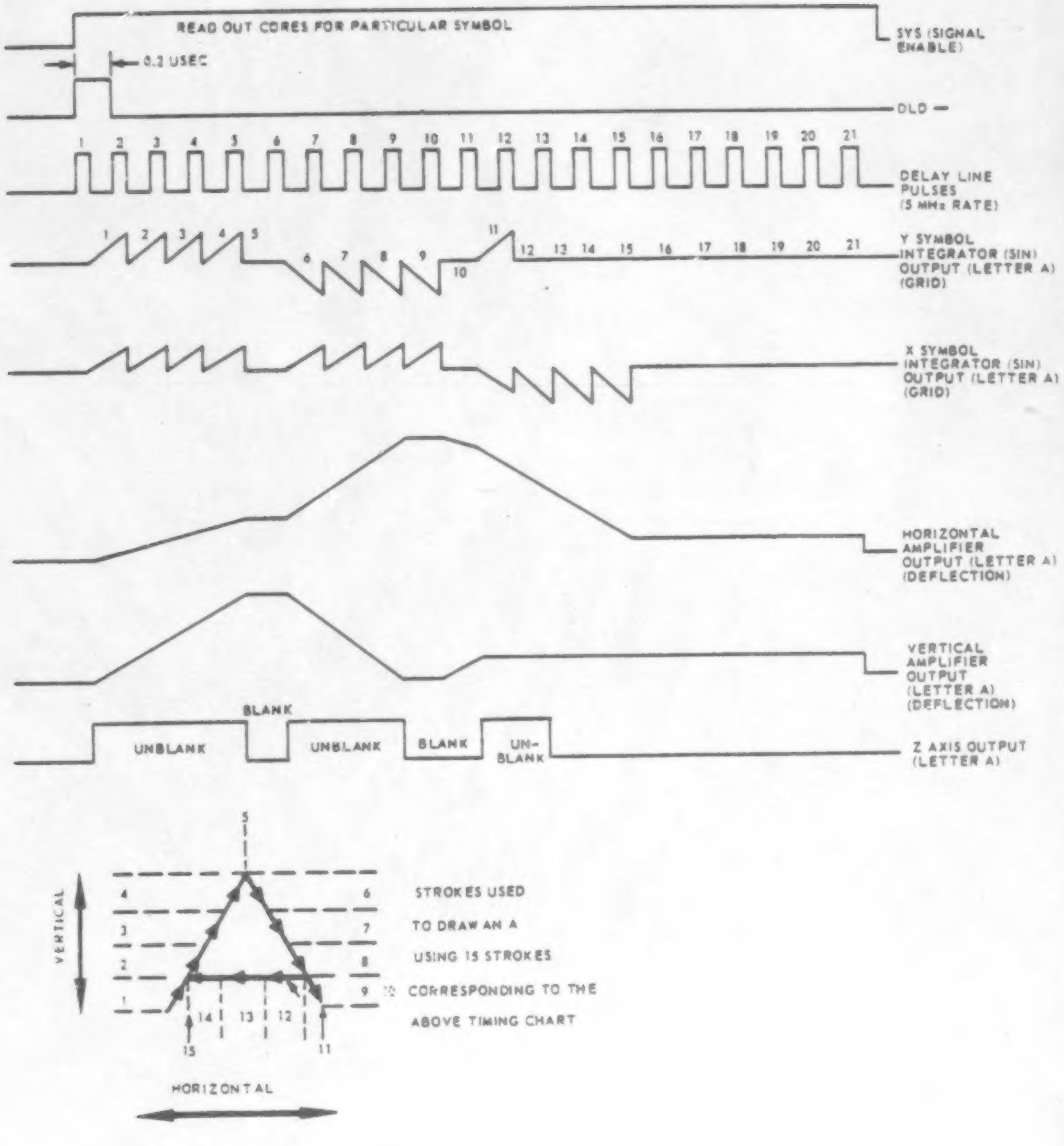

READ OUT CORES FOR PARTICULAR SYMBOL
SYS (SIGNAL ENABLE)
0.2 USEC
DLD —
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
DELAY LINE PULSES (5 MHz RATE)
Y SYMBOL INTEGRATOR (SIN) OUTPUT (LETTER A) (GRID)
X SYMBOL INTEGRATOR (SIN) OUTPUT (LETTER A) (GRID)
HORIZONTAL AMPLIFIER OUTPUT (LETTER A) (DEFLECTION)
VERTICAL AMPLIFIER OUTPUT (LETTER A) (DEFLECTION)
UNBLANK
BLANK
UNBLANK
BLANK
UN-BLANK
Z AXIS OUTPUT (LETTER A)
VERTICAL
HORIZONTAL
STROKES USED
TO DRAW AN A
USING 15 STROKES
CORRESPONDING TO THE
ABOVE TIMING CHART

Figure 71. Time sharing (unblanking).

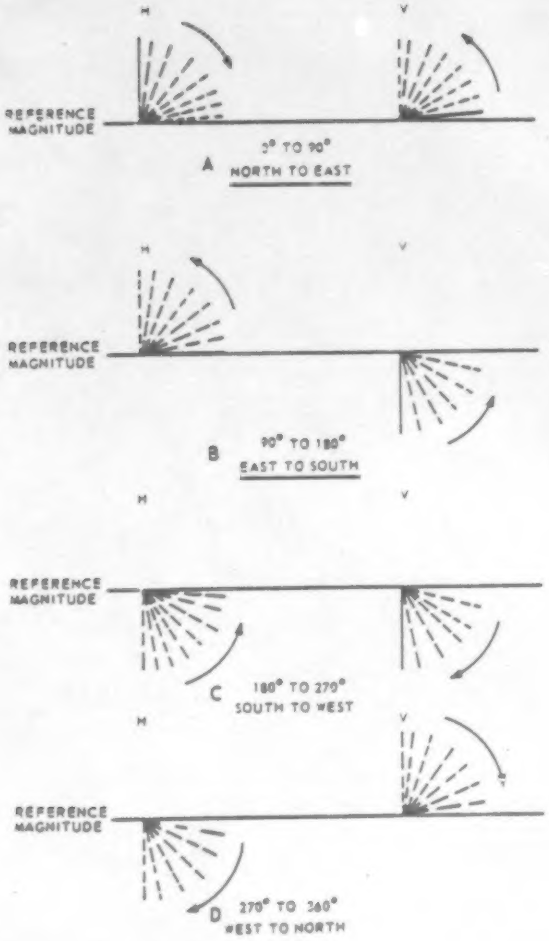
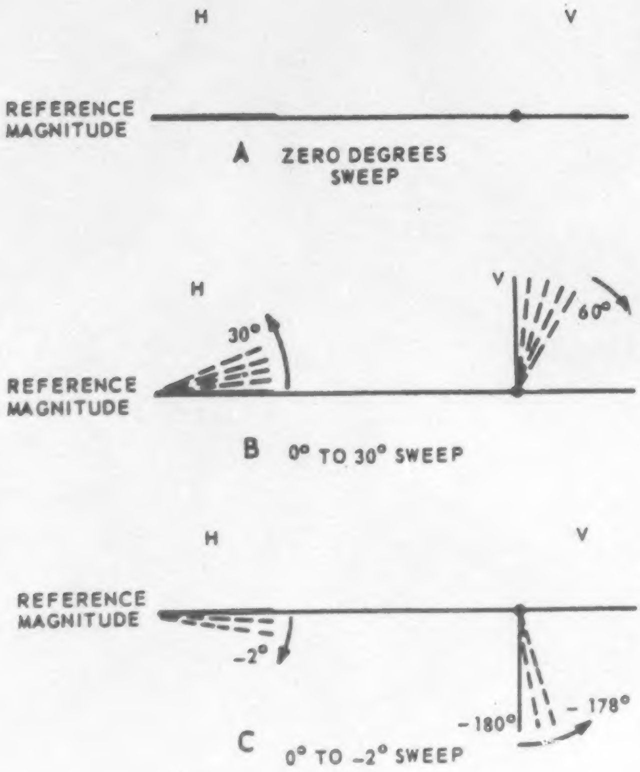

H
V
REFERENCE MAGNITUDE
0° TO 90°
A
NORTH TO EAST
H
V
REFERENCE MAGNITUDE
90° TO 180°
B
EAST TO SOUTH
H
V
REFERENCE MAGNITUDE
180° TO 270°
C
SOUTH TO WEST
H
V
REFERENCE MAGNITUDE
270° TO 360°
D
WEST TO NORTH

Figure 73. Sweep reference generator magnitudes (search).

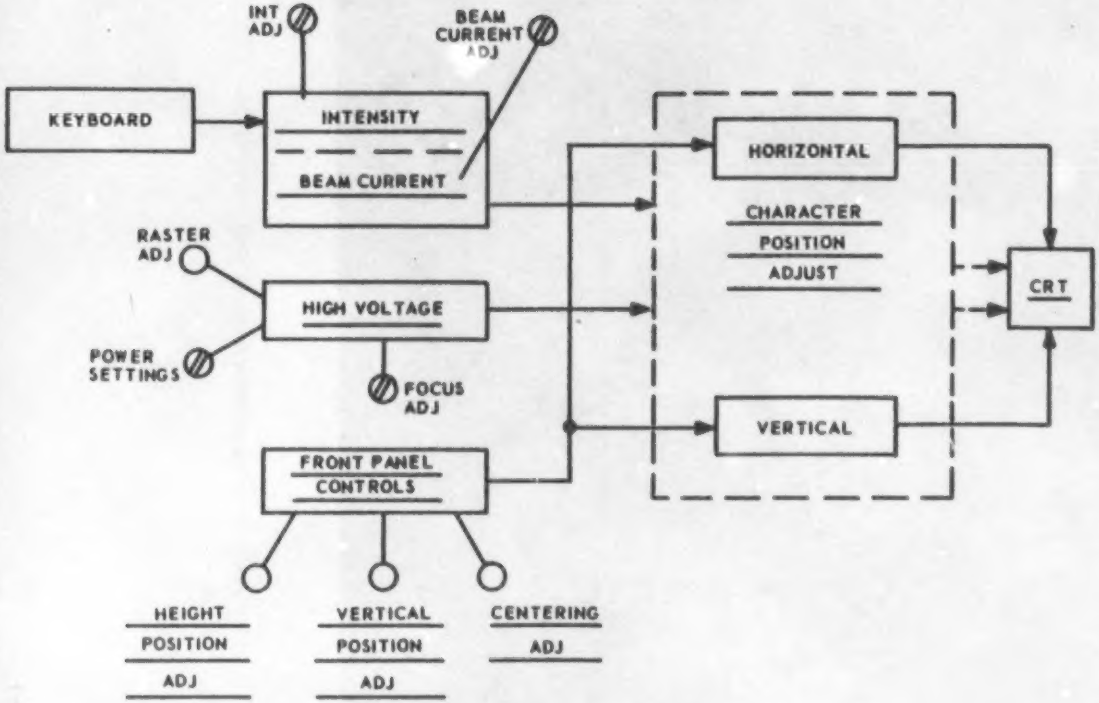

H
V
REFERENCE MAGNITUDE
H
V
30°
60°
REFERENCE MAGNITUDE
H
V
REFERENCE MAGNITUDE
-2°
-180°
-178°

A ZERO DEGREES SWEEP

B 0° TO 30° SWEEP

C 0° TO -2° SWEEP

Figure 74. Sweep reference generator magnitudes (height).



INT ADJ
BEAM CURRENT ADJ
KEYBOARD
INTENSITY
BEAM CURRENT
RASTER ADJ
HIGH VOLTAGE
POWER SETTINGS
FOCUS ADJ
FRONT PANEL CONTROLS
HORIZONTAL
CHARACTER POSITION ADJUST
VERTICAL
CRT
HEIGHT POSITION ADJ
VERTICAL POSITION ADJ
CENTERING ADJ

Figure 76. Interrelated units with controls.

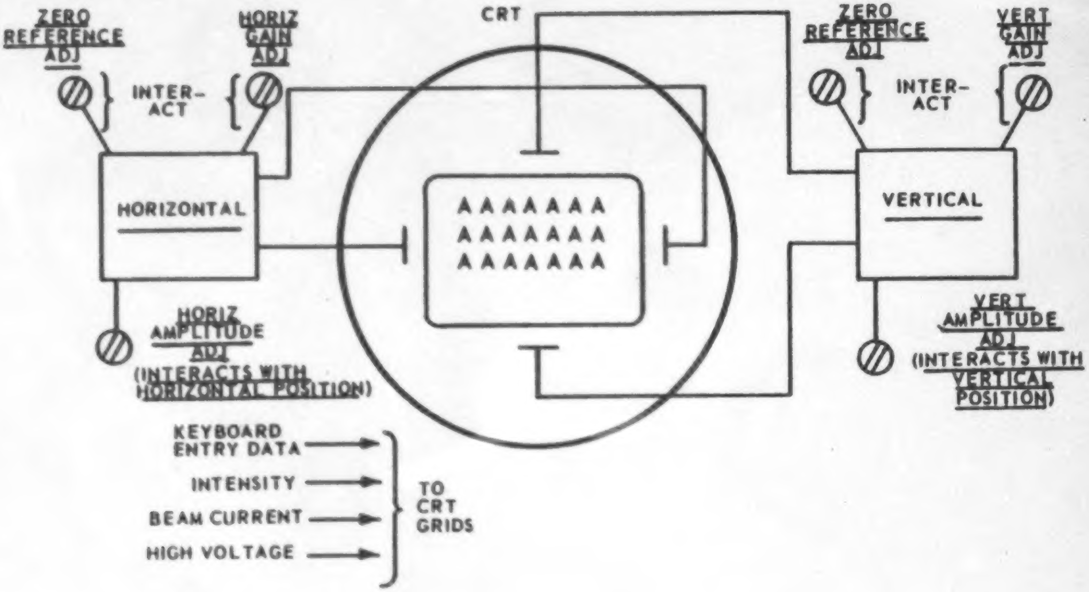

ZERO REFERENCE ADJ
HORIZ GAIN ADJ
INTER-ACT
CRT
ZERO REFERENCE ADJ
VERT GAIN ADJ
INTER-ACT
HORIZONTAL
AAAAAAA
AAAAAAA
AAAAAAA
VERTICAL
HORIZ AMPLITUDE ADJ (INTERACTS WITH HORIZONTAL POSITION)
VERT AMPLITUDE ADJ (INTERACTS WITH VERTICAL POSITION)
KEYBOARD ENTRY DATA
INTENSITY
BEAM CURRENT
HIGH VOLTAGE
TO CRT GRIDS

Figure 77. Deflection units with controls.

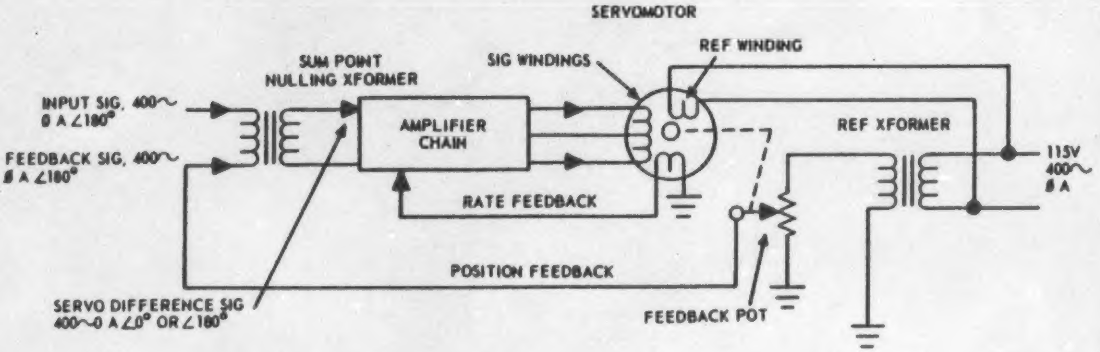

SERVOMOTOR
SIG WINDINGS
REF WINDING
SUM POINT
NULLING XFORMER
INPUT SIG, 400~
ø A ∠180°
FEEDBACK SIG, 400~
ø A ∠180°
AMPLIFIER
CHAIN
REF XFORMER
115V
400~
ø A
RATE FEEDBACK
POSITION FEEDBACK
SERVO DIFFERENCE SIG
400~ø A ∠0° OR ∠180°
FEEDBACK POT

Figure 78. Simplified servo block diagram.

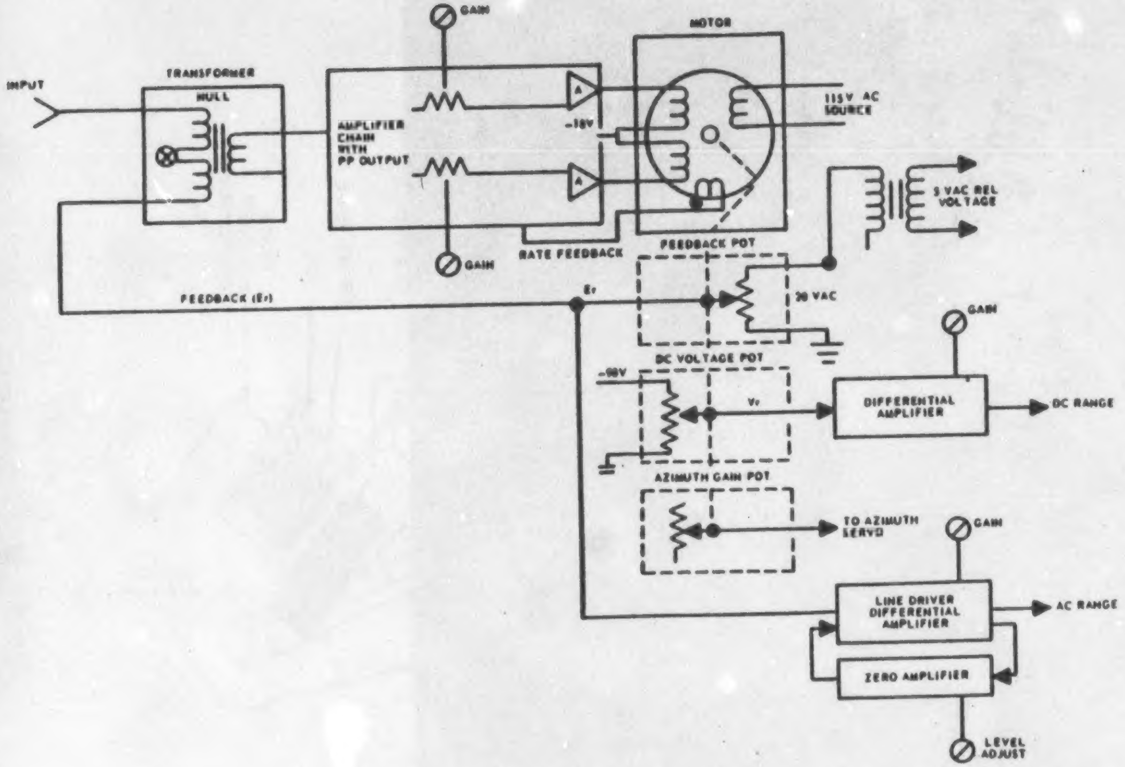

INPUT
TRANSFORMER
NULL
GAIN
AMPLIFIER CHAIN WITH PP OUTPUT
A
A
-18V
GAIN
MOTOR
115V AC SOURCE
5 VAC REF VOLTAGE
RATE FEEDBACK
FEEDBACK POT
FEEDBACK (Er)
Er
20 VAC
GAIN
DC VOLTAGE POT
-18V
Vr
DIFFERENTIAL AMPLIFIER
DC RANGE
AZIMUTH GAIN POT
TO AZIMUTH SERVO
GAIN
LINE DRIVER DIFFERENTIAL AMPLIFIER
AC RANGE
ZERO AMPLIFIER
LEVEL ADJUST

Figure 79. Servo subelements.

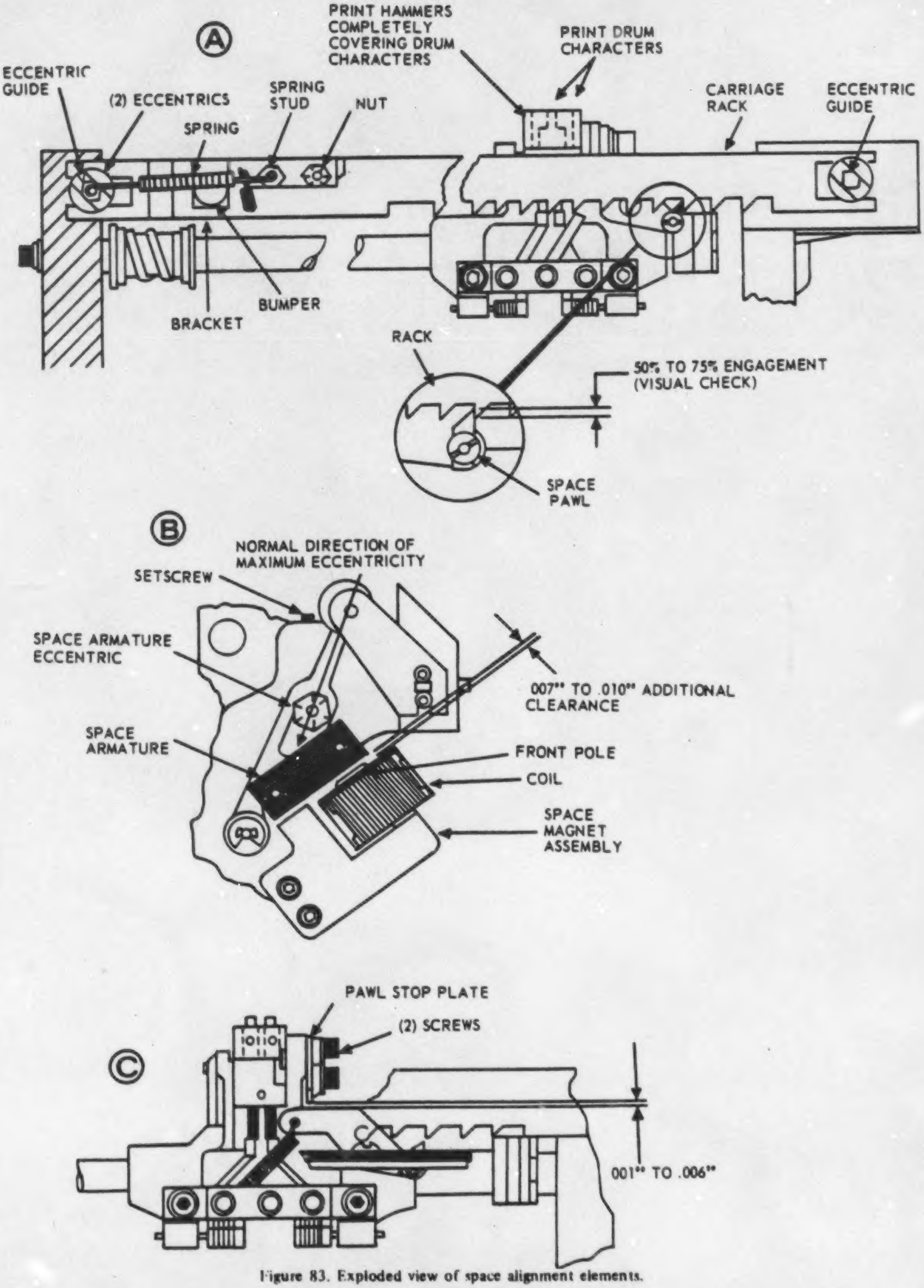

A
ECCENTRIC GUIDE
(2) ECCENTRICS
SPRING
SPRING STUD
NUT
PRINT HAMMERS COMPLETELY COVERING DRUM CHARACTERS
PRINT DRUM CHARACTERS
CARRIAGE RACK
ECCENTRIC GUIDE
BUMPER
BRACKET
RACK
50% TO 75% ENGAGEMENT (VISUAL CHECK)
SPACE PAWL
B
NORMAL DIRECTION OF MAXIMUM ECCENTRICITY
SETSCREW
SPACE ARMATURE ECCENTRIC
007" TO .010" ADDITIONAL CLEARANCE
SPACE ARMATURE
FRONT POLE
COIL
SPACE MAGNET ASSEMBLY
PAWL STOP PLATE
(2) SCREWS
C
001" TO .006"

Figure 83. Exploded view of space alignment elements.

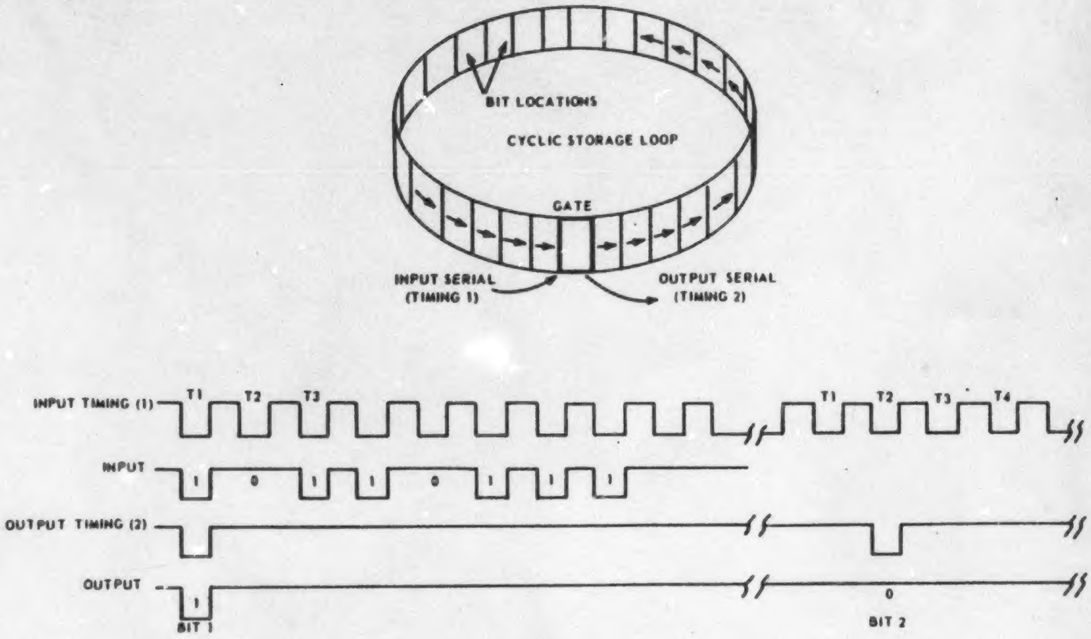

BIT LOCATIONS
CYCLIC STORAGE LOOP
GATE
INPUT SERIAL (TIMING 1)
OUTPUT SERIAL (TIMING 2)
INPUT TIMING (1)
T1
T2
T3
T1
T2
T3
T4
INPUT
1
0
1
1
0
1
1
1
OUTPUT TIMING (2)
OUTPUT
1
BIT 1
0
BIT 2

Figure 86. Cyclic storage.

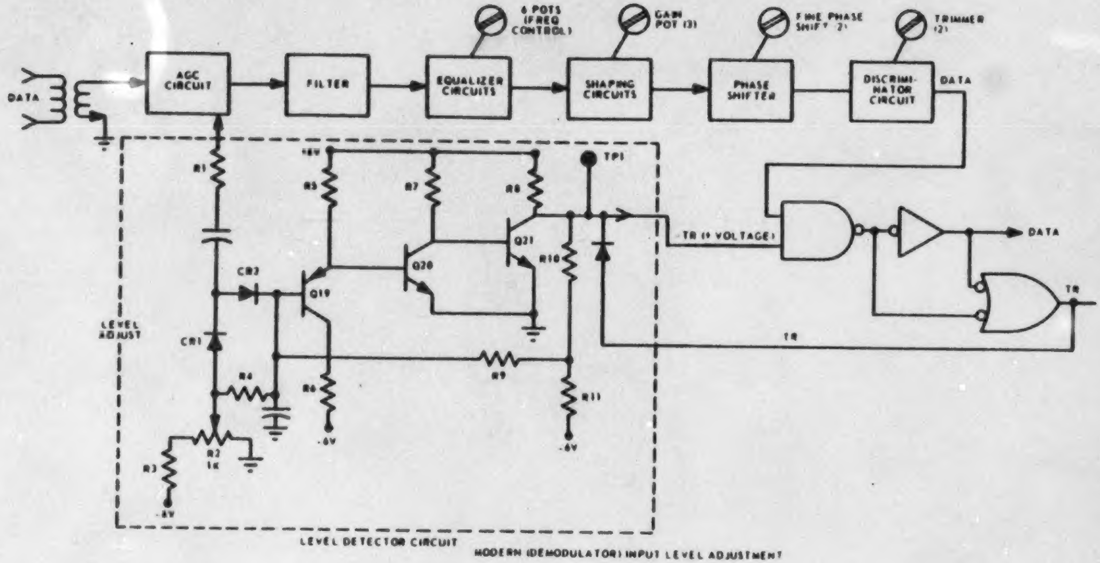

6 POTS (FREQ CONTROL)
GAIN POT (3)
FINE PHASE SHIFT (2)
TRIMMER (2)
DATA
AGC CIRCUIT
FILTER
EQUALIZER CIRCUITS
SHAPING CIRCUITS
PHASE SHIFTER
DISCRIMI-NATOR CIRCUIT
DATA
+8V
TP1
R1
R5
R7
R8
-TR (+ VOLTAGE)
DATA
Q21
R10
Q20
CR2
Q19
LEVEL ADJUST
CR1
TR
TR
R4
R9
R6
R11
-6V
-6V
R2
1K
R3
-6V
LEVEL DETECTOR CIRCUIT
MODERN (DEMODULATOR) INPUT LEVEL ADJUSTMENT

Figure 90. Data flow (modem).

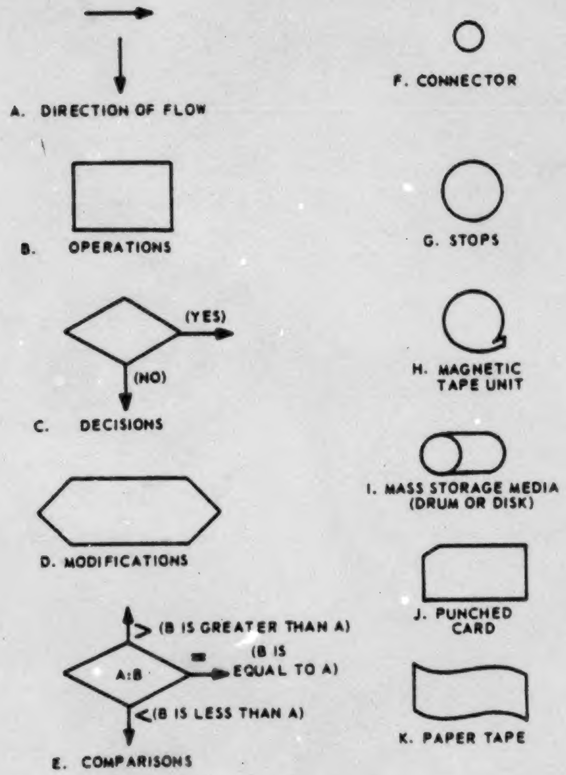

A. DIRECTION OF FLOW
F. CONNECTOR
B. OPERATIONS
G. STOPS
(YES)
(NO)
C. DECISIONS
H. MAGNETIC TAPE UNIT
I. MASS STORAGE MEDIA (DRUM OR DISK)
D. MODIFICATIONS
J. PUNCHED CARD
> (B IS GREATER THAN A)
= (B IS EQUAL TO A)
A:B
< (B IS LESS THAN A)
E. COMPARISONS
K. PAPER TAPE

Figure 91. Typical flow chart symbols.

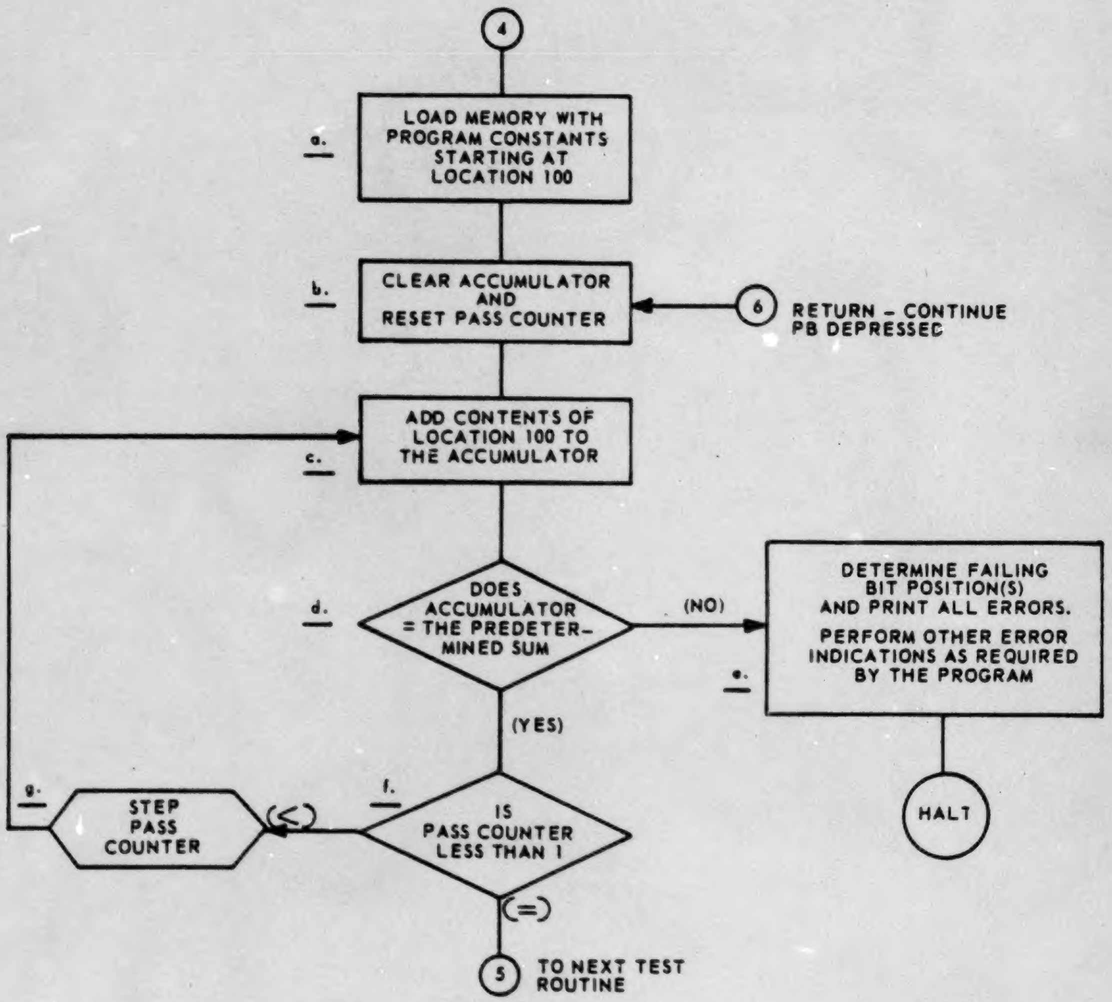

4
a.
LOAD MEMORY WITH PROGRAM CONSTANTS STARTING AT LOCATION 100
b.
CLEAR ACCUMULATOR AND RESET PASS COUNTER
6
RETURN - CONTINUE PB DEPRESSEC
c.
ADD CONTENTS OF LOCATION 100 TO THE ACCUMULATOR
d.
DOES ACCUMULATOR = THE PREDETERMINED SUM
(NO)
DETERMINE FAILING BIT POSITION(S) AND PRINT ALL ERRORS.
PERFORM OTHER ERROR INDICATIONS AS REQUIRED BY THE PROGRAM
e.
(YES)
HALT
g.
STEP PASS COUNTER
(<)
f.
IS PASS COUNTER LESS THAN 1
(=)
5
TO NEXT TEST ROUTINE

Figure 92. Flow chart for computer test program (add class instruction).

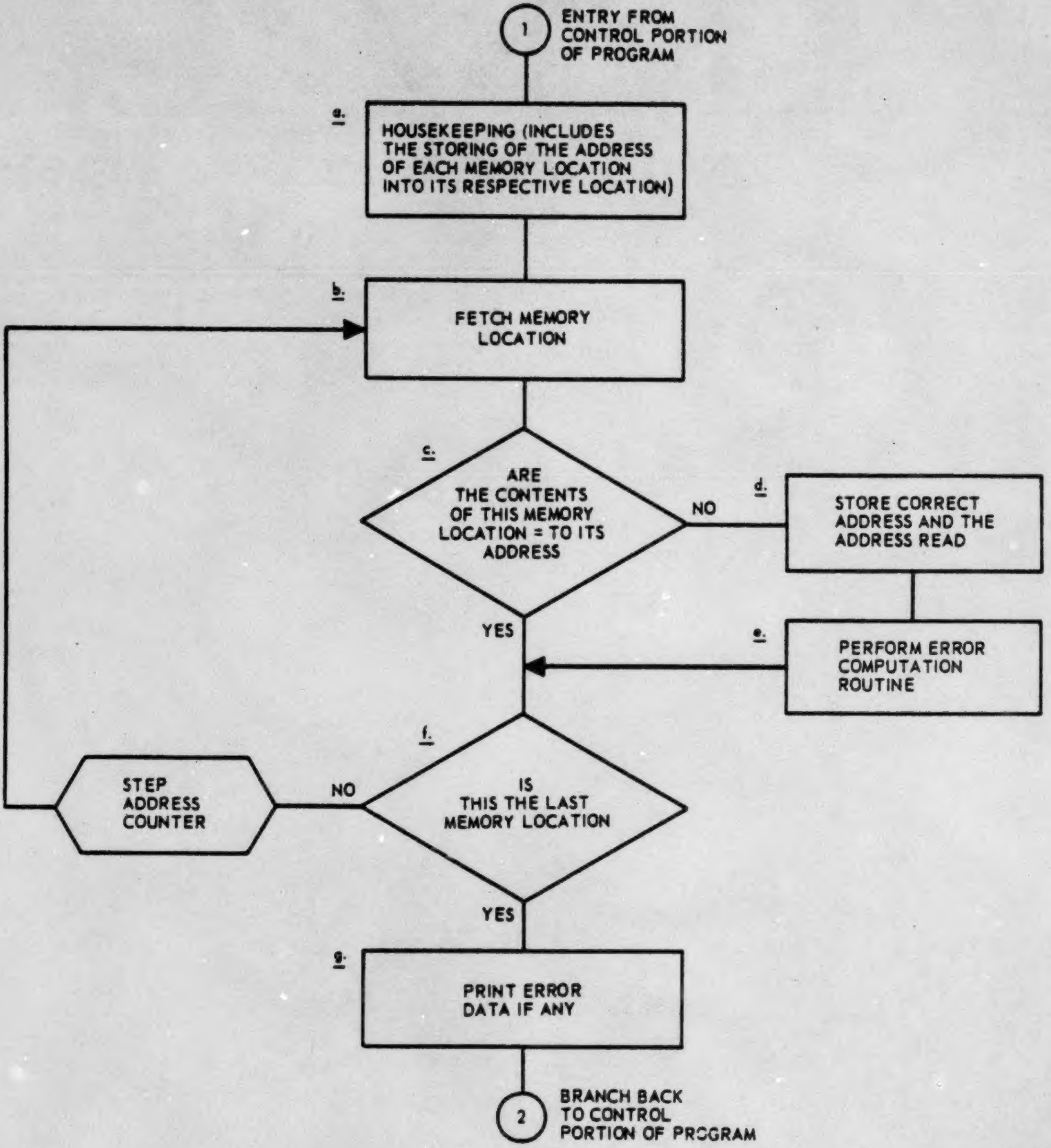

1
ENTRY FROM CONTROL PORTION OF PROGRAM
a.
HOUSEKEEPING (INCLUDES THE STORING OF THE ADDRESS OF EACH MEMORY LOCATION INTO ITS RESPECTIVE LOCATION)
b.
FETCH MEMORY LOCATION
c.
ARE THE CONTENTS OF THIS MEMORY LOCATION = TO ITS ADDRESS
NO
d.
STORE CORRECT ADDRESS AND THE ADDRESS READ
YES
e.
PERFORM ERROR COMPUTATION ROUTINE
f.
IS THIS THE LAST MEMORY LOCATION
NO
STEP ADDRESS COUNTER
YES
g.
PRINT ERROR DATA IF ANY
2
BRANCH BACK TO CONTROL PORTION OF PROGRAM

Figure 93. Flow chart for memory addressing test.

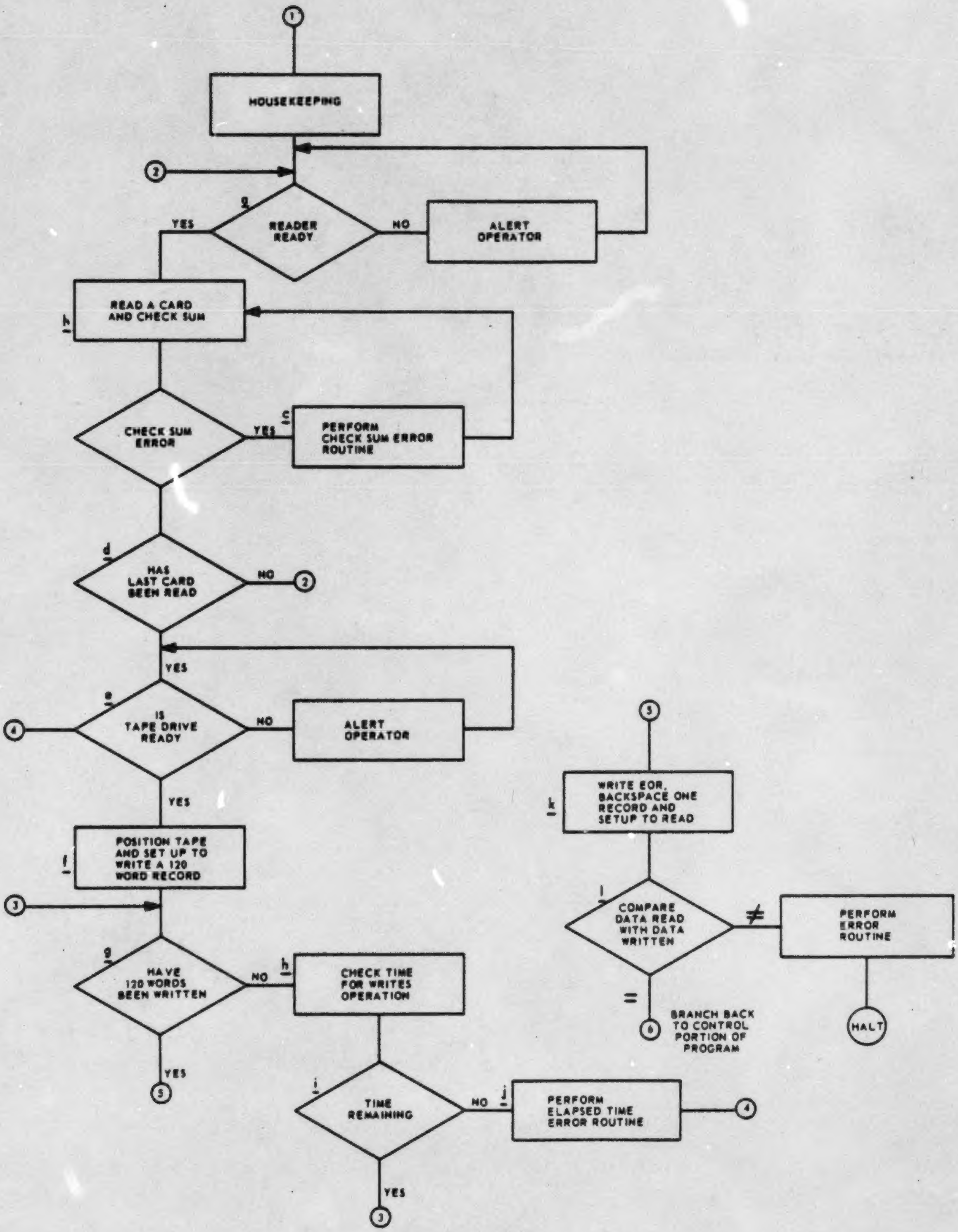

1
HOUSEKEEPING
2
a
READER READY
YES
NO
ALERT OPERATOR
b
READ A CARD AND CHECK SUM
CHECK SUM ERROR
YES
c
PERFORM CHECK SUM ERROR ROUTINE
d
HAS LAST CARD BEEN READ
NO
2
YES
e
IS TAPE DRIVE READY
4
NO
ALERT OPERATOR
YES
f
POSITION TAPE AND SET UP TO WRITE A 120 WORD RECORD
3
g
HAVE 120 WORDS BEEN WRITTEN
NO
h
CHECK TIME FOR WRITES OPERATION
YES
5
i
TIME REMAINING
NO
j
PERFORM ELAPSED TIME ERROR ROUTINE
4
YES
3
5
k
WRITE EOR, BACKSPACE ONE RECORD AND SETUP TO READ
l
COMPARE DATA READ WITH DATA WRITTEN
≠
PERFORM ERROR ROUTINE
HALT
=
6
BRANCH BACK TO CONTROL PORTION OF PROGRAM

Figure 94. Flow chart for card reader and tape drive test.

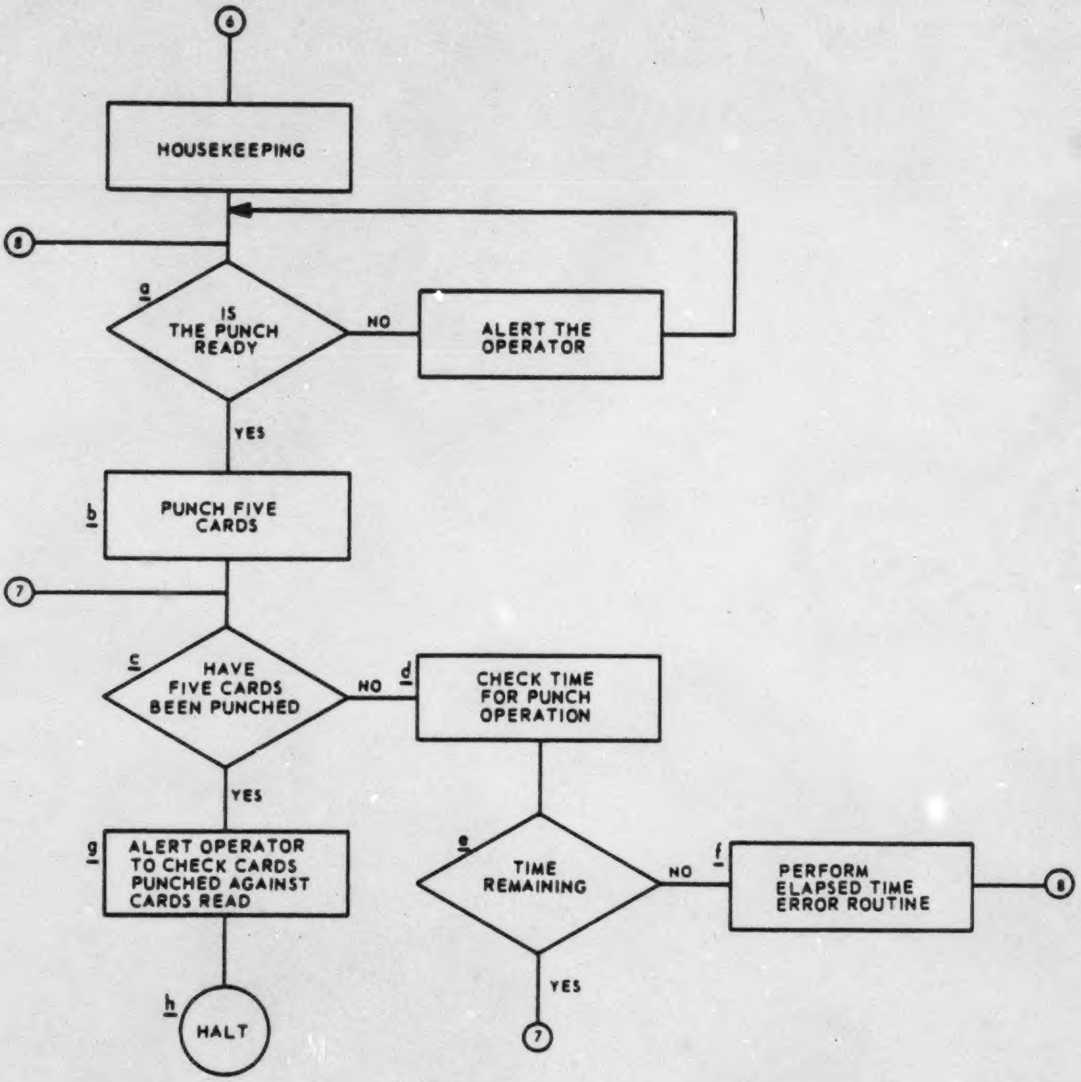

6
HOUSEKEEPING
8
a
IS THE PUNCH READY
NO
ALERT THE OPERATOR
YES
b
PUNCH FIVE CARDS
7
c
HAVE FIVE CARDS BEEN PUNCHED
NO
d
CHECK TIME FOR PUNCH OPERATION
YES
g
ALERT OPERATOR TO CHECK CARDS PUNCHED AGAINST CARDS READ
e
TIME REMAINING
NO
f
PERFORM ELAPSED TIME ERROR ROUTINE
8
h
HALT
YES
7

Figure 95. Flow chart for card punch test routine.

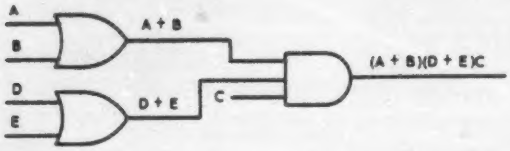

A
B
A + B
D
E
D + E
C
(A + B)(D + E)C

Figure 99. Logic AND function.

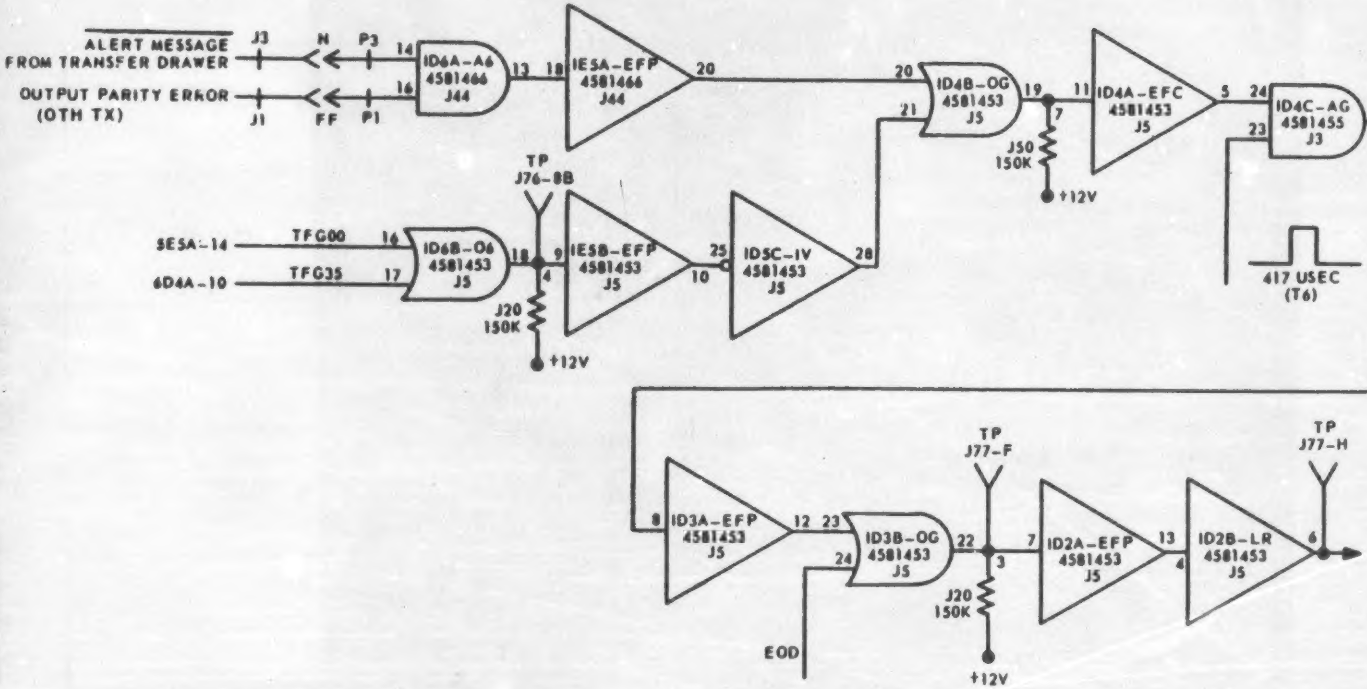
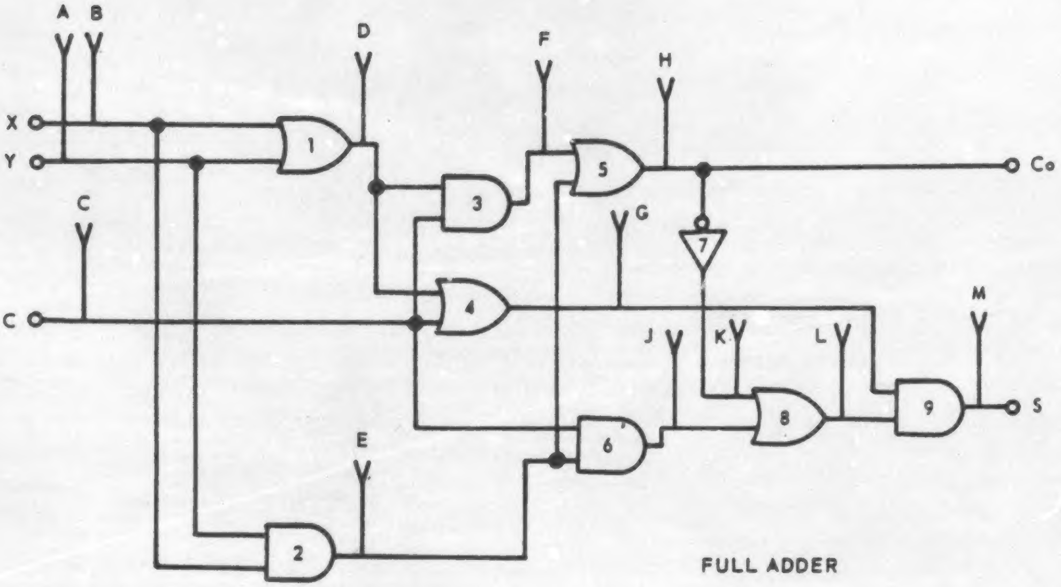

ALERT MESSAGE
FROM TRANSFER DRAWER
OUTPUT PARITY ERROR
(OTH TX)
J3
N
P3
J1
FF
P1
14
16
ID6A-A6
4581466
J44
13
18
IE5A-EFP
4581466
J44
20
20
21
ID4B-OG
4581453
J5
19
7
J50
150K
+12V
11
ID4A-EFC
4581453
J5
5
24
23
ID4C-AG
4581455
J3
22
417 USEC
(T6)
TP
J76-8B
5E5A-14
6D4A-10
TFG00
TFG35
16
17
ID6B-O6
4581453
J5
18
9
4
J20
150K
+12V
IE5B-EFP
4581453
J5
10
25
ID5C-IV
4581453
J5
28
8
ID3A-EFP
4581453
J5
12
23
24
ID3B-OG
4581453
J5
EOD
22
TP
J77-F
3
J20
150K
+12V
7
ID2A-EFP
4581453
J5
13
4
ID2B-LR
4581453
J5
6
TP
J77-H

Figure 100. Stepping circuit.

579


A
B
D
F
H
X
Y
C
C
1
3
5
Co
G
7
4
J
K
L
M
9
S
8
6
E
2
FULL ADDER

	INPUT			OUTPUT	
	X	Y	C	S	Co
1	0	0	0	0	0
2	0	0	1	1	0
3	0	1	0	1	0
4	0	1	1	0	1
5	1	0	0	1	0
6	1	0	1	0	1
7	1	1	0	0	1
8	1	1	1	1	1

TRUTH TABLE

Figure 101. Full adder circuit and truth table.

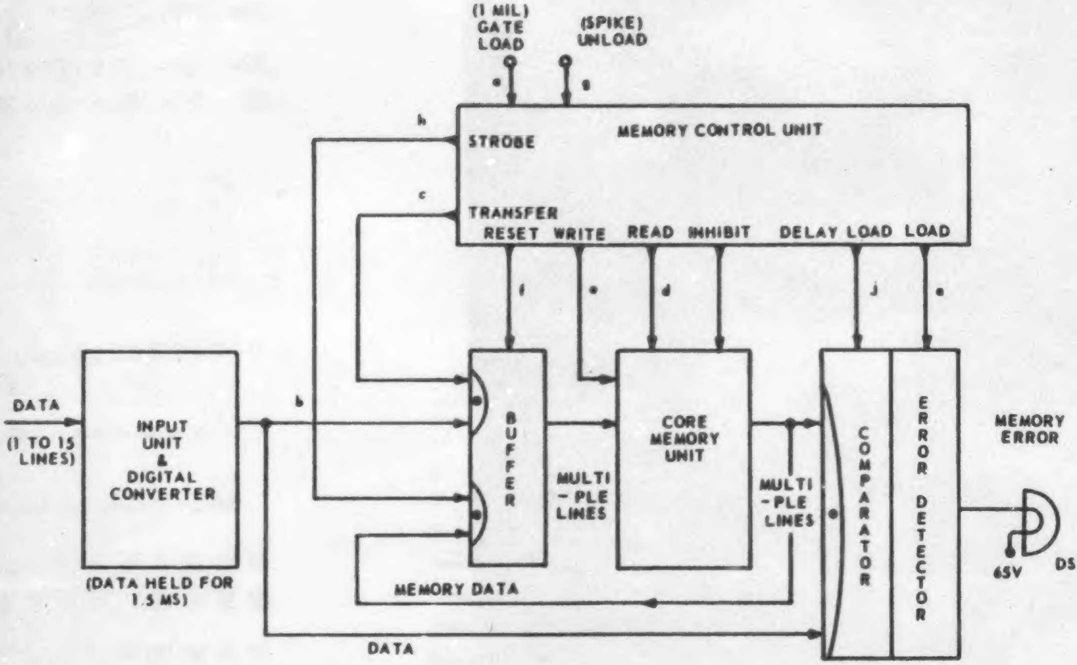

(1 MIL) GATE LOAD
(SPIKE) UNLOAD
a
g
h
STROBE
MEMORY CONTROL UNIT
c
TRANSFER
RESET
WRITE
READ
INHIBIT
DELAY LOAD
LOAD
f
e
d
j
e
DATA
(1 TO 15 LINES)
INPUT UNIT & DIGITAL CONVERTER
(DATA HELD FOR 1.5 MS)
b
BUFFER
MULTI - PLE LINES
CORE MEMORY UNIT
MULTI - PLE LINES
COMPARATOR
ERROR DETECTOR
MEMORY ERROR
6SV
DS1
MEMORY DATA
DATA

Figure 113. Memory unit block diagram.

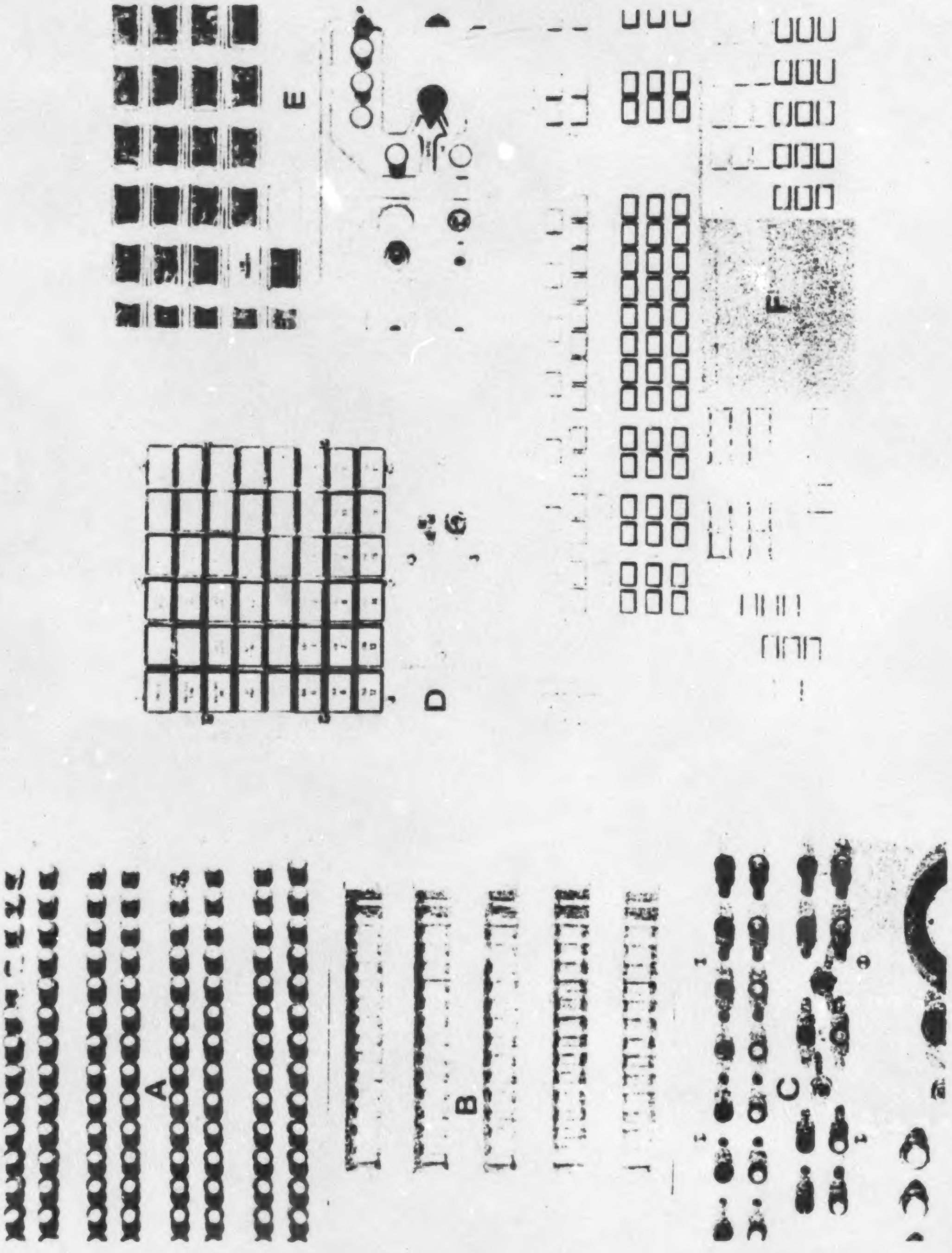


Figure 118. Types of indicator panels.

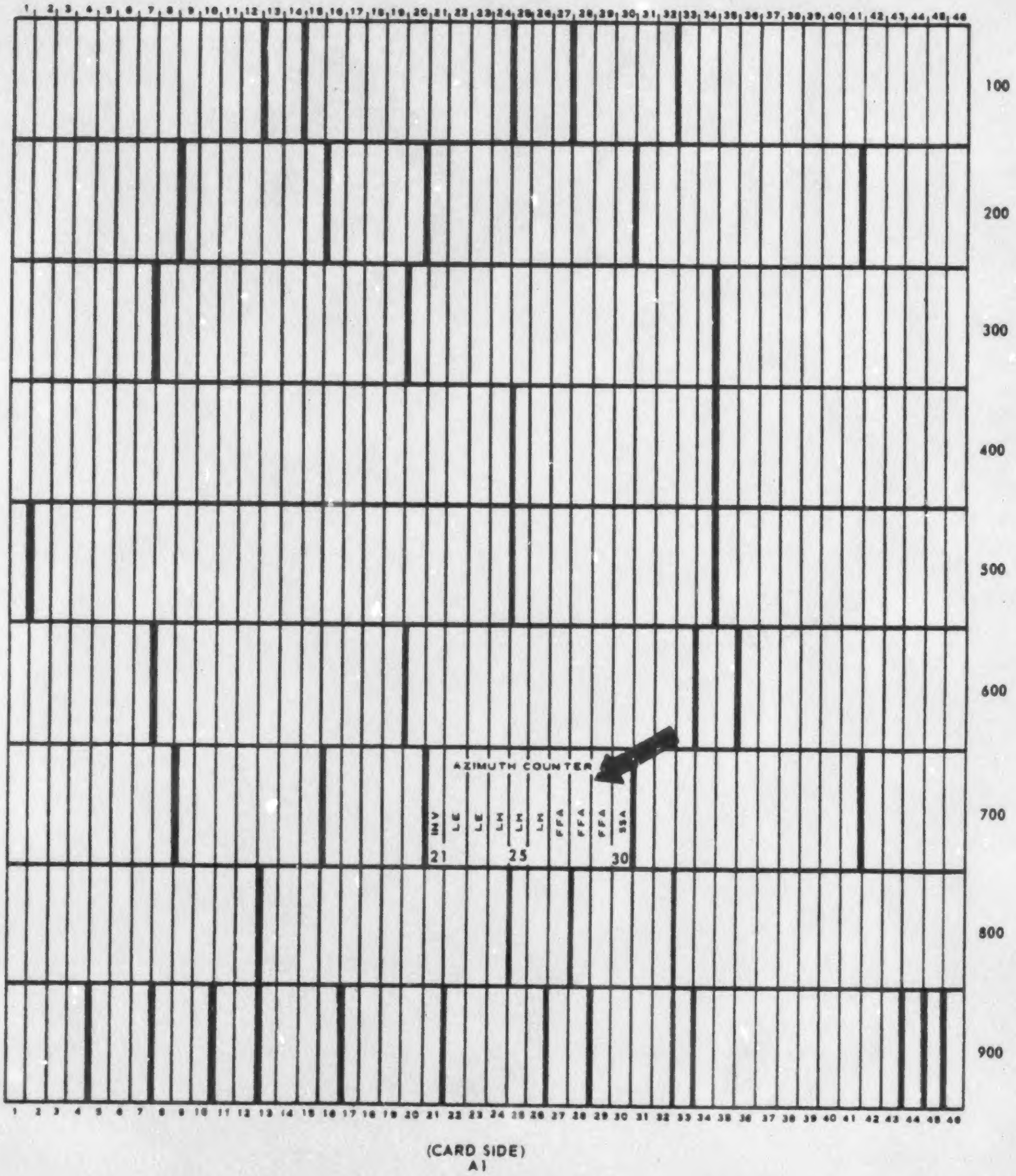

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46
100
200
300
400
500
600
700
800
900
AZIMUTH COUNTER
INV
LE
LE
LH
LH
LH
FFA
FFA
FFA
SSA
21
25
30
(CARD SIDE)
A1

Figure 120. Card location chart.

Card Group	Rack	Row	Slot	Part Number
B405	DBSG	10	32	1570471
		10	33	1570471
		10	34	1570471
		10	35	1570471
		10	36	1570471
B406	DBSG	10	33	1570471
		10	36	1570471
B502	DBSG	10	26	1570468
		10	35	1570471
		10	36	1570471
		10	38	1570470
		10	45	1570480
B503	DBSG	10	38	1570470
B504	DBSG	10	38	1570470
B505	DBSG	10	34	1570471
		10	38	1570470
B506	DBSG	10	34	1570471
B507	DBSG	10	33	1570471
B508	DBSG	10	33	1570471
B509	DBSG	10	32	1570471
B510	DBSG	10	32	1570471

Card Group	Rack	Row	Slot	Part Number
B601*	DBSG	10	39	1570472
		10	40	1570473
		10	41	1570477
		10	45	1570480
		10	46	1570475
B701*	DBSG	10	33	1570471
see	AROSG	9	43	1570380
NOTE A				
B801	DBSG	10	14	1571163
see		10	26	1570468
NOTE A		10	29	1570169
		10	33	1570471
		10	35	1570471
		10	39	1570472
		10	40	1570473
		10	42	1570479
		10	43	1570474
		10	47	1570476
	PPISG	8	40	1570386
B802	DBSG	10	36	1570471
		10	40	1570473
		10	41	1570477
B803	DBSG	10	15	1570469
see		10	42	1570479
NOTE A		10	44	1570478
	AROSG	9	24	1570376
		9	25	1570376
		9	26	1570378
		9	27	1570378
		9	39	1570378

Figure 121. Self-test table displays.

UNITS DEVICES	LINE DATA	POWER SUPPLIES	CRT DISPLAYS	SERVO UNITS	RADAR DATA	CENTRAL PROCESSORS DATA	DIGITAL DATA DISPLAYS	ELECTROGRAPHIC PRINTERS	IMPACT PRINTERS	RADAR ANTENNA ORIENTATION	PARITY CIRCUITS	TAPE TRANSPORT UNITS	REFERENCE VOLTAGES
METERS													
1. AC VOLT													
2. DC VOLT													
3. DIFFERENTIAL													
4. CURRENT													
OSCILLOSCOPES DISPLAYS													
CRT DISPLAYS													
PRINTOUTS													
LAMPS AND AUDIO ALARMS													
VISUAL EXAM OF MECHANICAL ASSEMBLIES													

Chart 1. Performance checking devices and units.

HORIZONTAL CHARACTER AND DEFLECTION CIRCUITRY

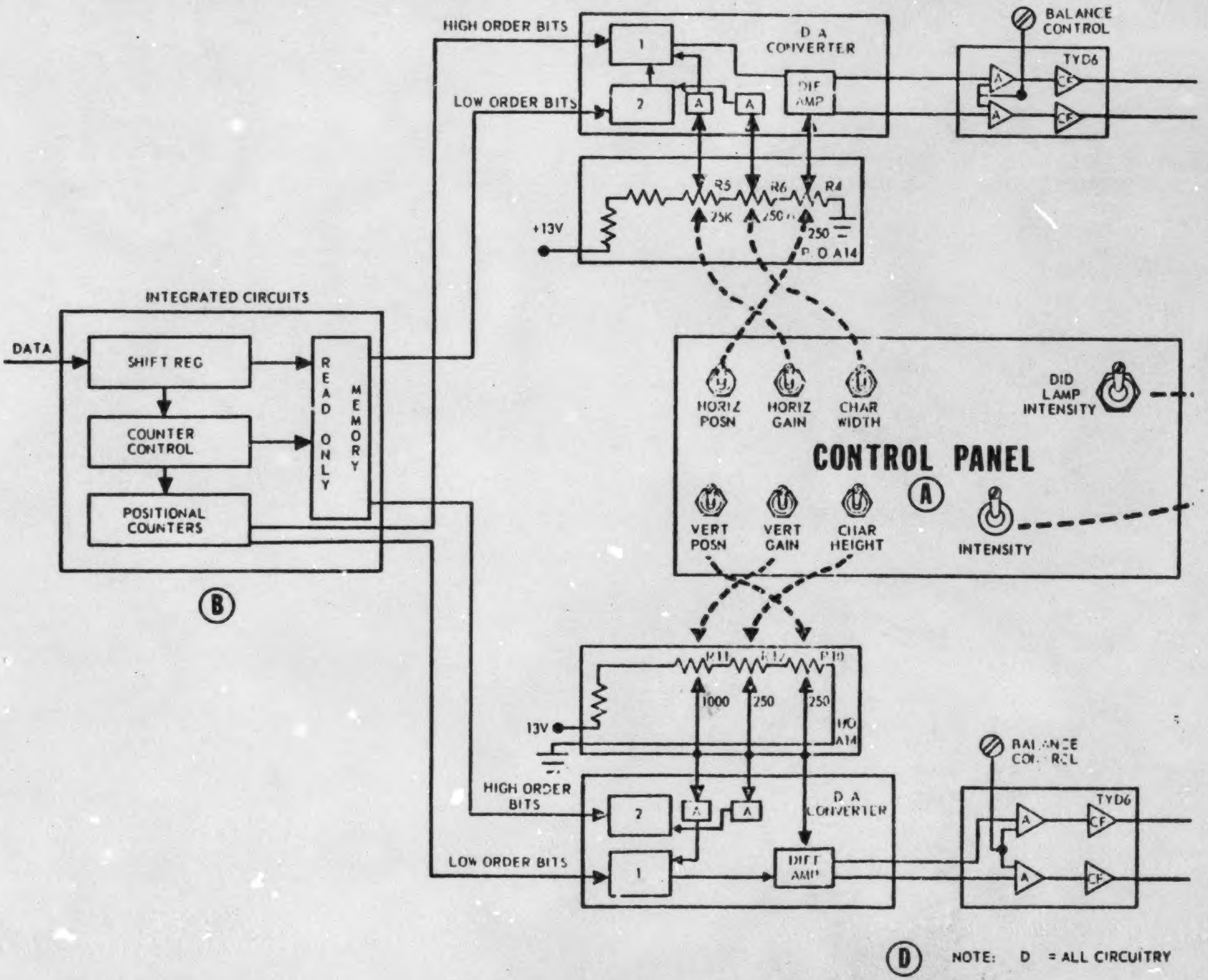

HIGH ORDER BITS
LOW ORDER BITS
1
2
A
A
D A CONVERTER
DIF AMP
BALANCE CONTROL
TYD6
A
A
CF
CF
R5
R6
R4
+13V
25K
250
250
P. O A14
INTEGRATED CIRCUITS
DATA
SHIFT REG
COUNTER CONTROL
POSITIONAL COUNTERS
READ ONLY
MEMORY
B
HORIZ POSN
HORIZ GAIN
CHAR WIDTH
DID LAMP INTENSITY
CONTROL PANEL
A
VERT POSN
VERT GAIN
CHAR HEIGHT
INTENSITY
R11
R12
R10
1000
250
250
13V
P/O A14
HIGH ORDER BITS
LOW ORDER BITS
2
1
A
A
D A CONVERTER
DIFF AMP
BALANCE CONTROL
TYD6
A
A
CF
CF
D
NOTE: D = ALL CIRCUITRY

Figure 55 (cut apart)

VERTICAL CHARACTER AND DEFLECTION CIRCUITRY

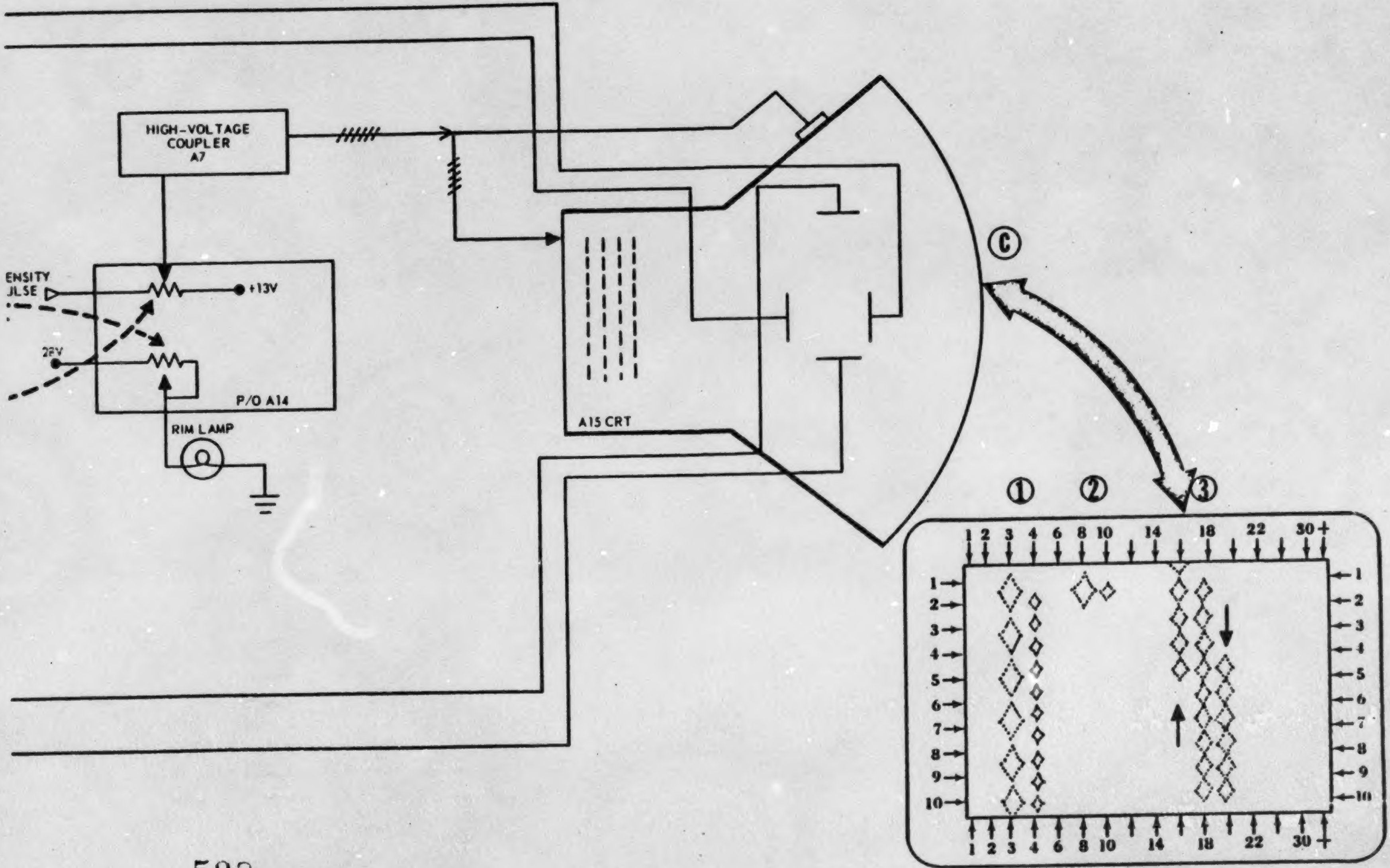
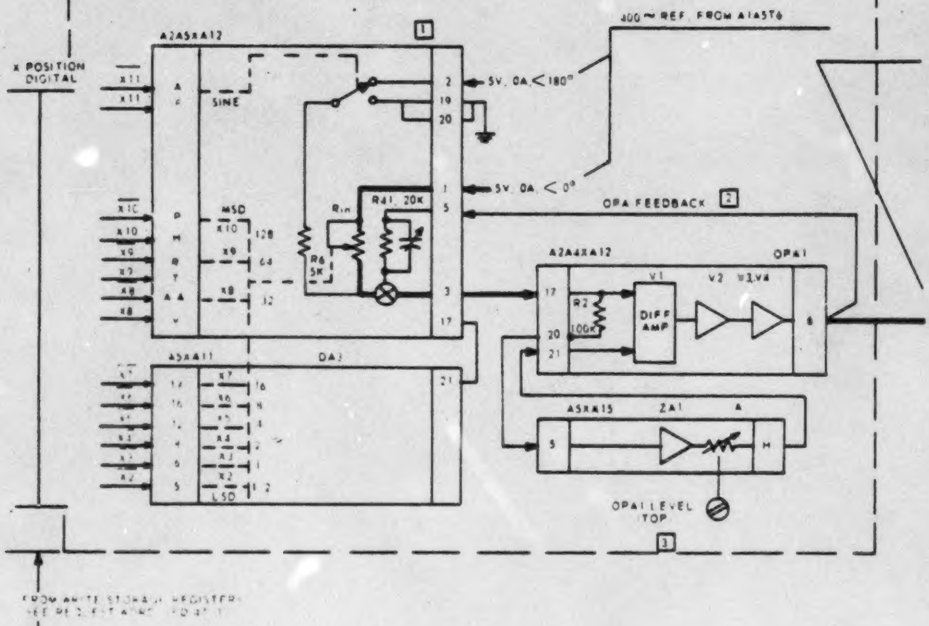

HIGH-VOLTAGE
COUPLER
A7
ENSITY
JLSE
+13V
28V
P/O A14
RIM LAMP
A15 CRT
Ⓒ
①
②
③
1 2 3 4 6 8 10 14 18 22 30 +
1 2 3 4 5 6 7 8 9 10

Figure 55. D [illegible] unit.

587

DIGITAL TO ANALOG CONVERTER "X"


X POSITION DIGITAL
A2A5XA12
400 ~ REF. FROM A1A5T6
SINE
5V, 0A, < 180°
5V, 0A, < 0°
OPA FEEDBACK
MSD
R41, 20K
Rin
R6 5K
128
64
32
A2A4XA12
OPA1
V1
V2
V3,V4
R2 100K
DIFF AMP
A5XA11
DA3
LSD
A5XA15
ZA1
OPA1 LEVEL (TOP)
FROM WRITE STORAGE REGISTERS

DIGITAL TO ANALOG CONVERTER "Y"

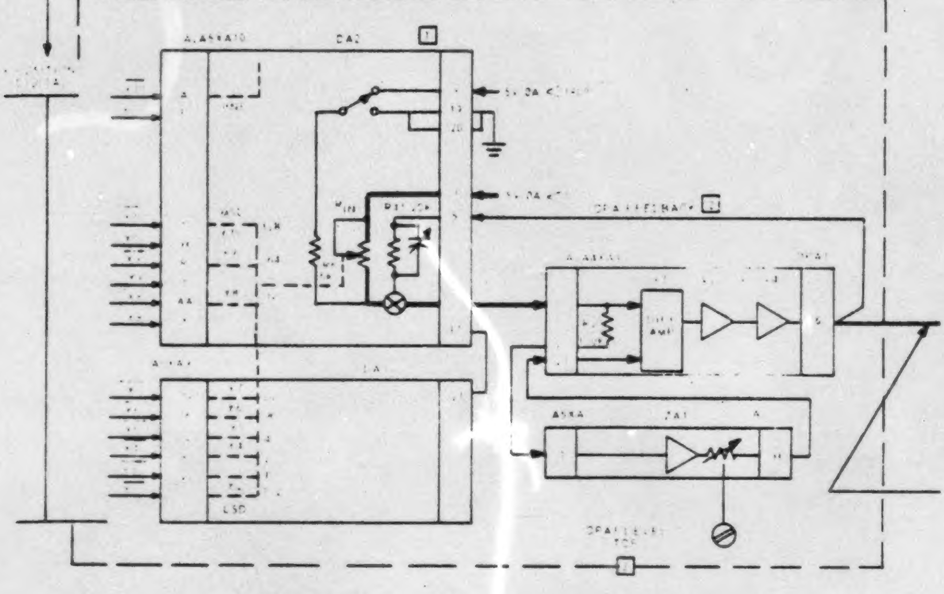
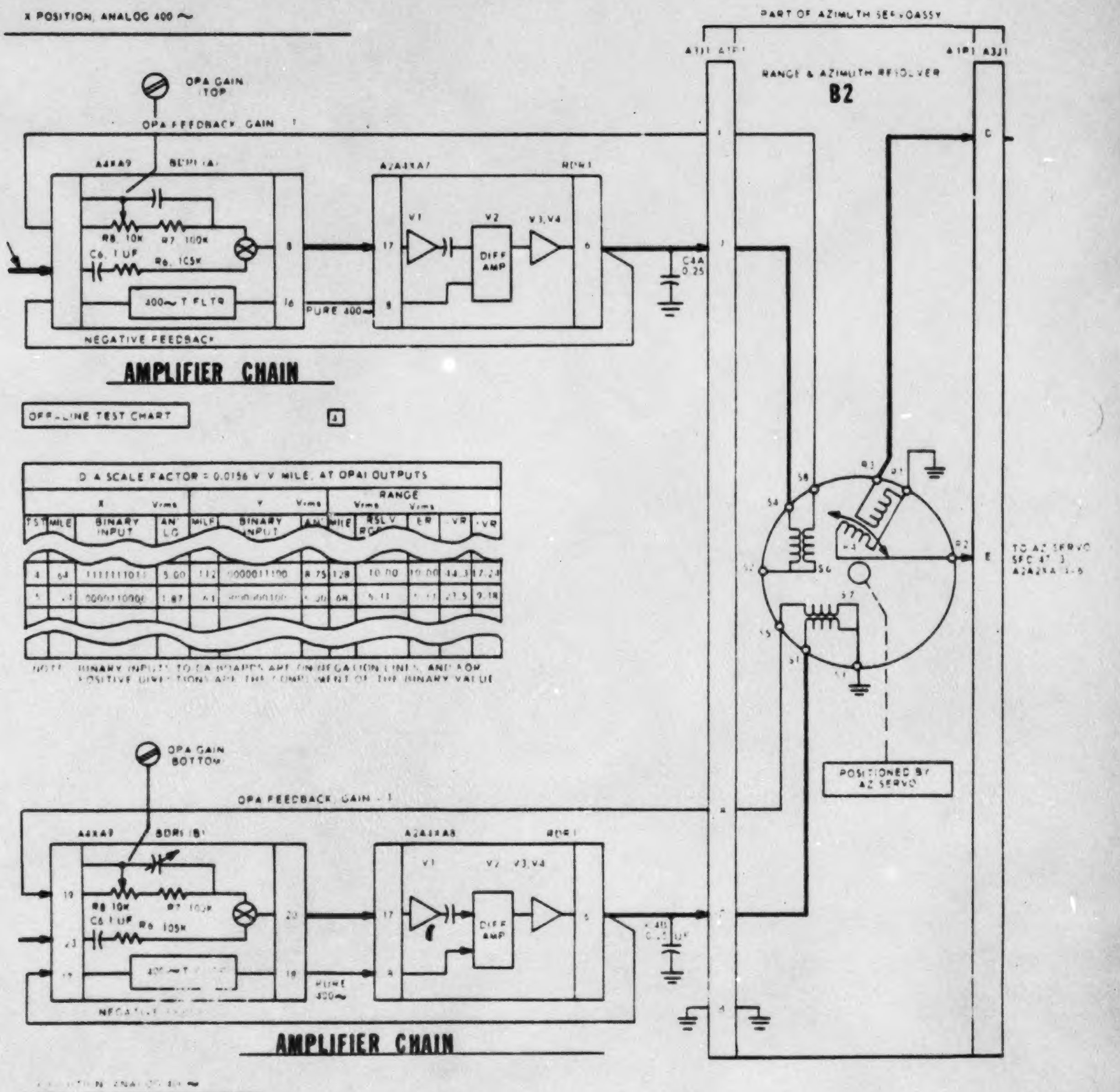

DA2
OPA FEEDBACK
DIFF AMP
OPA1
ZA1
LSD
OPA1 LEVEL (TOP)

Figure 81 (cut apart)

588


X POSITION, ANALOG 400 ~
OPA GAIN (TOP)
OPA FEEDBACK, GAIN 1
A4XA9
BDR1 (A)
R8, 10K
R7, 100K
C6, 1 UF
R6, 105K
400~ T FLTR
NEGATIVE FEEDBACK
A2A4XA7
RDR1
V1
V2
V3, V4
DIFF AMP
PURE 400~
C4A 0.25
AMPLIFIER CHAIN
OFF-LINE TEST CHART
PART OF AZIMUTH SERVOASSY
RANGE & AZIMUTH RESOLVER
B2
S4
S8
R3
R1
R2
S6
S2
S7
S5
S1
S3
TO AZ SERVO
POSITIONED BY AZ SERVO
OPA GAIN BOTTOM
OPA FEEDBACK, GAIN - 1
BDR1 (B)
A2A4XA8
AMPLIFIER CHAIN

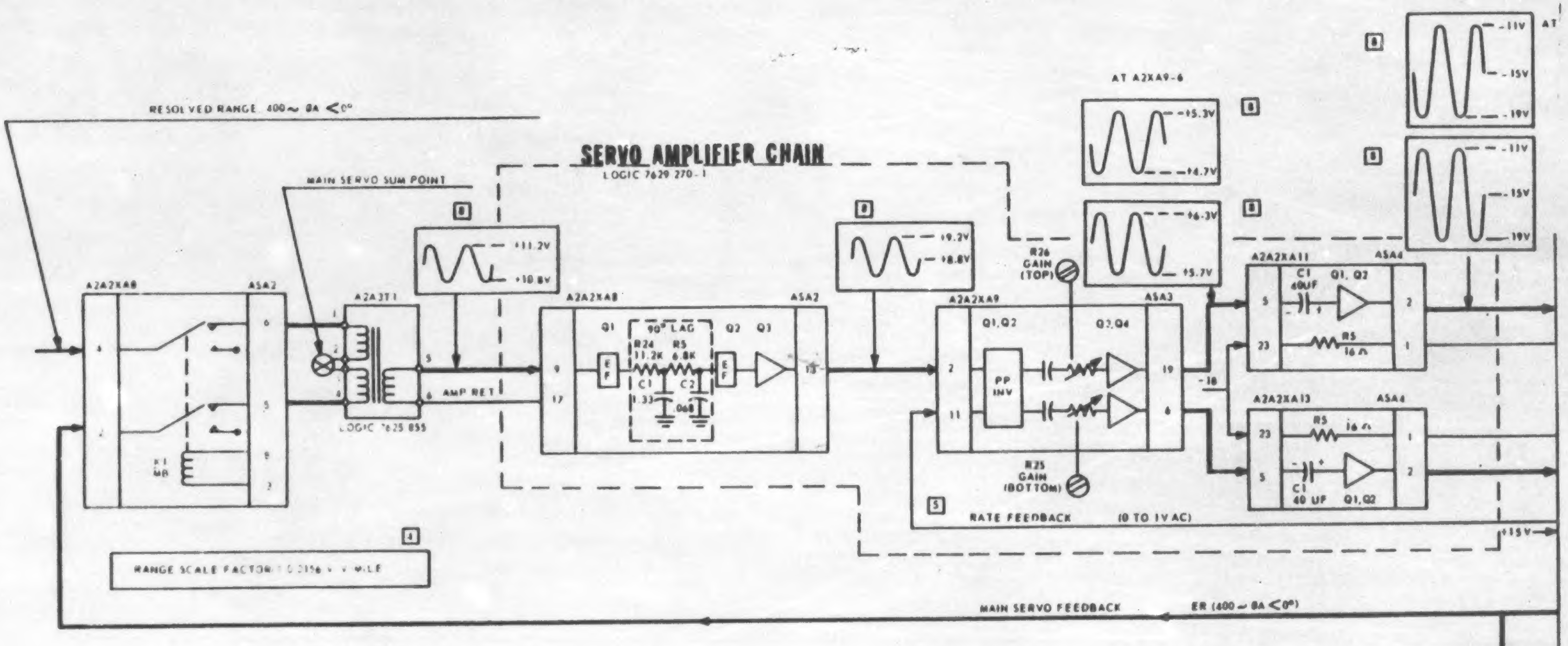
D A SCALE FACTOR = 0.0156 V V MILE, AT OPA1 OUTPUTS

	X		Vrms	Y		Vrms	RANGE Vrms		Vrms		
TST	MILE	BINARY INPUT	ANLG	MILE	BINARY INPUT	AN	MILE	RSLV RCR	ER	-VR	+VR
4	64	1111111011	5.00	112	0000011100	8.75	128	10.00	10.00	44.3	17.24
5	[illegible]	0000110000	1.87	61	[illegible]	[illegible]	68	5.11	[illegible]	27.5	9.18

NOTE: BINARY INPUTS TO D A BOARDS ARE ON NEGATION LINES, AND FOR POSITIVE DIRECTIONS ARE THE COMPLEMENT OF THE BINARY VALUE

Figure 81 (cut apart)

601


SERVO AMPLIFIER CHAIN
LOGIC 7629 270-1
RESOLVED RANGE 400~ 8A <0°
MAIN SERVO SUM POINT
A2A2XA8
ASA2
K1
MB
A2A3T1
LOGIC 7625 855
AMP RET
8
+11.2V
+10.8V
A2A2XA8
ASA2
Q1
90° LAG
R24
11.2K
R5
6.8K
C1
1.33
C2
.068
Q2
Q3
E
F
8
+9.2V
+8.8V
A2A2XA9
ASA3
Q1,Q2
PP
INV
Q3,Q4
R26
GAIN
(TOP)
R25
GAIN
(BOTTOM)
AT A2XA9-6
8
+5.3V
+4.7V
8
+6.3V
+5.7V
-18
A2A2XA11
ASA4
C1
40UF
Q1, Q2
R5
16 Ω
A2A2XA13
ASA4
R5
16 Ω
C1
40 UF
Q1,Q2
8
-11V
-15V
-19V
8
-11V
-15V
-19V
AT
5
RATE FEEDBACK
(0 TO 1V AC)
+15V
4
RANGE SCALE FACTOR: 0.2156 V/V MILE
MAIN SERVO FEEDBACK
ER (400 ~ 8A <0°)

NOTES

[1] DA2 AND DA3 BOARDS ARE SHOWN FUNCTIONALLY. TRANSISTOR SWITCHING CIRCUITRY INSERTS DIFFERENT VALUES OF OPA INPUT RESISTANCE BETWEEN PINS 1 AND 3, AS R_{in}. (SEE DA2s AT LEFT OF PAGE.)

[2] GAIN OF OPERATIONAL AMPLIFIERS IS THE RATIO OF FEEDBACK RESISTANCE (DA2-R41) TO INPUT RESISTANCE (DA2-R_{in}).

[3] ZA1 BOARDS ARE ADJUSTABLE GAIN, DC, TRANSISTOR, INVERTING AMPLIFIERS USED TO COMPENSATE FOR DC DRIFT OF OPA, GAM, AND LDR BOARDS. ADJ FOR 0 VDC (NO INPUT) AT CONTROLLED BOARDS' OUTPUTS.

[4] SCALE FACTORS ARE VOLTS PER MILE FOR EACH VOLT (ACTUAL) OF REF AT A1A5T6, PIN 14 OR LL. IF REF VOLTAGE IS EXACTLY 5000 RMS, MULTIPLY BY 5000, ETC. E_r AND ANALOG VOLTAGES ARE RMS, FOR 5000 REF, RMS.

[5] RATE FEEDBACK IS ZERO WHEN SERVO IS STATIONARY, APPROX 1V RMS AT MAX VELOCITY.

[7] SAME AS [3]

[8] AMPLITUDES AND LEVELS OF NULL VOLTAGES ARE TYPICAL ONLY. AMPLITUDES WILL VARY APPROX 50% WITH RANGE.

Figure 81 (cut apart)

A2XA13-2

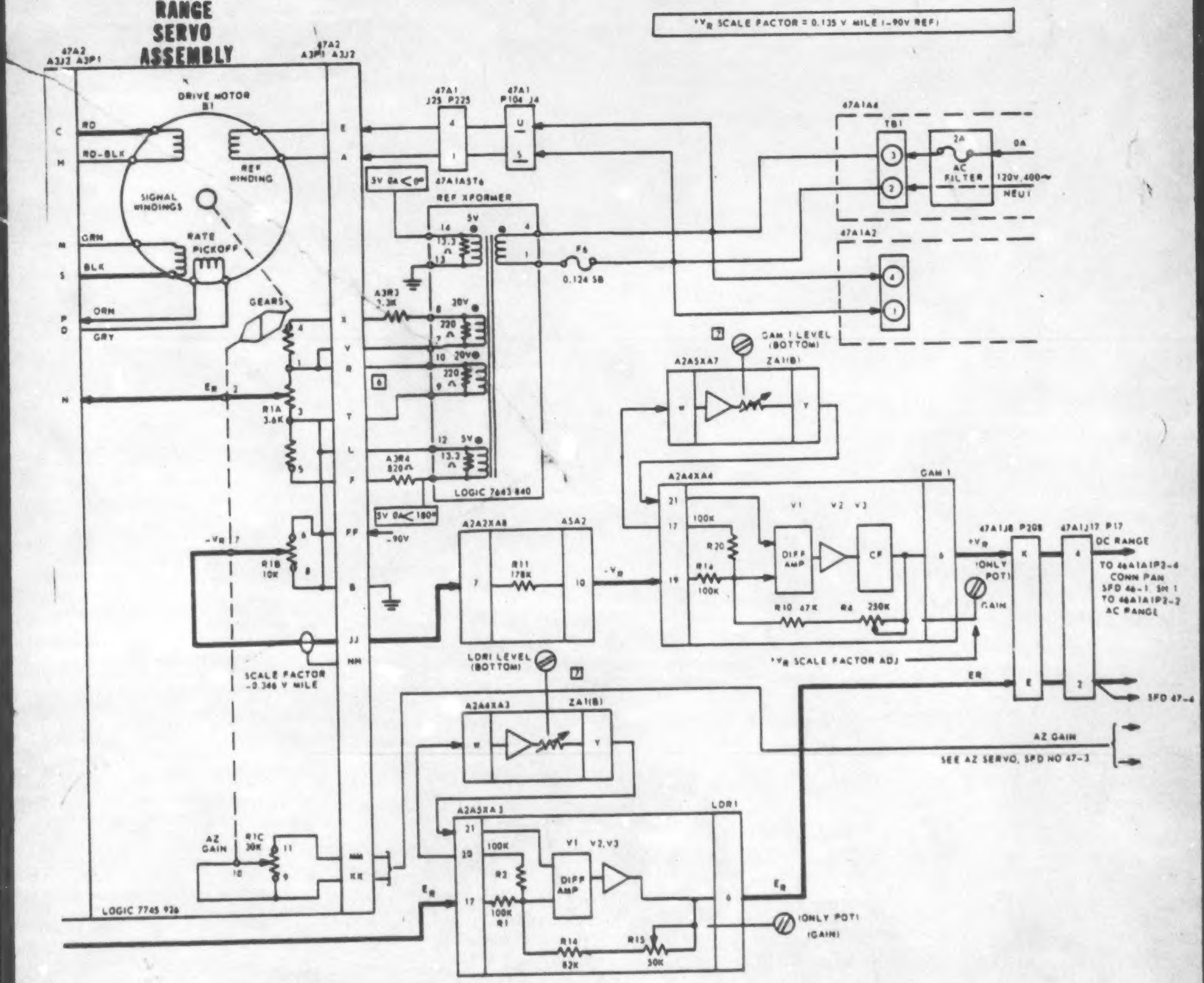

RANGE SERVO ASSEMBLY
47A2 A3J2 A3P1
47A2 A3P1 A3J2
DRIVE MOTOR B1
C
H
RD
RD-BLK
REF WINDING
SIGNAL WINDINGS
RATE PICKOFF
N
S
P
D
GRN
BLK
ORN
GRY
GEARS
N
E_R 2
R1A 3.6K
4
1
3
5
E
A
X
V
R
T
L
F
FF
B
JJ
NN
MM
KK
-V_R 7
R1B 10K
6
8
SCALE FACTOR -0.346 V MILE
AZ GAIN
R1C 30K
11
10
9
LOGIC 7745 936
47A1 J25 P225
4
1
47A1 P104 J4
U
5
5V 0A < 0°
47A1A5T6
REF XFORMER
5V
14
13.3 Ω
13
4
1
A3R3 3.3K
8
20V
220 Ω
7
10 20V
220 Ω
9
6
12 5V
13.3 Ω
A3R4 820 Ω
LOGIC 7643 840
5V 0A < 180°
-90V
F6
0.124 SB
+V_R SCALE FACTOR = 0.135 V MILE (-90V REF)
47A1A4
TB1
3
2
2A
AC FILTER
0A
120V, 400~
NEUT
47A1A2
4
1
7
GAM 1 LEVEL (BOTTOM)
A2A5XA7
ZA1(B)
W
Y
A2A2XA8
A5A2
7
R11 178K
10
-V_R
A2A4XA4
GAM 1
21
17
19
100K
R20
R14 100K
V1
V2 V3
DIFF AMP
CF
R10 47K
R4 250K
6
+V_R
(ONLY POT)
GAIN
+V_R SCALE FACTOR ADJ
47A1J8 P208
47A1J17 P17
K
E
4
2
DC RANGE
TO 46A1A1P2-4 CONN PAN SFD 46-1, SH 1
TO 46A1A1P2-2 AC RANGE
ER
SFD 47-4
AZ GAIN
SEE AZ SERVO, SFD NO 47-3
LDR1 LEVEL (BOTTOM)
7
A2A4XA3
ZA1(B)
W
Y
A2A5XA3
LDR1
21
20
17
100K
R2
100K R1
V1
V2, V3
DIFF AMP
R14 82K
R15 30K
6
E_R
E_R
(ONLY POT)
(GAIN)

Figure 81. Complete servo with interrelated functions, outputs, and test data.

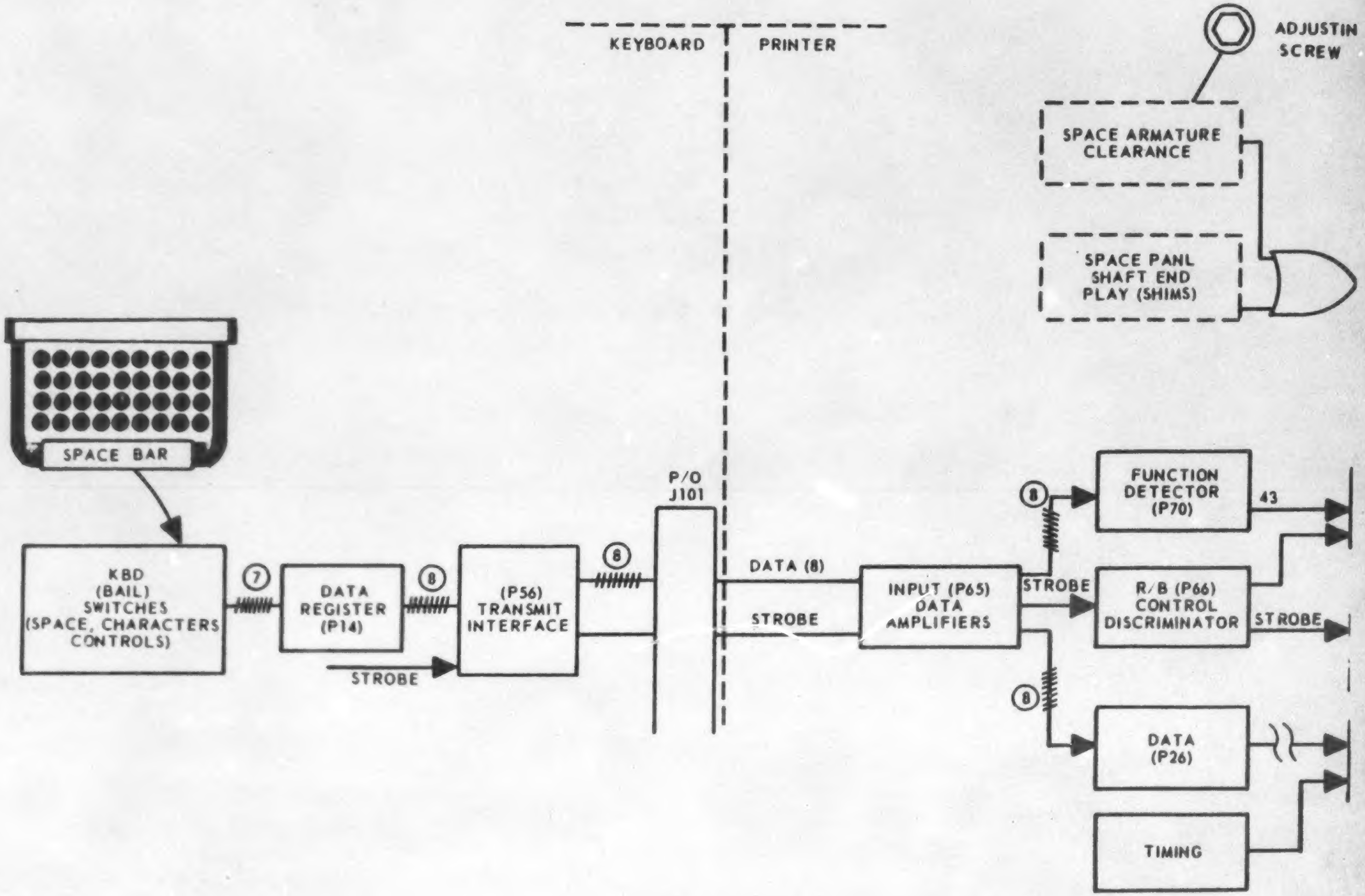
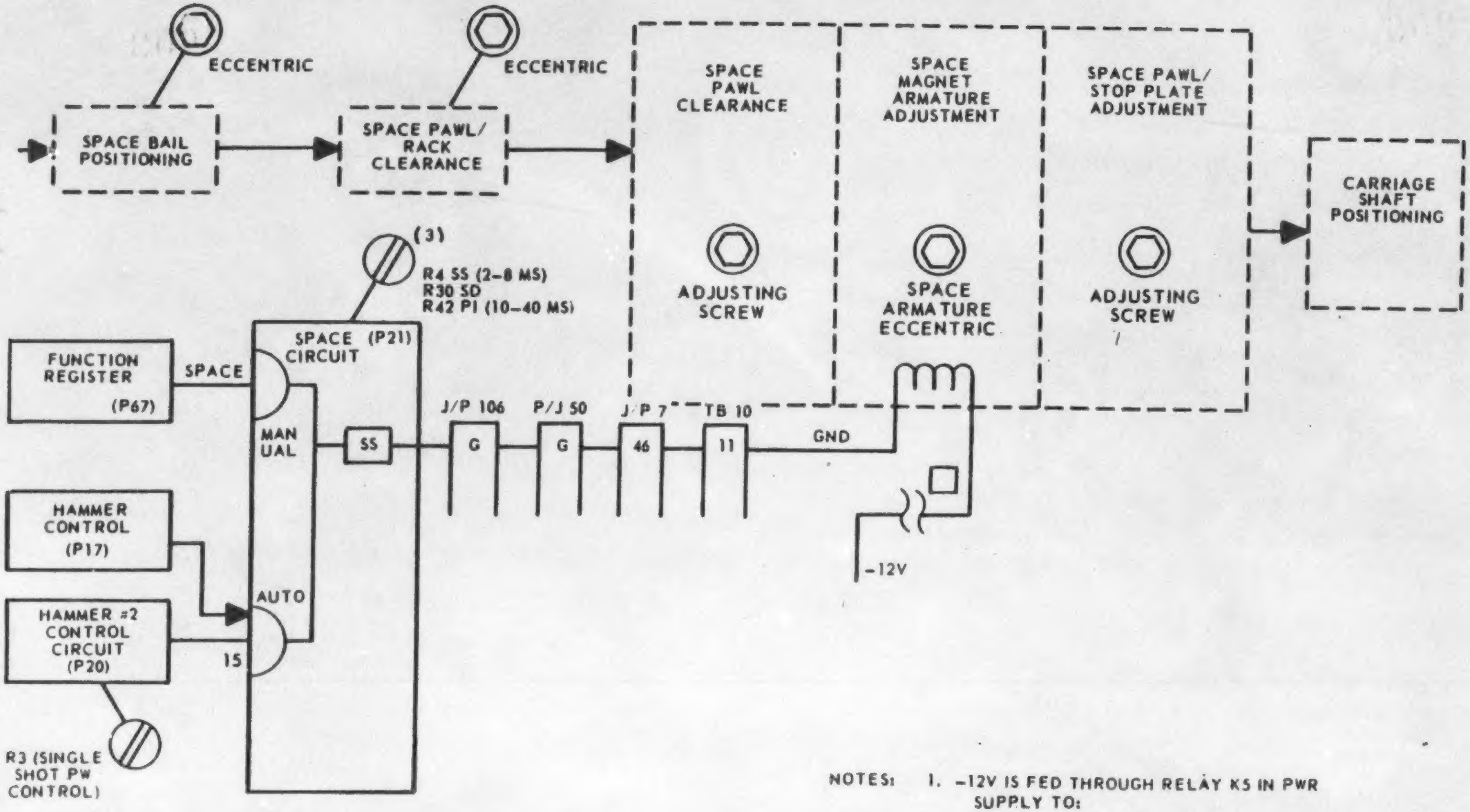
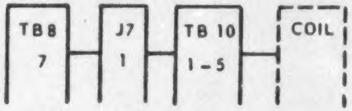

KEYBOARD
PRINTER
ADJUSTIN SCREW
SPACE ARMATURE CLEARANCE
SPACE PANL SHAFT END PLAY (SHIMS)
SPACE BAR
KBD (BAIL) SWITCHES (SPACE, CHARACTERS CONTROLS)
7
DATA REGISTER (P14)
8
STROBE
(P56) TRANSMIT INTERFACE
8
P/O J101
DATA (8)
STROBE
INPUT (P65) DATA AMPLIFIERS
8
STROBE
8
FUNCTION DETECTOR (P70)
43
R/B (P66) CONTROL DISCRIMINATOR
STROBE
DATA (P26)
TIMING

Figure 84 (cut apart)


ECCENTRIC
ECCENTRIC
SPACE BAIL POSITIONING
SPACE PAWL/ RACK CLEARANCE
SPACE PAWL CLEARANCE
SPACE MAGNET ARMATURE ADJUSTMENT
SPACE PAWL/ STOP PLATE ADJUSTMENT
CARRIAGE SHAFT POSITIONING
ADJUSTING SCREW
SPACE ARMATURE ECCENTRIC
ADJUSTING SCREW
(3)
R4 SS (2-8 MS)
R30 SD
R42 PI (10-40 MS)
SPACE (P21) CIRCUIT
FUNCTION REGISTER (P67)
SPACE
MAN UAL
SS
J/P 106
G
P/J 50
G
J/P 7
46
TB 10
11
GND
-12V
HAMMER CONTROL (P17)
AUTO
HAMMER #2 CONTROL CIRCUIT (P20)
15
R3 (SINGLE SHOT PW CONTROL)

NOTES: 1. -12V IS FED THROUGH RELAY K5 IN PWR SUPPLY TO:


TB8
7
J7
1
TB 10
1-5
COIL

2. TWO ELECTRONIC PATHS PROVIDE SOURCE GROUND FOR ARMATURE ENERGIZING.

3. SPACE BINARY CODE IS 0000010 (LSD LEFT)

Figure 84. Space interrelated functions.

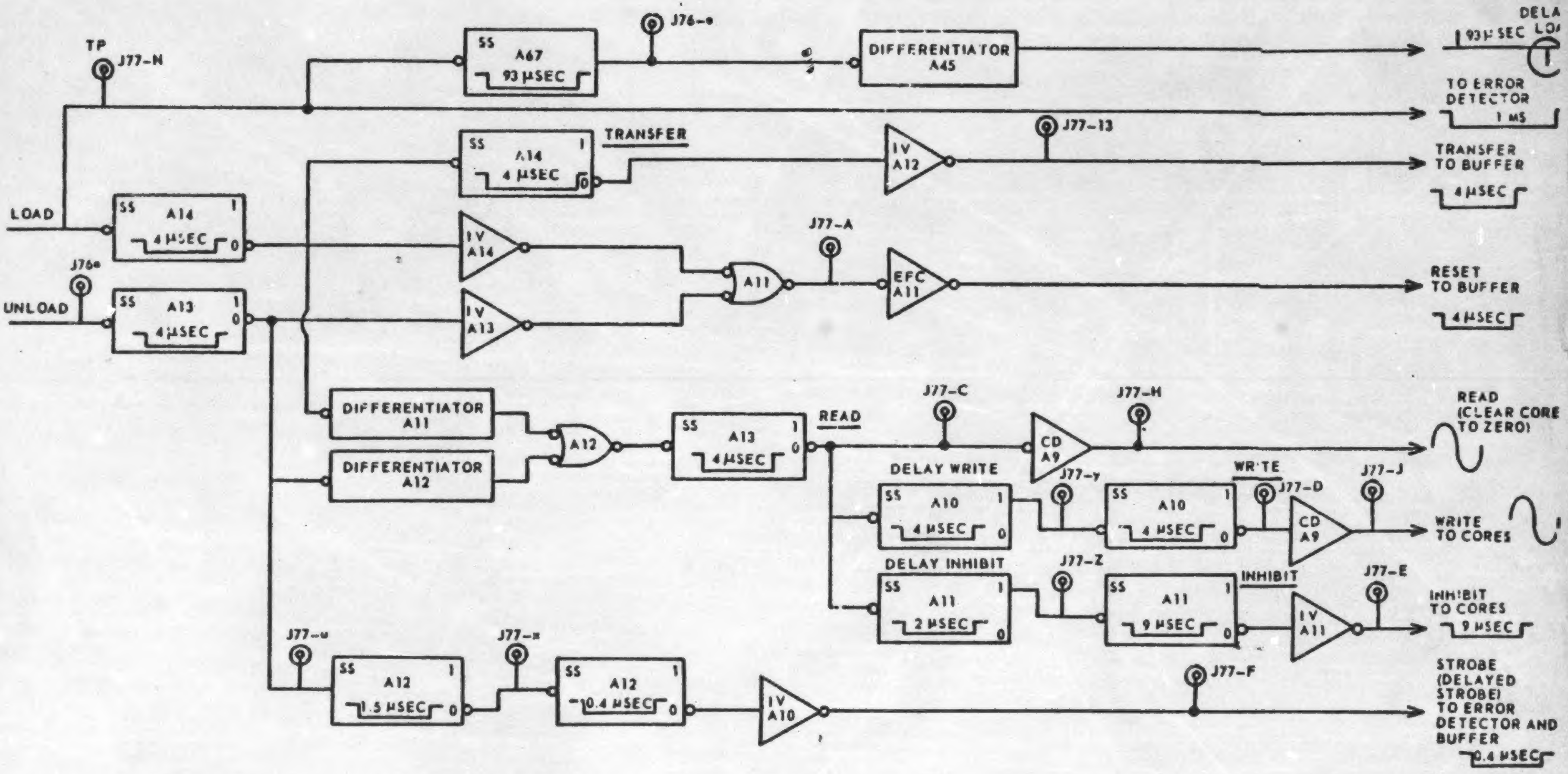

TP
J77-N
J76-e
SS A67 93 μSEC
DIFFERENTIATOR A45
DELA
93 μSEC
TO ERROR DETECTOR
1 MS
SS A14 4 μSEC
TRANSFER
J77-13
IV A12
TRANSFER TO BUFFER
4 μSEC
LOAD
SS A14 4 μSEC
IV A14
J77-A
A11
EFC A11
RESET TO BUFFER
4 μSEC
J76e
UNLOAD
SS A13 4 μSEC
IV A13
DIFFERENTIATOR A11
DIFFERENTIATOR A12
A12
SS A13 4 μSEC
READ
J77-C
CD A9
J77-H
READ (CLEAR CORE TO ZERO)
DELAY WRITE
SS A10 4 μSEC
J77-Y
SS A10 4 μSEC
WRITE
J77-D
CD A9
J77-J
WRITE TO CORES
DELAY INHIBIT
SS A11 2 μSEC
J77-Z
SS A11 9 μSEC
INHIBIT
IV A11
J77-E
INHIBIT TO CORES
9 μSEC
J77-u
SS A12 1.5 μSEC
J77-x
SS A12 0.4 μSEC
IV A10
J77-F
STROBE (DELAYED STROBE) TO ERROR DETECTOR AND BUFFER
0.4 μSEC

Figure 114 (cut apart)

593

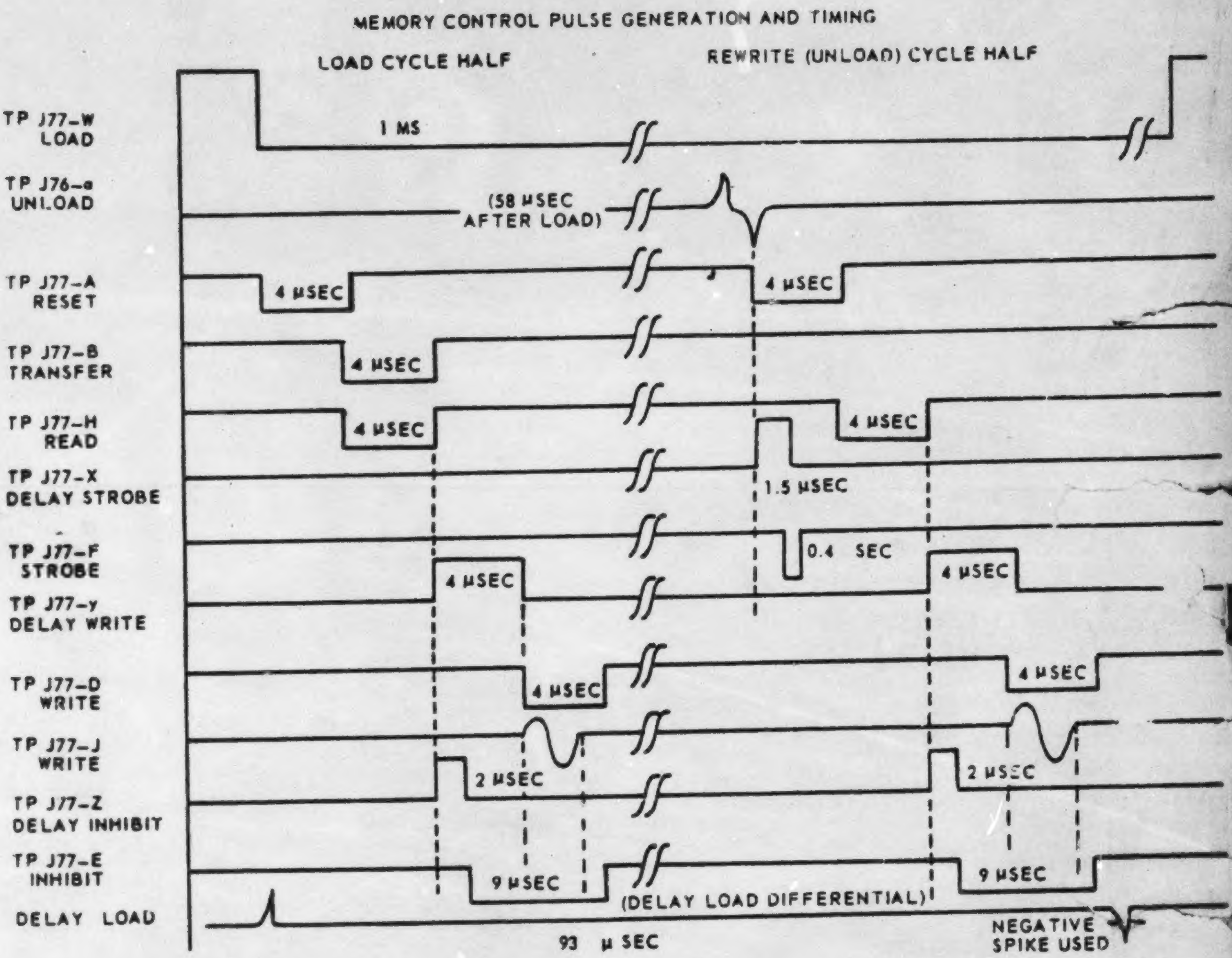

MEMORY CONTROL PULSE GENERATION AND TIMING
LOAD CYCLE HALF
REWRITE (UNLOAD) CYCLE HALF
TP J77-W LOAD
1 MS
TP J76-a UNLOAD
(58 µSEC AFTER LOAD)
TP J77-A RESET
4 µSEC
4 µSEC
TP J77-B TRANSFER
4 µSEC
TP J77-H READ
4 µSEC
4 µSEC
TP J77-X DELAY STROBE
1.5 µSEC
TP J77-F STROBE
0.4 SEC
4 µSEC
TP J77-y DELAY WRITE
4 µSEC
TP J77-D WRITE
4 µSEC
4 µSEC
TP J77-J WRITE
2 µSEC
2 µSEC
TP J77-Z DELAY INHIBIT
TP J77-E INHIBIT
9 µSEC
9 µSEC
(DELAY LOAD DIFFERENTIAL)
DELAY LOAD
93 µ SEC
NEGATIVE SPIKE USED

Figure 114. Memory control pulse generation and timing.